NEW ZVS PWM STEP-UP/STEP-DOWN DC-DC CONVERTER WITH ACTIVE CLAMPING TECHNIQUE

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Abstract – This paper presents a new regenerative step-up/step-down DC-DC converter, with active clamping and soft commutation. The losses in the switches are reduced due to implementation of the simple active snubber circuit, that provides ZVS conditions to all the interrupters of the converter, also in the auxiliary. Its main advantages are: small number of components, simple command strategy, robustness, reduced size and weight and high efficiency.

Keywords – active clamping, AGV, DC-DC converter, regeneration and soft commutation.

I. INTRODUCTION

In the industry, in the last years, the DC power drives have largely lost its popularity to the alternating current (AC) ones. The preference for the induction machines is known, mainly due to low maintenance, durability and reduced cost. However, in certain applications, DC machines are not easy to be replaced. They are still found, for example, in AGV’s (Automatic Guided Vehicles) and in the electric fork lift trucks, used in great part of the industrial environment.

Currently, amongst the problems associated to the AGV’s, has been pointed out the low relative autonomy of the batteries, and the necessity of the use of special machines and low voltage DC power drives, that usually have high cost and are difficult to be found.

This paper has as one of the main objectives, to present an alternative to power drive industrial vehicles using batteries, but making possible the use of AC machines and inverters, easily found in the market under reduced costs.

II. DEVELOPMENT

A. Alternative Topology For The Power Circuit

The classic topology of the power circuit of an AGV can be observed in the Figure 1. A critical point related to the efficiency of the DC-DC converter is verified, and as consequence, in the autonomy of the equipment. Moreover, for the power driving, special machines are used, what increases the final cost of the product.

A possible alternative is a step-up/step-down DC-DC converter reversible in current, with a CA power drive, as illustrated on Figure 2.

This converter must increase the voltage of the batteries for a level that makes possible the use of power inverters and AC machines.

In the stage step-up/step-down, the classic converters, have low efficiency, caused by the commutation losses, with are increased due to the high frequencies, and the high levels of voltage and current on the switches. The use of this alternative topology with a soft commutation, becomes sufficiently interesting.

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Fig. 1 Classic power topology of an AGV

Fig. 2 Alternative power topology to an AGV

The possibility of the use of CA machines present considerable advantage, as already mentioned. Moreover, the energy regeneration to be used, during the braking, will contribute to make the time of use of the vehicle longer. And still, through the diverse developed techniques, the frequency inverters also allow the vehicle control with great precision.

B. Commutation Switches Considerations

The architectures that use the bridge configuration have some peculiar characteristics. At the moment that the main switch turns on, the anti-parallel diode of the bridge complementary switch begins its reverse recovery phase. During this stage the switches are submitted to a high current ramp rate (di/dt) and a high peak reverse recovery current I_r. Both contribute significantly to the increasing of the commutation losses and produce electromagnetic interference.

To solve this problem, diverse works had been developed by the scientific community in the last years and can be divided in two groups: Passive Techniques [1], [2], [3], [4] and [5], and Active Techniques [6], [7], [8], [9] and [10]. The main difference between the two is that the second group use controlled switches in the auxiliary circuit that helps the commutation.

Recently, some researches were made using the reverse-recovery energy from the diodes to obtain soft commutation
in the switches of the pre-regulated rectifiers with high power factor [11] and [12].

In this paper, a new ZVS PWM step-up/step-down DC-DC converter, with active clamping technique, is proposed. Your structure uses the reverse-recovery energy from the diodes to obtain soft commutation in all switches of circuit, including the auxiliary one.

C. Presentation And Analysis Of The Circuit

The proposed converter can be observed in the Figure 3. It is similar to a classic current reversible converter, with the inclusion of one auxiliary switch, one clamping capacitor and one small inductor. The capacitor Cs is responsible for the storage of the diode reverse recovery energy and for the clamping of switches voltage. The inductor Ls is responsible for the control of the di/dt during the diode reverse recovery time [13]. The Figures 04 and 05 illustrate the switches commands for the modes “step up” and “step down” respectively.

Some simplifications to facilitate the sketch of the operation stages of the converter will be also considered: The voltage in the capacitors Cout and C2, and the current in the inductor Ls will be considered constant during a period of switching. Finally, the set formed by the input voltage Vin and the inductance Lmin will be simplified by a current source, called of Iin.

First stage (t0-t1): This interval initiates with the input current Iin delivering energy to the source Vin via diode D2 and the inductor Ls. At the same time, the additional current iCs flows around the loop, formed by Qa, Ls and Cs. In the end of this stage, the current iCs will reach its maximum value, called of Ic.

Second stage (t1-t2): This stage starts when the auxiliary switch Qa is blocked. The current iCs begins the charge of the capacitor Cs from zero to Vout+VCs, and discharges C1 from Vout+VCs to zero.

Third stage (t2-t3): At this stage the voltage across C1 reaches zero, and it is clamping by the anti-parallel diode Da. So, the switch Qa conducts with ZVS condition. At this moment, the voltage Vout, is applied across the inductor Ls and the currents iLs decrease linearly. The diode D1 conducts the current iLs, while D2 conducts the current iLs+Iin.

Fourth stage (t3-t4): It begins when the current iLs inverts its direction and flows through the switch Q1. The current in D2 continues to decrease until inverting its direction, starting its reverse recovery phase. The inductor Ls limits the diLs/dt. In the end this stage the current in Ls is equal to Ic.

Fifth stage (t4-t5): This stage starts when the diode D2 finishes its reverse recovery phase. The current iLs increases, due the application of the voltage VCs across the inductor Ls. This stage finishes when the current in Ls reaches zero.

Sixth stage (t5-t6): At this stage the voltage across the capacitor C2 reaches zero, and it is clamped by the diode Da. Thus, the auxiliary switch Qa conducts with zero-voltage switching. The current iLs increases, due the application of the voltage Vout across the diode Da. The capacitor Ci is charged from zero to Vout+VCs, and the capacitor C2 is discharged from Vout+VCs to zero.

Seventh stage (t6-t7): This stage begins when the current iLs changes its direction and flows through the switch Qa. The current iLs continues to increase linearly.

Eighth stage (t7-t8): At this stage the switch Q1 is blocked, and the current in Cs inverts its direction and flows through the diode Da. The capacitance Ci is charged from zero to Vout+VCs, and the capacitor C2 is discharged from Vout+VCs to zero.

Ninth stage (t8-t9): It begins when the voltage across the capacitor C2 reaches zero, and it is clamped by the diode D2. The current iLs continues increasing. This stage finishes when iLs is equal to Iin and flows through the auxiliary switch Qa, restarting the first operation stage.

D. Operation Stages (Positive Half-Cycle)

The operation of the proposed converter is symmetrical for both positive and negative semi cycles. Thus, only for the first half cycle of the operation the circuit analysis will be made.

![Fig. 3 Regenerative ZVS converter circuit](image)

![Fig. 4 Switches commands in “step up” mode](image)

![Fig. 5 Switches commands in “step down” mode](image)
The circuit sketch of the mentioned stages of operation, and the respective waveforms, can be visualized in Figures 06 and 07, respectively.

**Fig. 6.a** First stage (t0-t1) and Second stage (t1-t2)

**Fig. 6.b** Third stage (t2-t3) and Fourth stage (t3-t4)

**Fig. 6.c** Fifth stage (t4-t5) and Sixth stage (t5-t6)

**Fig. 6.d** Seventh stage (t6-t7) and Eighth stage (t7-t8)

**Fig. 6.e** Eighth stage (t7-t8) and Ninth stage (t8-t0)

**Fig. 7** Theoretical waveforms

**E. Mathematical Analysis**

The output voltage converter is controlled by the duty cycle $D$, as follow:

$$D = \frac{V_{out} - V_{in}}{V_{out}} \quad (1)$$
The inductor $L_{in}$ can be calculated by the use of the equation (2), as follow:

$$L_{in} = \frac{V_{in} \times T_{s}}{\Delta l_{in}} \cdot D$$  \hspace{1cm} (2)

One of the most important characteristics of the proposed converter is the voltage clamping over the switches. As indicated previously, its maximum voltage applied is $V_{cs} + V_{out}$. For the correct specifications of the components its necessary to know $V_{cs}$. The average current in $C_s$ must be zero to one period of switching in steady state conditions. Thus, its not difficult to see the follow relation:

$$i_{C_{ave}} = \frac{1}{T_s} \left[ \int_{0}^{t_f} \frac{V_{cs}}{L_s} \cdot t \cdot dt + \int_{t_f}^{t_1} \frac{V_{cs}}{L_s} \cdot t \cdot dt \right]$$  \hspace{1cm} (3)

Where, $T_s$ is the switching period.

Solving (3) and considering the expressions (4), (5) and (6), its possible to get the equation (7).

$$D = \frac{t_1}{T_s}$$  \hspace{1cm} (4)

$$t_1 \approx T_s$$  \hspace{1cm} (5)

$$i_{C_{ave}} = 0$$  \hspace{1cm} (6)

$$V_{cs} = \frac{2L_{s}}{T_s} \left[ I_{r} + I_{in}(1 - D) \right]$$  \hspace{1cm} (7)

The input current $I_{in}$ can be calculated by the use of the equation (8), as follow:

$$I_{in} = \frac{P_{out}}{\eta \cdot V_{in}}$$  \hspace{1cm} (8)

Where, $\eta$ is the efficiency of the converter.

By link of the equations (7) and (8) its possible to get the equation (9):

$$V_{cs} = \frac{2 \cdot L_{s}}{T_s} \left[ I_{r} + \frac{P_{out}(1 - D)}{\eta \cdot V_{in}} \right]$$  \hspace{1cm} (9)

As mentioned previously, $I_{r}$ is the maximum value of the reverse recovery current of the anti-parallel diode. There it can be obtained by the equation (10), as follow:

$$I_{r} = \frac{4}{3} \cdot \frac{Q_{rr}}{L_{s}} \cdot \frac{V_{out}}{\sqrt{3}}$$  \hspace{1cm} (10)

Where, $Q_{rr}$ is the reverse recovery charge.

To guarantee ZVS conditions, it is necessary, in the second stage, that the stored energy in the inductor $L_{s}$ be sufficient to discharge the capacitor $C_1$ and to charge $C_a$. Thus, by inspection of Fig. 6.a (Interval t1-t2) the following condition can be formulated:

$$L_{s} \cdot I_{f}^2 \geq (C_a + C_1)(V_{out} + V_{cs})^2$$  \hspace{1cm} (11)

Where $I_{f}$ is the maximum current in $C_s$, and $V_{cs}$ is maintained constant during a switching period. Assuming $V_{cs} << V_{out}$ we have:

$$I_{f} \cdot \min \geq V_{out} \cdot \sqrt{\frac{C_1 + C_a}{L_{s}}}$$  \hspace{1cm} (12)

Where, its possible to use $C_1 = C_a$.

The equation (12) to indicate the minimum value that the current $I_{f}$ must be to agree the ZVS commutation in all range to a determined condition of load.

An expression to the current $I_{f}$ can be obtained by the analysis of the current in the capacitor $C_S$. Thus:

$$I_{f} = \frac{V_{cs}}{L_{s}} \cdot T_s - \frac{I_{in}}{2} - I_{r}$$  \hspace{1cm} (13)

This way, $I_{f}$ can be obtained by use of equation (13), but your value must be bigger than the obtained in the equation (12).

The inductor $L_{s}$, that is responsible to the control of the current ramp rate, can be calculated by the use of the equation (14), as follow:

$$L_{s} = \frac{V_{out}}{\frac{dI_{f}/dt}{dt}}$$  \hspace{1cm} (14)

F. Project Results Summary

Following the equations of the mathematical analysis, the information had been concentrated through tables.

Thus, the initial design specifications, and the main results can be observed in the Tables 01 and 02, respectively.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>Initial Design Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in} = 48V_{cc}$</td>
<td>Input Nominal Voltage</td>
</tr>
<tr>
<td>$V_{out} = 200V_{cc}$</td>
<td>Output Nominal Voltage</td>
</tr>
<tr>
<td>$P_{out} = 1000W$</td>
<td>Output Nominal Power</td>
</tr>
<tr>
<td>$\eta = 95%$</td>
<td>Esteem Efficiency</td>
</tr>
</tbody>
</table>
TABLE II
Main Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>0.76</td>
</tr>
<tr>
<td>( F_s )</td>
<td>40kHz</td>
</tr>
<tr>
<td>( L_a )</td>
<td>10( \mu )H</td>
</tr>
<tr>
<td>( L_{in} )</td>
<td>830( \mu )H</td>
</tr>
<tr>
<td>( I_{in} )</td>
<td>22A</td>
</tr>
<tr>
<td>( I_r )</td>
<td>28A</td>
</tr>
<tr>
<td>( V_{Cs} )</td>
<td>13.5V</td>
</tr>
<tr>
<td>( I_{cap} )</td>
<td>28.5A</td>
</tr>
<tr>
<td>( I_{out} )</td>
<td>5A</td>
</tr>
<tr>
<td>( C_{out} )</td>
<td>475( \mu )F</td>
</tr>
</tbody>
</table>

TABLE III
Main Components Specifications

<table>
<thead>
<tr>
<th>Component</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1, Q2, Qa</td>
<td>Switches: APT5010B2VR</td>
</tr>
<tr>
<td>D1, D2, Da</td>
<td>Switches Intrinsic Diodes</td>
</tr>
<tr>
<td>C1, C2, Ca</td>
<td>Switches Intrinsic Capacitances ((\approx5)nF)</td>
</tr>
<tr>
<td>Lin</td>
<td>Iron-Silicon Inductor: (A_p=34.81cm^2, A_c=6.8cm^2, W_a=5.12cm^2, nfp=36,) wires=23AWG, 21 turns, and (l_g=0.041cm).</td>
</tr>
<tr>
<td>Ls</td>
<td>Ferrite Inductor: IP6-EE42/20, (nfp=20,) wires=23AWG, 17 turns, and (l_g=12.85mm).</td>
</tr>
<tr>
<td>Cs</td>
<td>Electrolytic Capacitor: 2 x 470(\mu)F/400V</td>
</tr>
<tr>
<td>Cout</td>
<td>Electrolytic Capacitor: 2 x 470(\mu)F/400V</td>
</tr>
</tbody>
</table>

G. Experimental Waveforms

In Figure 8 are presented the signals to the command of the switches Q1, Q2 e Qa. In the Figures 9 and 10 are showed the voltage and current in Q1. Of similar form, in the Figures 11 and 12 are showed the voltage and current in Qa. Finally, on Figure 13 is presented the voltage over de capacitor \(C_s\) and on Figure 14 the efficiency.
III CONCLUSIONS

This paper showed a new ZVS PWM step-up/step-down DC-DC converter, with active clamping technique. Was presented the operational stages, the values obtained of the equations, the mains waveforms and experimental results.

The converter was not tested in the nominal rated power because a limitation of our laboratory equipament. However, with base on others works already elaborated, and with the gotten results, many conclusions had become possible. The voltage in the clamping capacitor it revealed low, privileging the sizing of the switches - low stress voltage. It was verified soft commutation, confirming the theoretical studies, and the losses in the switches had been inside of the waited one. As consequence, could have been used small heat dissipations, reducing the weight, the volume and the costs.

Beyond of that was said previously, it could be affirmed that the soft commutation brings, inherently, a reduction of the electromagnetic interference generated by the converter.

Finally, the main advantages associates were: use of a small number of components, simple command strategy, robustness, reduced size and weight, low harmonic distortion of current and high efficiency.

REFERENCES