A Three-Phase Step-Up DC–DC Converter With a Three-Phase High-Frequency Transformer for DC Renewable Power Source Applications

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***Abstract*—This paper presents a new three-phase step-up dc–dc converter with a three-phase high-frequency (HF) isolation transformer in an average current-mode controlled closed loop. This converter was developed for industrial applications where the dc input voltage is lower than the output voltage, for instance, in installations fed by battery units, photovoltaic arrays, or fuel cell systems. The converter's main characteristics are reduced input ripple current, step-up voltage, HF transformer, reduced output-voltage ripple due to three-pulse output current, and the presence of only three active switches connected to the same reference, this being a main advantage of this converter. By means of a specific switch modulation, the converter allows two operational regions, each one depending upon the number of switches in overlapping conditions—if there are two switches, it is called R_2 region, and if there are three switches, it is called R_3 region. An average current-mode control strategy is applied to input-current and output-voltage regulation. Theoretical expressions and experimental results are presented for a 6.8-kW prototype, operating in the R_2 region, and for a 3.4-kW prototype, operating in the R_3 region, both in continuous conduction mode.**

***Index Terms*—Average current-mode control, dc–dc power conversion, dc–dc step-up converter, high-frequency (HF) three-phase transformer, installations fed by dc power sources.**

I. Introduction

THE great necessity in several areas, particularly the industrial sector, for switch mode power converters with larger power ratings in the end of the 80s was the starting point for the appearance of high-frequency (HF) three-phase dc–dc converter. Since the first three-phase dc–dc isolated converter introduced by Prazad *et al.* in 1988 [1], the three-phase dc–dc development follows two paths, both with the same goal: to increase the electronic power density ratings. The new topologies are from the first path and have important propositions [1]–[9]. The second path is the soft commutation with its main contributions given in [10]–[12].

The typical architecture of an HF three-phase dc–dc isolated converter is shown in Fig. 1. In the input stage, the most common configuration is this stage to operate as a voltage source, while the output stage has current source characteristics like in [1], [3], [4], [6], [9], [11], and [12]. The advantages of three-phase dc–dc isolated solutions are as follows:

1) reduction of the input and output filters' volume, as well as the reduction of weight and size of the isolation transformers;
2) lower rms current levels through the power components, when compared to single-phase solutions for the same power ratings.

With the increasing threat of the fast depletion of resources such as petroleum, coal, and natural gas forces, people seek renewable energy sources, such as solar, wind, geothermal, and hydraulic energies. In recent years, fuel cell (FC) research and development have received special attention for their higher energy-conversion efficiency and lower CO_2 emissions than thermal engines in the processes of converting fuel into usable energies. For these systems, different power converter topologies can be used for the power electronic interface between them and the load. Basically, low-voltage high-current structures are needed because of its electrical characteristics. In these systems, a classical boost converter is often selected as a possible converter. However, a classical boost converter will be limited when the power increases (greater than 4.5 kW) or for higher step-up ratios (greater than two times). The major problems of using a single dc/dc converter connected with FC in high-power applications are the difficulty of the design of magnetic component and high FC ripple current, which may lead to the reduction of its stack lifetime. To overcome these limitations, the use of paralleling power converters with interleaved technique is also applied and may offer some better performances [13]–[19]. In industrial applications, the inverter systems, together with dc–dc high-voltage-ratio converters, that feed electrical power from low-voltage-level systems into the grid must convert their direct current into alternating current for the grid.

In [20], a study focusing on this, offering a comparative view of some dc–dc converters applied in systems in the medium power range of 20 kW and higher, is presented.

The three-phase step-up dc–dc isolated converter presented in this paper, Fig. 2, has all of the main advantages of the three-phase solutions presented up until now. Moreover, the reduced number of switches, if compared with other topologies, such as presented in [21], and the voltage step-up characteristic improve the efficiency and reduce, along with a high

Manuscript received July 1, 2009; revised December 4, 2009 and February 12, 2010; accepted March 26, 2010. Date of publication October 7, 2010; date of current version July 13, 2011. This work was supported in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior and in part by the Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq).

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Digital Object Identifier 10.1109/TIE.2010.2084971

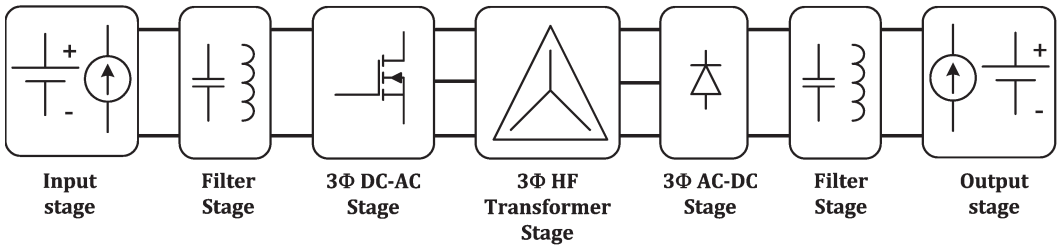

Fig. 1. Typical three-phase dc–dc converter architecture.

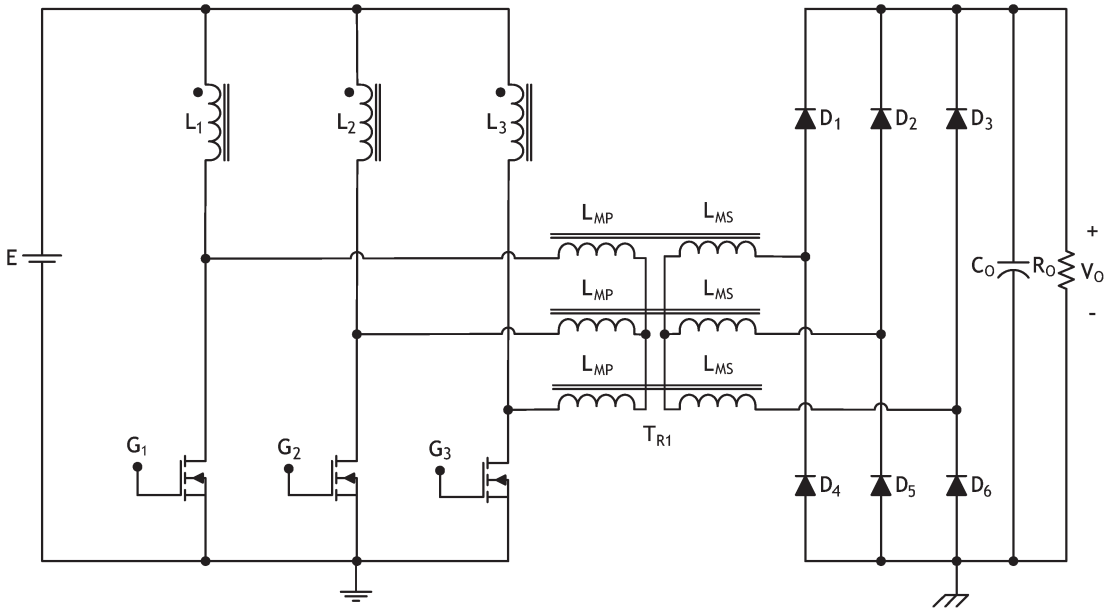

Fig. 2. Three-phase step-up dc–dc isolated converter.

TABLE I
OPERATION REGIONS FOR THE CONVERTER

Regions	Duty cycle	Switches status
1	D < 1/3	Forbidden
2	1/3 ≤ D ≤ 2/3	Up to 2 overlapped
3	D > 2/3	Up to 3 overlapped

switching frequency, the output filter volume, respectively. Furthermore, due to the input-current-source characteristic or nonpulsed input current, this topology can be adopted in all types of applications supplied by alternative energy sources, such as battery or photovoltaic (PV) arrays and, the more recent, FC systems. In this way, for the proposed converter, three converter operation regions are defined, each one depending upon the number of switches in overlapping conditions, Table I. Theoretical expressions and experimental results are presented for a 6.8-kW prototype, operating in region R_2, and for a 3.4 kW-prototype, operating in region R_3, both in continuous conduction mode (CCM).

II. PROPOSED CONVERTER AND THE OPERATION PRINCIPLE

A. Circuit Description

Fig. 2 shows the power stage of the proposed circuit [7]. The left side of the circuit (inverter) comprises three inductors and three switches connected to a dc link. The right side of the circuit is a traditional three-branch six-diode rectifier with a capacitive output filter. An HF three-phase transformer links to both sides.

The three-phase step-up dc–dc isolated converter characteristics are as follows.

1) The proposed three-phase inverter (left-side) circuit presents a low input ripple current, because it acts as nonpulsed current source, independent of both operation modes and regions of the converter.
2) The output-voltage ripple is reduced due to the three-pulse output current; consequently, a small capacitance value is required.
3) Only the three switches connected to the same reference attribute simplicity to the drive and control circuits.
4) The voltage level applied across the switches is reduced due to the employed transformer.

B. Analysis of Operation

To facilitate the analysis of the circuit operation, Fig. 2 shows a simplified circuit diagram. In the simplified circuit, Tr1 is modeled as an ideal transformer with turns ratio $n = 1$. It is assumed that its magnetizing inductance is large enough that it can be neglected. Moreover, it is assumed that the filter capacitor C is large enough and, thus, its output-voltage ripple

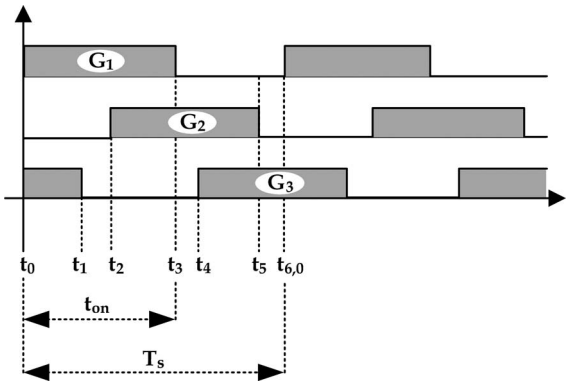

Fig. 3. Power switch driving signals for region R_2.

is small compared to its dc voltage. Finally, it is assumed that all semiconductor components are ideal, i.e., they present zero impedance when on and infinite impedance when off. The power flux transfer and the output/input voltage ratio are controlled by the duty ratio D of the switches.

A PWM technique is used for switches S_1, S_2, and S_3. The duty ratio D is defined by (1), where $t_{\rm ON}$ is the on-time interval of the switches and T_S is the switching period

$$D = \frac{t_{\rm ON}}{T_S}. \tag{1}$$

C. Operation Regions

The circuit proposed has three different operation regions according to Table I. Each one differs from each other by the number of switches in the ON state at the same time (overlapping). For each region, the duty cycle ratio can assume different values. Due to the converter's input-current-source characteristic, at least one switch must always be on. Hence, the first region, R_1 is forbidden. Fig. 3 shows a modulation of the switches for the converter operation in region R_2.

D. Steady-State Stage Operations for Region R_2

Fig. 4 shows the six topological stages of the converter's operation at R_2 region during a switching period.

1) First Stage (t_0, t_1)*—Fig. 4(a):* In t_0, switch S_1 is turned on and conducts along with switch S_3. Inductances L_1 and L_3 store energy from source E. The energy stored in L_2 is transferred to the load through D_2, D_4, and D_6. Currents $iD_4(t)$ and $iD_6(t)$ are added to $iS_1(t)$ and $iS_3(t)$, respectively. This stage finishes in t_1 when $\rm S_3$ is turned off.

2) Second Stage (t_1, t_2)*—Fig. 4(b):* In t_1, S_3 is turned off, and the energy stored in L_2 and L_3 is transferred to the load through D_3, D_2, and D_4. Current $iD_4(t)$ is added to $iS_1(t)$. This stage finishes in t_2 when S_2 is turned on.

3) Third Stage (t_2, t_3)*—Fig. 4(c):* In t_2, the energy of source E is stored in inductances L_1 and L_2. The energy stored in L_3 continues to be transferred to the load through D_3, D_4, and D_5. This stage finishes in t_3 when S_1 is turned off.

4) Fourth stage (t_3, t_4)*—Fig. 4(d):* In t_3, the energy stored in L_1 and L_3 is transferred to the load through D_1, D_3, and D_5. Current $iD_5(t)$ is added to $iS_2(t)$. This stage finishes in t_4 when S_3 is turned on.

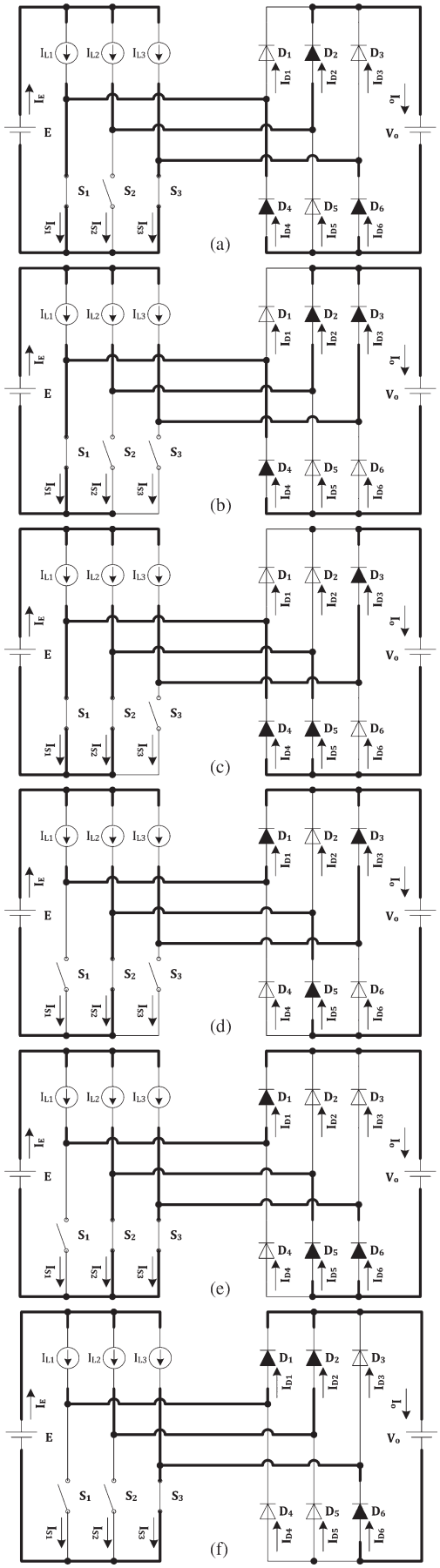

Fig. 4. Topological stages of the converter in region R_2.

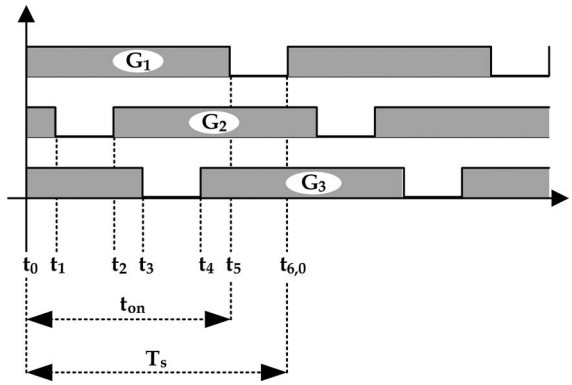

Fig. 5. Power switch driving signals for region R_3.

5) Fifth Stage (t_4, t_5)*—Fig. 4(e):* In t_4, the energy of source E is stored in inductances L_2 and L_3. The energy stored in L_1 continues to be transferred to the load through D_1, D_5, and D_6. This stage finishes in t_5 when S_2 is turned off.

6) Sixth Stage (t_5, t_6)*—Fig. 4(f):* The converter's last stage of operation in a T_S switching period starts at t_5, when S_2 is turned off. The energy from source E stored in inductances L_2 and L_1 is then transferred to the load through D_1, D_2, and D_6. $iD_6(t)$ is added to switch current $iS_3(t)$. In t_6, a switching period is finished.

E. Steady-State Stage Operations for Region R_3

Fig. 5 shows the modulation of the switches for the converter's operation in region R_3. Fig. 6 shows the topological stages of the converter's operation in R_3 region.

1) First Stage (t_0, t_1)*—Fig. 6(a):* In t_0, switch S_1 is turned on and conducts along with switches S_2 and S_3. Inductances L_1, L_2, and L_3 stored energy from source E. This stage finishes in t_1 when S_2 is turned off.

2) Second Stage (t_1, t_2)*–Fig. 6(b):* In t_1, S_2 is turned off, and the energy stored in L_2 is transferred to the load through diodes D_2, D_4, and D_6. Currents $iD_4(t)$ and $iD_6(t)$ are added to currents $iS_1(t)$ and $iS_3(t)$, respectively. This stage finishes in t_2 when S_2 is turned on.

3) Third Stage (t_2, t_3)*—Fig. 6(a):* In t_2, S_2 is turned on, and the first stage is repeated, with the energy of the source being stored in inductances L_1, L_2, and L_3. This stage finishes in t_3 when S_3 is turned off.

4) Fourth Stage (t_3, t_4)*—Fig. 6(c):* When S_3 is turned off, the energy stored in L_3 is transferred to the load through D_3, D_4, and D_5. Currents $iD_4(t)$ and $iD_5(t)$ are added to switch currents $iS_1(t)$ and $iS_2(t)$, respectively. This stage finishes in t_4 when S_3 is turned on again.

5) Fifth Stage (t_4, t_5)*—Fig. 6(a):* In t_4, S_3 is turned on, and the first stage is repeated, with the energy off the source being stored in inductances L_1, L_2, and L_3. This stage finishes in t_5 when S_1 is turned off.

6) Sixth Stage (t_5, t_6)*—Fig. 6(d):* The last stage starts at t_5, with S_1 being turned off and the energy stored in inductance L_1 being transferred to the load through diodes D_1, D_5, and D_6. Diode currents $iD_5(t)$ and $iD_6(t)$ are added to switch currents $iS_2(t)$ and $iS_3(t)$, respectively. In t_6, one period of switching operation is concluded.

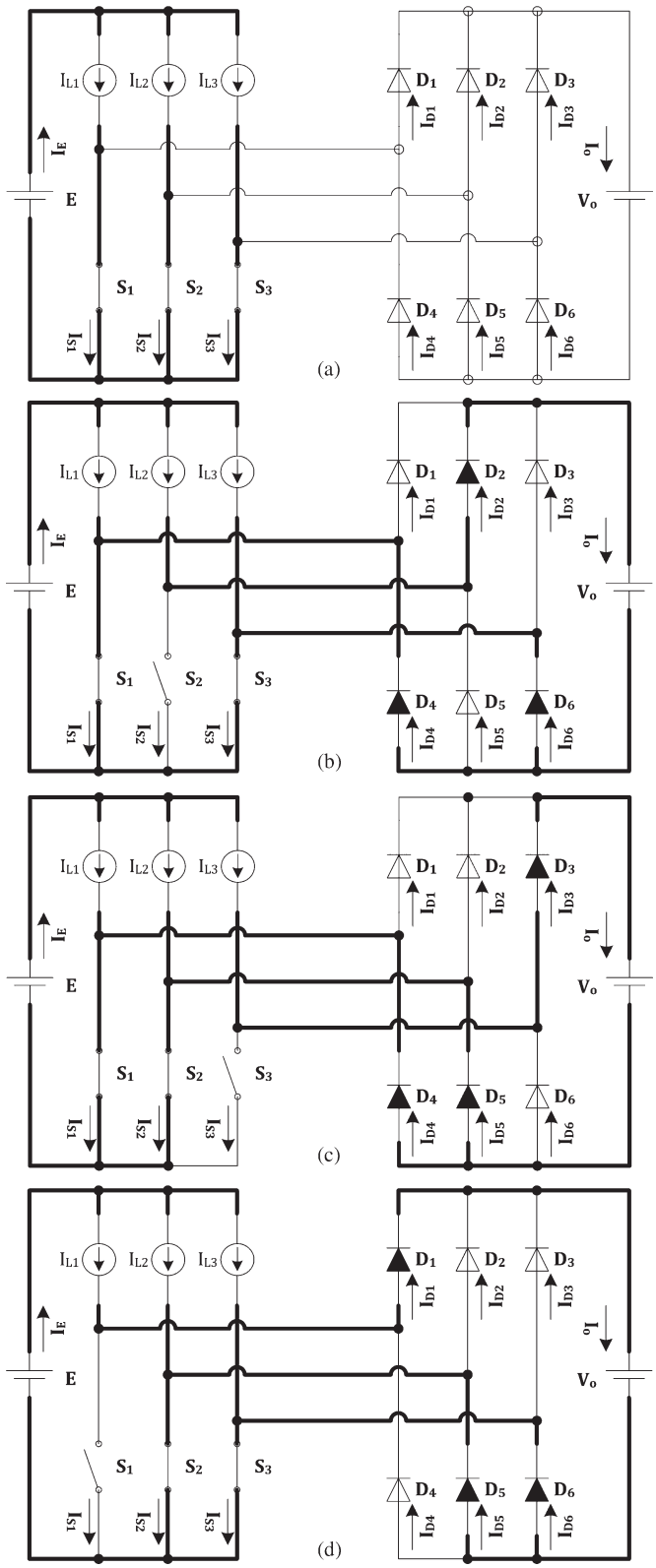

Fig. 6. Topological stages of the converter in operational region R_3.

III. Power Stage Design Procedure

The main equations (2)–(9) are used to design the power stage of the converter. Equation (2) gives the normalized output current, and (3) gives the turns ratio. By means of (4) and (5), the designer can determine the minimum value of inductances

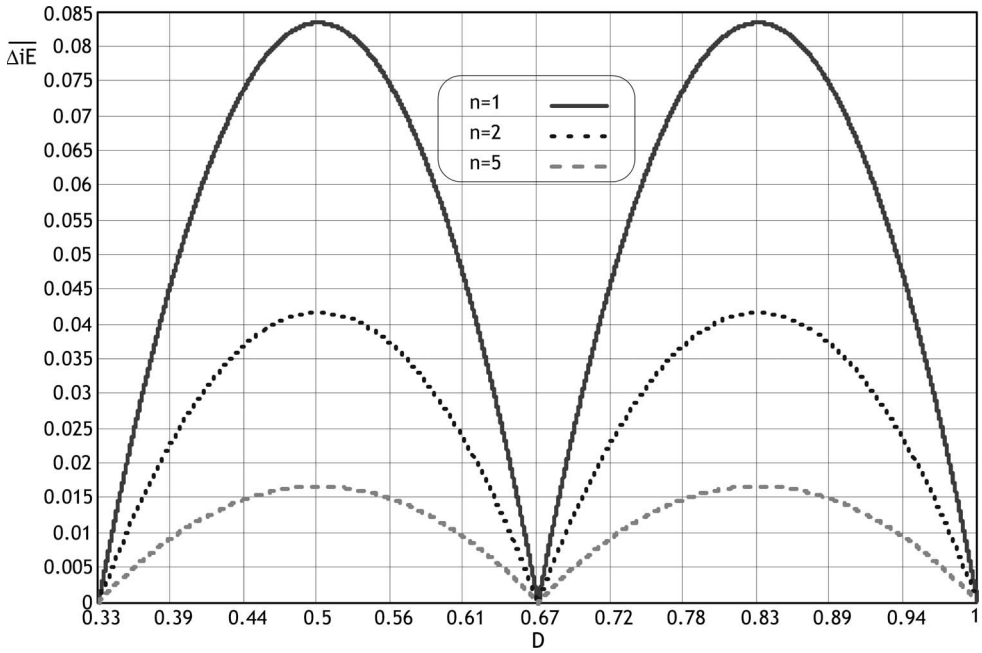

Fig. 7. Normalized input ripple current for both R_2 and R_3 operation regions.

to maintain the converter operation in CCM for a specific condition of load current.

Equation (6), plotted in Fig. 7, can be used to define the minimum inductances' values to guarantee a maximum ripple in the input current for $1/3 \leq D \leq 1$. In the Appendix, more detailed equations are shown to facilitate comprehension and the design of converter. Equations (7) and (8) can be used to determine the output capacitance and input inductance values in CCM, respectively

$$\overline{I_o} = \frac{I_o \cdot f_s \cdot L}{E} \tag{2}$$

$$n = \frac{N_s}{N_p} \tag{3}$$

$$\Delta iL = \frac{V_o}{fsL} \cdot \frac{D(1-D)}{n} = \frac{V_o}{fsL} \cdot \frac{q-n}{q^2}$$

$$\overline{\Delta iL} = \frac{D(1-D)}{n} = \frac{q-n}{q^2} \tag{4}$$

$$\begin{cases} L_{Cr} = \frac{\overline{\Delta iL}(n;0.5)}{n} \cdot \frac{V_o}{fs \cdot \Delta iL} \\ L_{Cr} = \frac{3}{16 \cdot n^2} \cdot \frac{V_o}{I_o \cdot fs} \\ \overline{L_{Cr}} = L_{Cr} \cdot \frac{I_o \cdot fs}{V_o} = \frac{3}{16 \cdot n^2} \end{cases} \tag{5}$$

$$\overline{\Delta i_E} = \begin{cases} \Delta i_E \cdot \frac{Lf_S}{V_o} \\ \frac{1}{3}\left(\frac{9n(q-n)-2q^2}{nq^2}\right) \rightarrow R_2 \\ \frac{3n-q}{q^2} \rightarrow R_3 \end{cases} \tag{6}$$

$$C = \begin{cases} \frac{I_o}{9nq} \cdot \frac{(2q-3n)(3n-q)}{f_S \Delta Vo} \rightarrow R_2 \\ \frac{I_o}{3q} \cdot \frac{(q-3n)}{f_S \Delta Vo} \rightarrow R_3 \end{cases} \tag{7}$$

$$L_{\min} = \frac{1}{12 \cdot n} \cdot \frac{V_o}{\Delta iE \cdot f_S}. \tag{8}$$

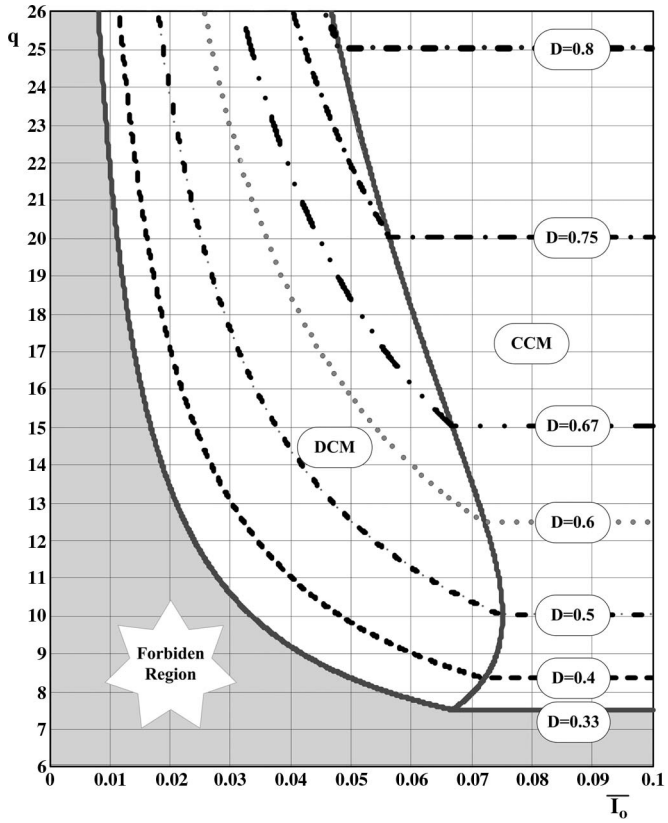

Fig. 8. DC transfer function of the proposed converter as a function of both duty cycle and normalized output current for $n = 5$.

IV. DC Transfer Function

Fig. 8 shows the three operation regions related to the output characteristic of the proposed converter. There, the three modes of conduction of the converter can be observed. The output/input voltage gain q or the dc transfer function for operation

area R_2 in CCM is limited to a maximum of three times the transformer's turns ratio. Otherwise, in region R_3, the minimum value of the output voltage in CCM is three times the transformer's turns ratio. The gain q for the three modes and two regions of converter operation is given by (9), detailed in the Appendix, and is shown in Fig. 8, highlighting that the duty cycle must be higher than 33% for the correct functionality of the converter.

Equation (9) was obtained applying the inductor voltage–second balance described in [22] and [23]. Figs. 9 and 10 show the theoretical waveforms for both regions of operation R_2 and R_3

$$q = \begin{cases} q_{\mathrm{CCM}} = n\left(\frac{1}{1-D}\right) \\ q_{\mathrm{CrCM}} = \frac{1}{4\overline{I_o}}\left(3 \pm \sqrt{9 - 24n\overline{I_o}}\right) \\ q_{\mathrm{DCM}} = n + \frac{3}{2}\left(\frac{D^2}{\overline{I_o}}\right). \end{cases} \tag{9}$$

V. Control Design

In this section, the average current-mode control technique applied to the regulation of both input current and output voltage of the converter is described [24]. Fig. 11 shows the feedback loop for input-current and output-voltage regulation. There are two loops, namely, inner current loop and outer voltage loop. $G_i(s)$ is the control-to-input-current transfer function, where the controlled variable is the input current $I_E(s)$ and the control variable is the duty ratio $d(s)$. $G_v(s)$ is the line-to-output or input-current-to-output-voltage transfer function. $C_i(s)$ and $C_v(s)$ are the current and voltage compensators, respectively. V_{ref} and I_{ref} are the references to be reached. The inner loop imposes an input current $I_E(s)$ as a function of the reference current generated by the outer loop. The current compensation network is designed as a function of the control criterion and by the response of the system.

The output-voltage control-loop action must change the input-current reference slowly, in relation to the current control-loop action in order to avoid the interference of the outer control loop.

A. Control Design Equations

The control transfer functions $G_i(s)$ and $G_v(s)$ are described by (10) and (11), respectively. Other modeling equations are presented at the Appendix

$$G_i(S) = \frac{I_E(S)}{V_C(S)} = G_{id}\frac{(S+\omega_{Zi})}{\left(\frac{S^2}{\omega_o^2} + \frac{S}{\omega_o Q} + 1\right)}$$

$$G_{id} = \frac{V_o \cdot C}{V_s(1-D)^2} \qquad \omega_{Zi} = \frac{2}{RC}$$

$$\omega_o = \frac{(1-D)}{\sqrt{LC}} \qquad Q = \sqrt{\frac{L}{C}}R(1-D) \tag{10}$$

$$G_v(S) = \frac{V_o(S)}{I_E(S)} = G_{vo}\frac{(S+\omega_{Zv})}{S(S+\omega_{Pv})}$$

$$G_{vo} = \frac{R \cdot R_{se}(1-D)}{(R+R_{se})n} \qquad \omega_{Zv} = \frac{1}{R_{se}C}$$

$$\omega_{Pv} = \frac{1}{(R+R_{se})C}. \tag{11}$$

VI. Prototype Description and Experimentation

The goal of this analysis is to show the advantages of using the proposed converter. The experimental results are obtained for a system with the following specifications:

1) $Po = 3.4$ and $6.8 =$ kW, output power;
2) $Vo = 450$ V, rated output voltage;
3) $E = 27$ and 47 V dc, rated input voltages;
4) $fs = 20$ kHz, switching frequency;
5) $n = 21/4$, transformer's turns-ratio;
6) $\Delta Vo \leq 9$ V, output ripple voltage;
7) $\Delta IE \leq 3$ A, input ripple current.

A. DC Voltage Gain

From the output and input rated voltages, the gain q is given by

$$q = \frac{450V}{47V} = 9.57. \tag{12}$$

B. Duty Ratio

The duty cycle ratio is given by

$$D = \frac{q-n}{q} = \frac{9.57 - 5.25}{9.57} \cong 0.45. \tag{13}$$

C. Input Inductances

The values of the inductances were defined, taking into account that the converter keeps operating in CCM, even with 10% of the rated power. Under these conditions, the inductance values are given by

$$L_{1,2,3} \geq 10\overline{L_{Cr}} \cdot \frac{V_o}{f_s \cdot I_o} \cong 134\ \mu\mathrm{H}. \tag{14}$$

D. Output Capacitance

The value of output capacitance is obtained using (7). However, due to its rms current stress, it was changed to 2000 μF/500 V.

E. Controller Design

The implementation of the compensators for input current and output voltage is realized by

$$C_i(S) = \frac{V_c(S)}{V_{i\mathrm{Hall}}(S)} = K_i\frac{(S+\omega_{Zci})}{S(S+\omega_{Pci})}$$

$$K_i = \frac{1}{R_{ci}C2_{fi}} = 555556$$

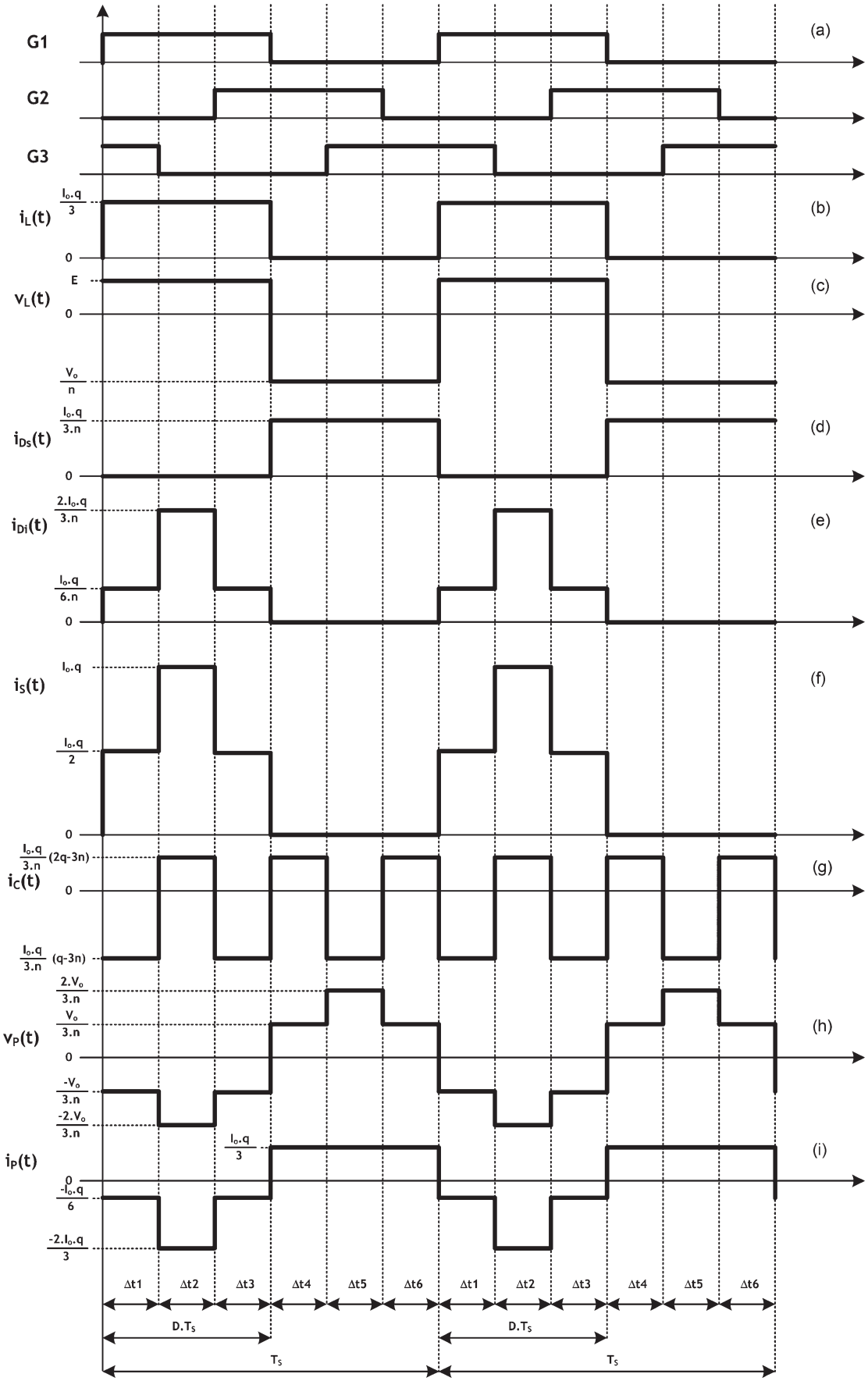

Fig. 9. Theoretical waveforms in R_2 for $D = 0.5$. (a) Command pulses. (b) L_1 inductor current. (c) L_2 inductor voltage. (d) D_1 output diode current. (e) D_5 and D_6 diode currents. (f) S_1 switch current. (g) Output capacitor current. (h) Primary winding voltage. (i) Primary winding current.

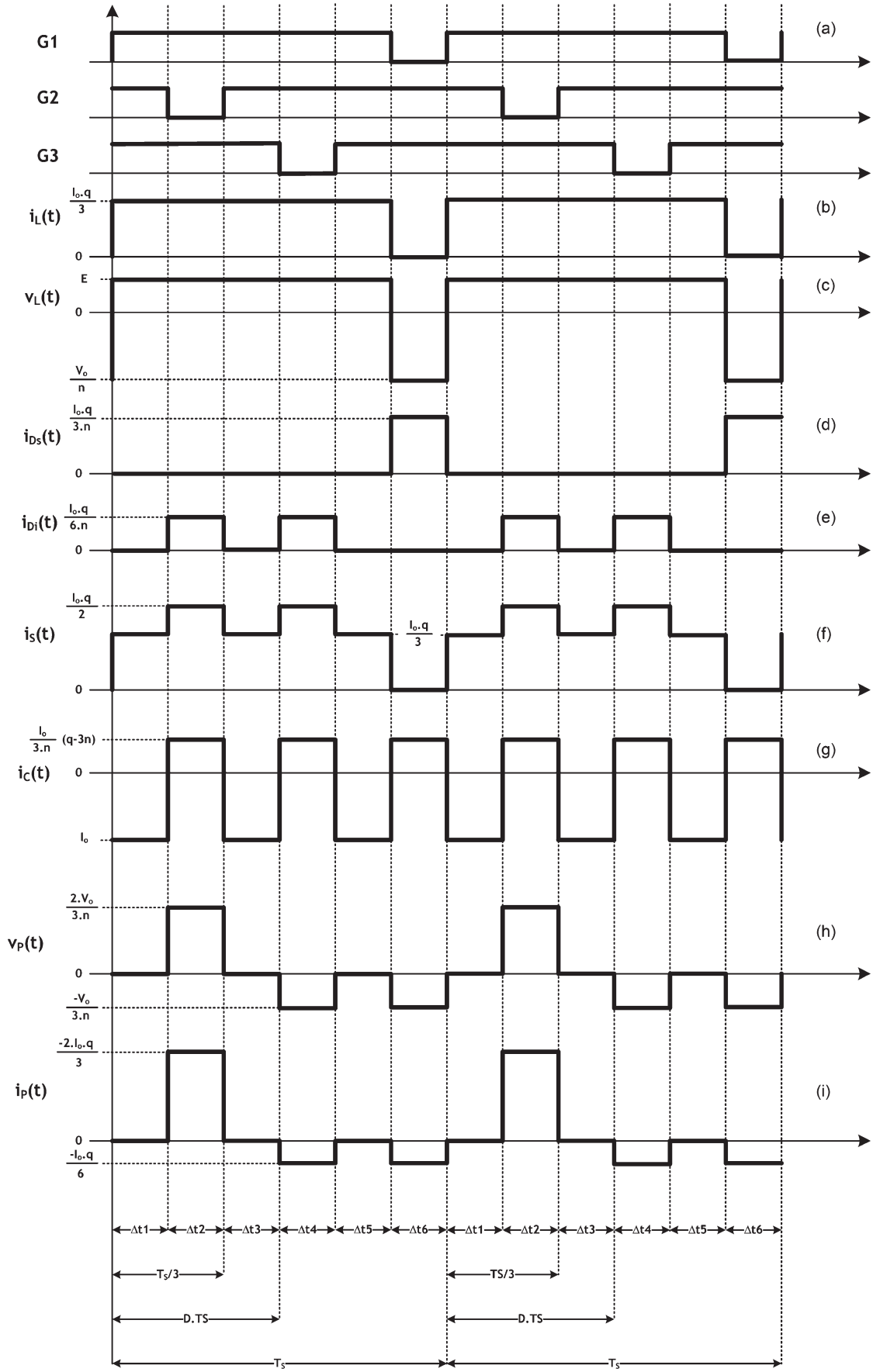

Fig. 10. Theoretical waveforms in R_3 for $D = 0.83$. (a) Command pulses. (b) L_1 inductor current. (c) L_2 inductor voltage. (d) D_1 output diode current. (e) D_5 and D_6 diode currents. (f) S_1 switch current. (g) Output capacitor current. (h) Primary winding voltage. (i) Primary winding current.

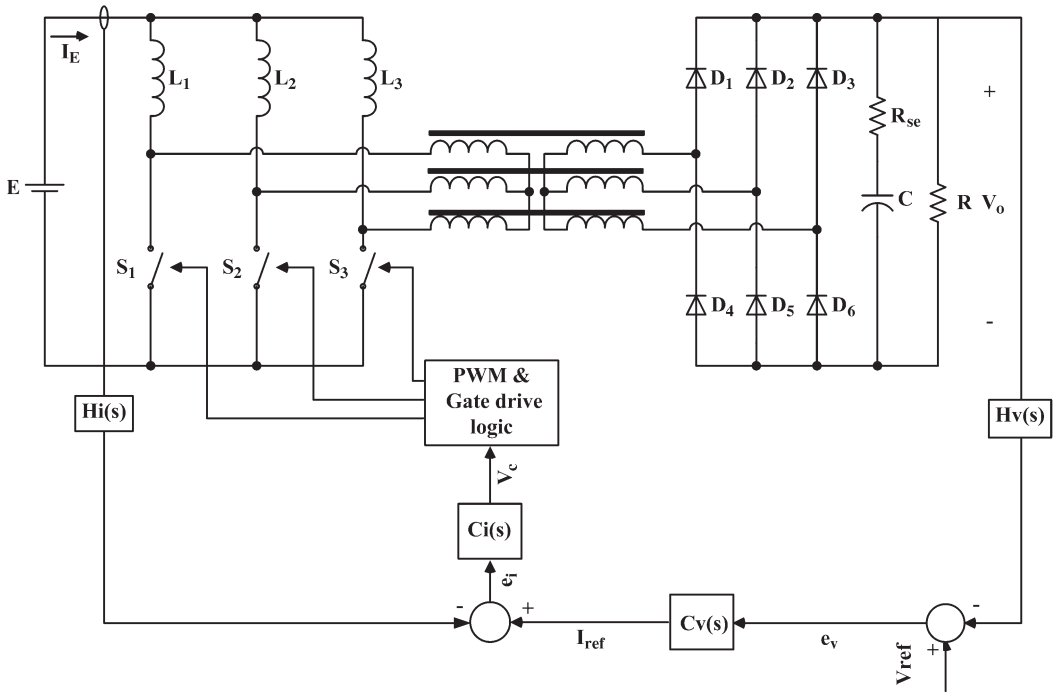

Fig. 11. Feedback loop for input-current and output-voltage regulation.

$$\omega_{Zi} = \frac{1}{R_{fi}C1_{fi}} = 1191\frac{\text{rad}}{\text{s}}$$
$$\omega_{Pi} = \left(\frac{C1_{fi}+C2_{fi}}{C2_{fi}}\right)\omega_{Zi} = 100397\frac{\text{rad}}{\text{s}} \quad (15)$$
$$C_v(S) = \frac{I_{\text{Ref}}(S)}{V_{v\text{Hall}}(S)} = K_v\frac{(S+\omega_{Zcv})}{S(S+\omega_{Pcv})}$$
$$K_v = \frac{1}{R_{cv}C2_{fv}} = 60.6$$
$$\omega_{Zcv} = \frac{1}{R_{fv}C1_{fv}} = 1250\frac{\text{rad}}{\text{s}}$$
$$\omega_{Pcv} = \left(\frac{C1_{fv}+C2_{fv}}{C2_{fv}}\right)\omega_{Zc} = 3230\frac{\text{rad}}{\text{s}}. \quad (16)$$

The crossover frequencies obtained from the current control and the voltage control loop are 12.2 and 1.8 kHz, respectively. The crossover frequency must be lower than the switching frequency, and a phase margin near to 45° provides good response with very little output-voltage overshoot. The conventional phase-margin and gain-margin stability criteria are applied to maintain the system stable.

F. Prototype Description

Using the design equations, a 6.8-kW prototype was implemented, as shown in Fig. 12. The main power components employed were three 134-μH inductors built in a toroidal core of Kool μ material, two output capacitors with 1000 μF/500 V (2XB43510) from Epcos, and three MOSFET switches SKM 121AR. The output rectifier diodes are the HFA15TB60 from IR.

The modulation strategy and the gate drives are allowed by the TMS320F2812 DSP Starter Kit. Three single-phase transformers in Y–Y connection operating as a three-phase HF transformer are employed; they use two ferrite cores 80-38-20 in parallel per phase of TSF 7070 material. The inductor currents are measured by three Hall-effect sensors LA100P from LEM.

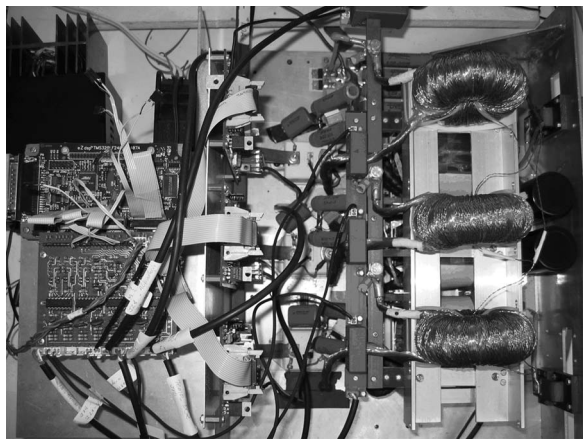

Fig. 12. Photograph of the prototype.

The snubber circuit in Fig. 13 is adapted from [25] and, containing Ds, Rs, and Cs, is used to control the overvoltage across the switches due to the leakage inductances (Ldp). It was implemented using $Rs = 50\ \Omega/50$ W, $Cs = 1\ \mu\text{F}/250$ V, and $Ds =$ HFA15TB60. Other details of the prototype and more experimental results for a 3.4-kW prototype operating in R_3 are presented.

G. Experimental Results

In Fig. 14, the three inductor currents of the Hall sensors, as well as the output voltage, are depicted. The currents

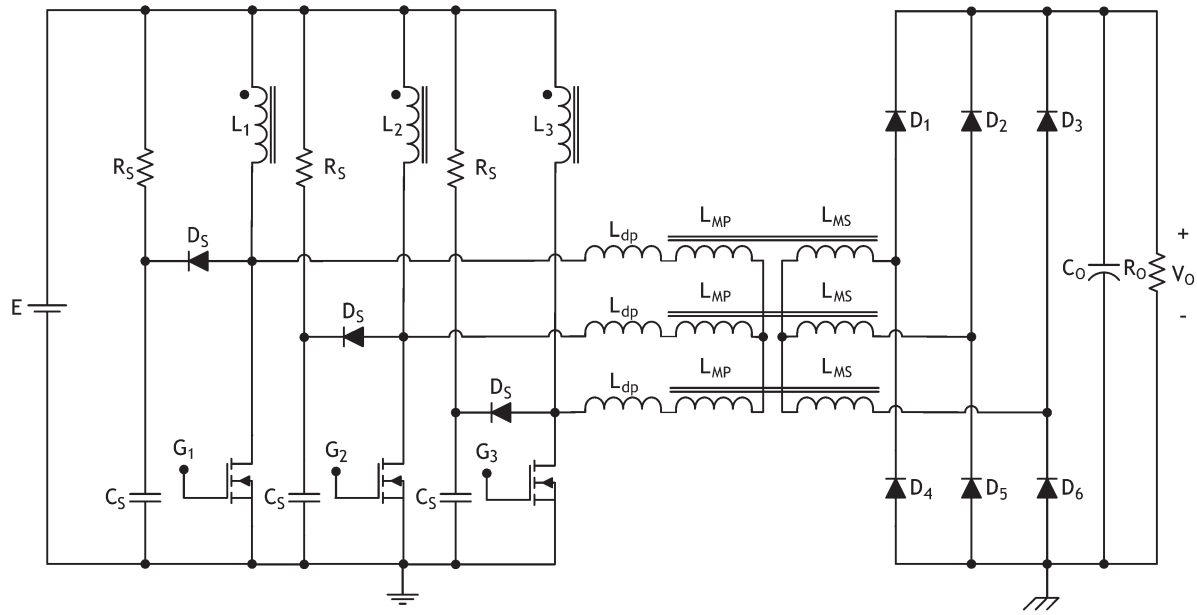

Fig. 13. Prototype schematic implemented.

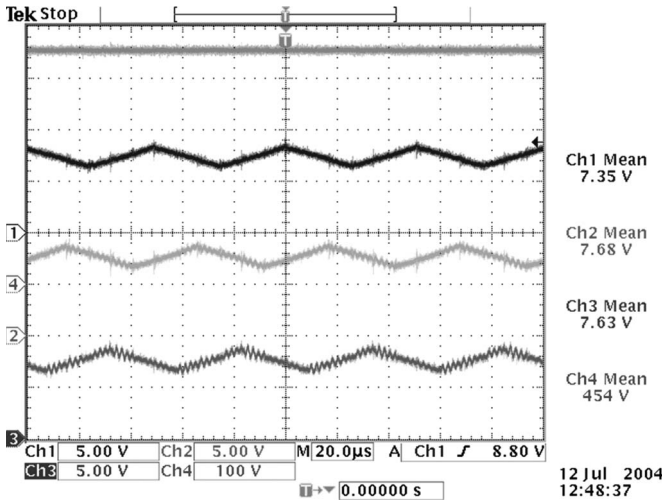

Fig. 14. (Ch4) Output voltage and inductor currents.

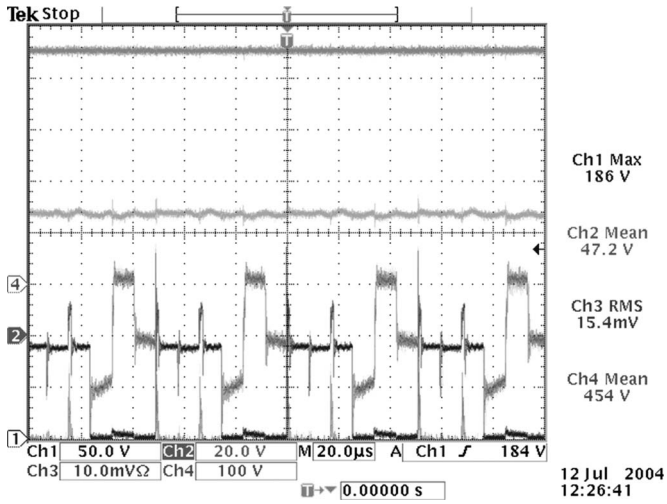

Fig. 15. Commutation of S_1, (Ch1) voltage (with 50 V/div), and (Ch3) current (with 50 A/div), plus the rated (Ch2) input and (Ch4) output voltages.

through the inductors are obtained by the conversion $i_{\mathrm{L}} = 100\ \mathrm{A} \cdot (v_{\mathrm{sensored}}/13.5\ \mathrm{V})$. The input current is the sum of the inductor currents. In Fig. 15, the commutation of switch S_1 on the rated power of the converter operation is shown. Fig. 16 shows the waveforms for a duty ratio of $D = 0.7$, i.e., the proposed converter is operating in region R_3. It is possible to verify the commutation of S_1 switch and both rated input and output voltages, respectively.

In Fig. 17, the converter's efficiency in the R_2 region is shown. The converter's efficiency is close to 87%.

Fig. 18 shows the output-voltage dynamic response for a load increment from 3.4 to 6.8 kW. Moreover, Fig. 19 shows the output-voltage variation for a reduction of the output power from 6.8 to 3.4 kW. In both transient responses, P_2 represents the rated load power, and P_1 denotes the 50% rated load power. The output-voltage overshoot is lower than 1% of the rated voltage.

VII. Conclusion

In order to develop a topology that presents greater efficiency with reduced weight and size, the three-phase step-up dc–dc isolated converter controlled by an average current-mode strategy has been presented. With these characteristics, this converter contains only three controlled switches and an HF transformer. The input and output filters are fed by three times the switching frequency, which will reduce their volume. This converter can be used in all applications that require a reduced input ripple current, e.g., in industrial applications where the dc input voltage is lower than the output voltage, for instance, in installations fed by battery units, PV arrays, or FC systems, since some of the features expected for these systems, such as nonpulsed input current and higher step-up ratios, can be obtained. The control model employed was the same with that of the classical boost dc–dc converter. Its simplicity joins with its very satisfactory results.

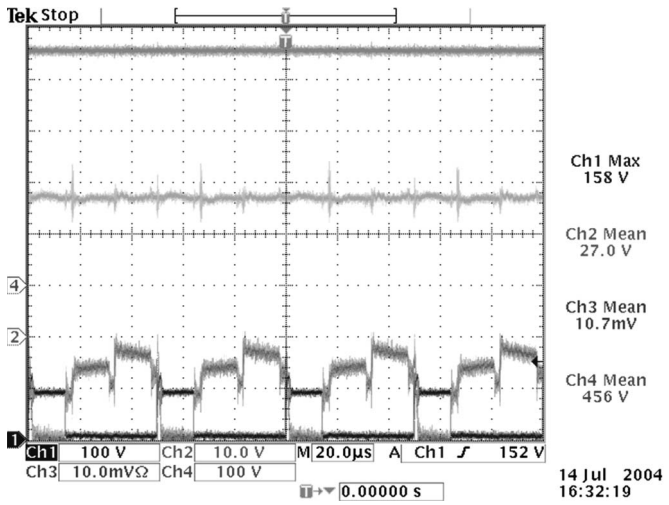

Fig. 16. Experimental results for operational region R_3: Commutation of S_1, (Ch1) voltage (with 50 V/div) and (Ch3) current (with 50 A/div), plus the rated (Ch2) input and (Ch4) output voltages.

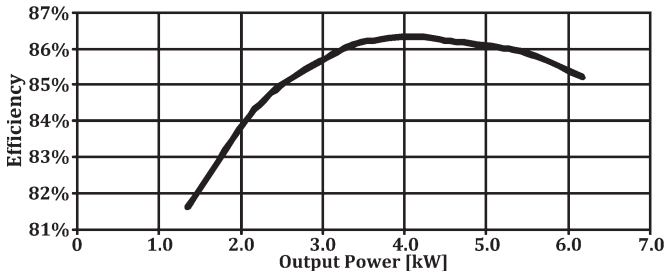

Fig. 17. Output converter's experimental efficiency on R_2.

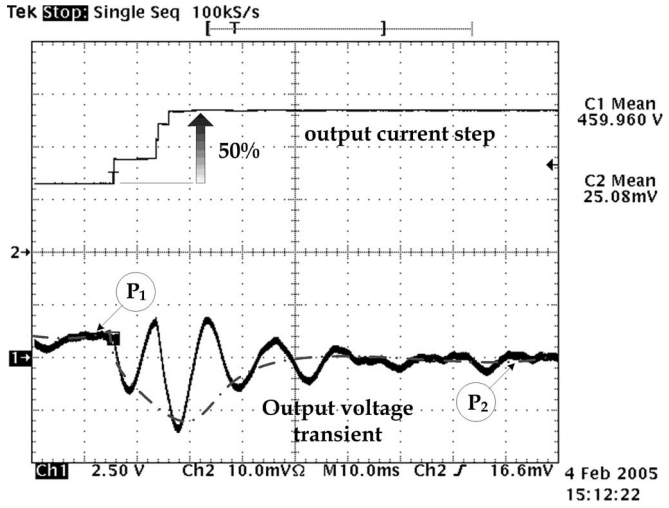

Fig. 18. Output voltage for an increment of 50% in the output power.

During the converter assembly, special care was taken in the construction of the transformer, mainly with respect to the reduction of its leakage inductance. This characteristic is an important constraint for choosing switching frequency.

The obtained efficiency for the converter operating at region R_2 was close to 87%; it can be considered high, considering its rated power and that it works with hard-switching commutation. With the goal of performing tests in both operational regions using the same prototype, in region R_3, results were obtained for a 3.4-kW output power and a 27-V input voltage for the same rated output voltage.

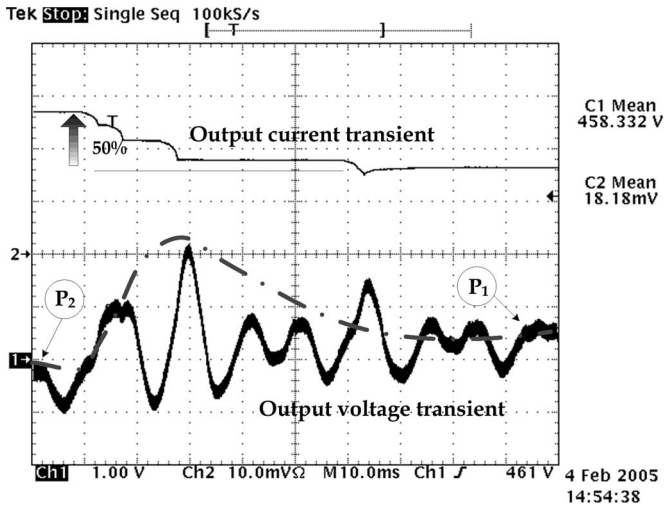

Fig. 19. Output voltage for a reduction of 50% in the output power.

APPENDIX

A. DC Transfer Function

In the following equations, the load variations are represented by means of the normalized output current $\overline{I}_o$. According to the converter's operational steps, the average output current is the sum of the average currents of the diodes (D_1, D_2, and D_3) given by (17). Using (18) and (19), (20), which evaluates the average load current, is obtained. From that, the normalized output current $\overline{I}_o$ is obtained by means of (21)

$$I_o = 3I_{D1} = \frac{3}{2} i L_{\max} \frac{\Delta_{td}}{T_S} \tag{17}$$

$$i_{L\max} = \frac{Vo}{fsL} \cdot \frac{D}{q} \tag{18}$$

$$\Delta td = \frac{i_{L\max} \cdot n \cdot L}{V_o - nE} \tag{19}$$

$$I_o = \frac{3}{2} \cdot \frac{D^2}{q-n} \cdot \frac{E}{fs \cdot L} \tag{20}$$

$$\overline{I_o} = I_o \cdot \frac{f_s \cdot L}{E} = \frac{3}{2} \cdot \frac{D^2}{q-n}. \tag{21}$$

From (21), the dc voltage gain in discontinuous conduction mode (DCM)($q_{\rm DCM}$) can be obtained by means of the following:

$$q_{\rm DCM} = n + \frac{3}{2}\left(\frac{D^2}{\overline{I_o}}\right). \tag{22}$$

In the critical conduction mode (CrCM), i.e., the boundary between the CCM and DCM, both $q_{\rm CCM}$ and $q_{\rm DCM}$ are equal,

and q_{CrCM} is described by means of (23). Thus, (9) synthesizes the voltage gain relations for all operational modes

$$\begin{aligned} & q_{\mathrm{MCC}} = q_{\mathrm{MCD}} \\ & \frac{n}{1-D} = n + \frac{3}{2}\cdot\frac{D^2}{\overline{I_o}} \\ & D = \frac{q_{\mathrm{CrCM}} - n}{q_{\mathrm{CrCM}}} \\ & 2\overline{I_o} q_{\mathrm{CrCM}}^2 - 3q_{\mathrm{CrCM}} + 3n = 0 \\ & q_{\mathrm{CrCM}} = \frac{1}{4\overline{I_o}}\cdot\left(3 \pm \sqrt{9 - 24n\overline{I_o}}\right). \end{aligned} \tag{23}$$

B. Modeling and Control

The adopted modeling is based on the development of the state-space equations for both nonlinear and linear models of the converter. The small-signal perturbations around the equilibrium values of the states are applied in the determination of both input-current and output-voltage control transfer functions. The models obtained show that they are very similar to the conventional dc–dc boost converter, for instance, traditional linear control strategies can be used to control it.

The state-space set of equations is defined in (24). The states x_1, x_2, and x_3 represent the inductors' currents, and the input current x_E is obtained by the instantaneous sum of them. The voltage across the output capacitor is represented by the state x_C, and the output variable y is the output voltage applied to the load. Equations (25) and (26) are used to represent the converter during the energy storage stages and the energy transfer stages, respectively

$$\begin{aligned} & x_1 = i_{L1}(t) \rightarrow \dot{x}_1 = \frac{di_{L1}(t)}{dt} \\ & x_2 = i_{L2}(t) \rightarrow \dot{x}_2 = \frac{di_{L2}(t)}{dt} \\ & x_3 = i_{L3}(t) \rightarrow \dot{x}_3 = \frac{di_{L3}(t)}{dt} \\ & x_C = v_C(t) \rightarrow \dot{x}_C = \frac{dv_C(t)}{dt} \\ & x_E = x_1 + x_2 + x_3 \\ & \dot{x}_E = \frac{d\left(i_{L1}(t) + i_{L2}(t) + i_{L3}(t)\right)}{dt} = \dot{x}_1 + \dot{x}_2 + \dot{x}_3 \\ & y = v_o(t) \end{aligned} \tag{24}$$

$$\begin{cases} L\cdot\dot{x}_1 + r_L\cdot x_1 = E \\ L\cdot\dot{x}_2 + r_L\cdot x_2 = E \\ \underbrace{L\cdot\dot{x}_3 + r_L\cdot x_3 = E}_{L\cdot\dot{x}_E + r_L\cdot x_E = 3E} \\ L\cdot\dot{x}_E + r_L\cdot x_E - 3E = 0 \\ C\cdot\dot{x}_C + \frac{1}{(R+Rse)}\cdot x_C = 0 \\ Y - x_C\frac{R}{(R+Rse)} = 0 \end{cases} \tag{25}$$

$$\begin{cases} L\cdot\dot{x}_1 + r_L\cdot x_1 = E - \left(\frac{Y+2V_D}{n}\right) \\ L\cdot\dot{x}_2 + r_L\cdot x_2 = E - \left(\frac{Y+2V_D}{n}\right) \\ \underbrace{L\cdot\dot{x}_3 + r_L\cdot x_3 = E - \left(\frac{Y+2V_D}{n}\right)}_{L\cdot\dot{x}_E + r_L\cdot x_E = \frac{3}{n}[nE-(Y+2V_D)]} \\ L\cdot\dot{x}_E + r_L\cdot x_E = \frac{3}{n}\left[nE - (Y+2V_D)\right] \\ C\cdot\dot{x}_C = \frac{1}{C\cdot n\cdot(R+Rse)}(R\cdot x_E - x_C n) \\ Y = \frac{R}{n(R+Rse)}(Rse\cdot x_E - x_C n). \end{cases} \tag{26}$$

Equation (27) describes the switched state-space model of the converter in terms of the switching function f. For the design of conventional feedback control compensation, it requires a model describing the converter's response to the modulating signal or the duty ratio $d(t)$

$$\begin{cases} \dot{x}_E = \frac{\left[(3E - r_L x_E)n^2(R+r_C) - 3R(1-f)(r_C x_E + n x_C)\right]}{n^2 L(R+r_C)} \\ \dot{x}_C = \frac{(1-f)x_E - n x_C}{nC(R+r_C)} \\ y = \frac{R[(1-f)r_C x_E + n x_C]}{n(R+r_C)}. \end{cases} \tag{27}$$

In (28), d represents the local average value of function $f(t)$ in a switching period. Applying the same concepts for all variables in (27), (29) is obtained, where the notation ($\widehat{\ }$) means that the variables are represented by their local average value

$$\begin{aligned} & \hat{d}(t) = \frac{1}{T_S}\int_{t-T_S}^{t} f(\tau)d(\tau) \\ & \hat{d} = \hat{f}(t) \end{aligned} \tag{28}$$

$$\begin{cases} \widehat{\dot{x}_E} = \frac{\left[(3\widehat{E} - r_L\widehat{x_E})n^2(R+r_C) - 3R(1-\widehat{d})(r_C\widehat{x_E} + n\widehat{x_C})\right]}{n^2 L(R+r_C)} \\ \widehat{\dot{x}_C} = \frac{(1-\widehat{d})\widehat{x_E} - n x_C}{nC(R+r_C)} \\ \widehat{y} = \frac{R\left[(1-\widehat{d})r_C\widehat{x_E} + n\widehat{x_C}\right]}{n(R+r_C)}. \end{cases} \tag{29}$$

To allow that the linear averaged models plus small perturbations around it represent the dynamic of the converter, the $\hat{d}$ variable must be described in terms of its rated value (D) and of its small perturbations $\tilde{d}$. From these assumptions, (30) represents the control variable modeled by its instantaneous average value

$$\widehat{d} = \widetilde{d} + D. \tag{30}$$

The equilibrium values of the states can be computed by (31). It was determined doing the $\widehat{\dot{x}_E}$ and $\widehat{\dot{x}_C}$ in (29) equal zero

$$\begin{aligned} & \overline{x_E} = I_E = \frac{3nV_o(1-D)(R+Rse)}{rL\cdot n^2(R+Rse) + 3R(1-D)\left[Rse + R(1-D)\right]} \\ & \overline{x_C} = V_o = \frac{I_E R(1-D)}{n}. \end{aligned} \tag{31}$$

Extending the concepts of small perturbations ($\sim$), applied in (30), to all variables of the system described in (31), the nonconservative linearized converter model is obtained, as described in (32), shown on top of the next page.

$$
\begin{aligned}
\widehat{x_E} &= I_E + \widetilde{x_E} \\
\widehat{x_C} &= V_o + \widetilde{x_C} \\
\widehat{d} &= D + \widetilde{d} \\
\begin{cases}
\begin{pmatrix} \dot{\widetilde{x_E}} \\ \dot{\widetilde{x_C}} \end{pmatrix} = \begin{pmatrix} -\frac{r_L n^2(R+r_C)+3Rr_C(1-D)}{n^2L(R+r_C)} & -\frac{3R(1-D)}{nL(R+r_C)} \\ \frac{R(1-D)}{nC(R+r_C)} & -\frac{1}{C(R+r_C)} \end{pmatrix} \cdot \begin{pmatrix} x_E \\ x_C \end{pmatrix} + \begin{pmatrix} \frac{3R(r_C I_E + nV_o)}{n^2L(R+r_C)} \\ -\frac{RI_E}{nC(R+r_C)} \end{pmatrix} \cdot \widetilde{d} \\
Y = \begin{pmatrix} \frac{Rr_C(1-D)}{n(R+r_C)} & \frac{R}{(R+r_C)} \end{pmatrix} \cdot \begin{pmatrix} x_E \\ x_C \end{pmatrix} + \left(-\frac{Rr_C I_E}{n(R+r_C)} \right) \cdot \widetilde{d}
\end{cases}
\end{aligned} \tag{32}
$$

$$
\begin{aligned}
G_I(S) &= \frac{x_E(S)}{d(S)} = Gpi \frac{S + \omega_{Zi}}{\left(\frac{S}{\omega_o}\right)^2 + \frac{S}{\omega_o Q} + 1} \\
G_V(S) &= \frac{x_C(S)}{d(S)} = Gpv \frac{S - \omega_{Zv}}{\left(\frac{S}{\omega_o}\right)^2 + \frac{S}{\omega_o Q} + 1} \\
\omega_o &= \frac{1}{n(R+r_C)} \sqrt{\frac{r_L n^2(R+r_C) + 3R(1-D)\left[R(1-D)+r_C\right]}{LC}} \\
Q &= \frac{\sqrt{LC}\left[n(R+r_C)\right]\left\{r_L n^2(R+r_C) + 3R(1-D)\left[R(1-D)+r_C\right]\right\}}{(R+r_C)\left\{n^2\left[r_L C(R+r_C)+L\right] + 3RCr_C(1-D)\right\}\sqrt{r_L n^2(R+r_C) + 3R(1-D)\left[R(1-D)+r_C\right]}} \\
Gpi &= \frac{9RV_o n(1-D)(R+r_C)\left\{C\left[2Rr_C + R^2(1-D) - RDr_C + r_C^2\right]\right\}}{\left\{r_L n^2(R+r_C) + 3R(1-D)\left[R(1-D)+r_C\right]\right\}^2} \\
\omega_{Zi} &= \frac{2R(1-D)+r_C}{C\left[2Rr_C + R^2(1-D) - RDr_C + r_C^2\right]} \\
Gpv &= -\frac{3V_o R(R+r_C)(1-D)\left[n^2L(R+r_C)\right]}{\left\{r_L n^2(R+r_C) + 3R(1-D)\left[R(1-D)+r_C\right]\right\}^2} \\
\omega_{Zv} &= \frac{3R^2(1-D)^2 - r_L n^2(R+r_C)}{n^2L(R+r_C)}
\end{aligned} \tag{33, 34}
$$

Applying the Laplace transformation concepts on (31) and (32), (33) and (34), shown on top of the page, are obtained. These ones, considering nonidealities like the series resistances of both input inductors (r_L) and output capacitor (r_C), are very similar to the conventional dc–dc boost converter transfer function.

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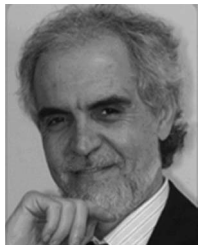

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