

MODELING AND CONTROL OF A THREE-PHASE PUSH-PULL DC-DC CONVERTER: THEORY AND SIMULATION

Hugo R. Estofanero Larico*, Diego S. Greff†, and Joselito A. Heerdt‡

*† Mechatronics Engineering, Federal University of Santa Catarina - UFSC, Joinville - SC, Brazil

‡ Department of Electrical Engineering, Santa Catarina State University - UDESC, Joinville - SC, Brazil
e-mail: hugo.larico@ufsc.br, diego.greff@ufsc.br, joselito.heerdt@udesc.br

Abstract—This paper presents closed loop control to a three-phase push-pull dc-dc converter. The converter originally offers the advantages of compact passive devices, low conduction power losses, low output ripples around duty cycle of 1/3. The control technique is based at inner control loop by current at switching transistors and an outer control loop by output voltage. The inner current control loop and the modulation proposed guarantee the operation of transformer out of core saturation area. Simulation results at closed loop were obtained on the mentioned converter with an input voltage of 120 V, output voltage of 48 V, load power of 500 W, and switching frequency of 35 kHz.

Index Terms—Three-phase DC-DC converter, transformer saturation, transformer flux control.

I. INTRODUCTION

THE growing market of renewable power systems, battery chargers, hybrid and electric vehicles demands widely application of low-voltage high-power dc-dc converters, where multiphase voltage-fed and current-fed push-pull converters are classical isolated dc-dc converters used due to their simplicity and good transformer core utilization [1,2].

Moreover, the evolution of energy conversion market have increased the need of dc-dc converters with high density of power optimizing the number of components, and this allow converters such the three-phase dc-dc push-pull converter [3] shown in Fig. 1, which presents inherent advantages of smaller filter sizes and capability to drive high current rates at low voltage rates. However, that converter is susceptible to transformer core saturation due to an imbalance in the volt-seconds applied to the phases, such as in the classical voltage-fed push-pull converter.

Thus, this study presents modeling and control for the three-phase dc-dc push-pull converter. In control section is proposed a current self-control [4,5] to balance leg currents in the three-phase transformer as well as to improve control action of the voltage loop. The main goal is to present a theoretical analysis of the converter in close loop. Thus, the theory is validated through simulation results.

II. THREE-PHASE DC-DC PUSH-PULL CONVERTER

The advantages of the three-phase dc-dc push-pull converter structure include:

- (1) Low conduction losses since there is only a single device voltage drop at the input and output and the RMS current of the power components is low;

- (2) Reduced number of components when compared to the classical three-phase dc-dc converter shown in Fig. 1: three switches, three diodes, a three-phase transformer (T), a filter inductor (L) and a filter capacitor (C);
- (3) Good transformer copper and core utilization since the windings are placed in a common magnetic core;
- (4) The switches can be driven directly by the control circuit since all of the switches are connected to the same reference point;
- (5) Small output filter size (L, C) since the frequency of the output ripple current is three times the switching frequency ($3f_s$); and
- (6) The maximum voltage of any switch is only one and a half times the input voltage ($3E_i/2$).

The small number of components and the reduction of transformer and output filter sizes allows for high-power density. Additionally, the reactive energy of the output filter (L, C) is zero when the duty cycle is equal to 1/3 ($\approx 33.33\%$).

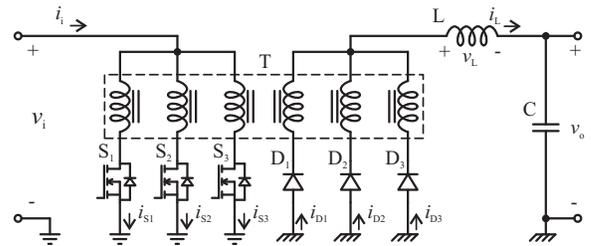


Fig. 1: Three-phase dc-dc push-pull converter.

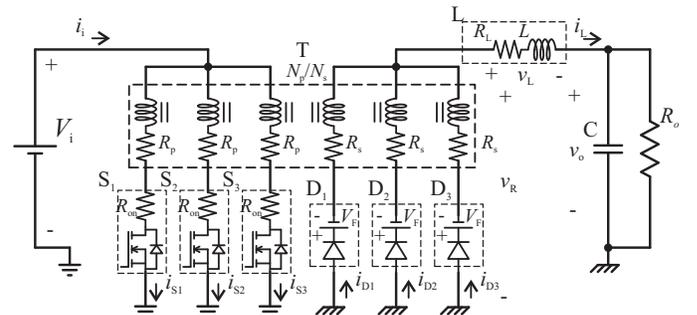


Fig. 2: Equivalent circuit of a three-phase dc-dc push-pull converter.

III. MODELING AND LINEARIZATION

The present section describes the modeling and linearization processes applied to the converter to obtain its transference functions. For this purpose the followed assumptions are made:

- (1) the input voltage is constant;
- (2) the equivalent series resistance (ESR) of output capacitor C is neglected;
- (3) the three-phase transformer is ideal, only the resistances of windings are considered;
- (4) the Mosfet transistor is represented by model with conduction losses R_S ; and
- (5) converter operating with duty cycle less than 1/3 and continuous conduction mode.

Fig. 2 shows equivalent circuit using aforementioned assumptions. Model of the converter is obtained using the averaged-circuit modeling. State equations, when one transistor is ON, are given by

$$\begin{aligned} L \frac{di_L}{dt} &= \frac{1}{2} V_i' - V_F - \left(\frac{R_p' + R_s}{2} + \frac{R_{on}'}{2} \right) i_L - R_L i_L - v_o \\ C \frac{dv_o}{dt} &= i_L - \frac{v_o}{R_o} \end{aligned} \quad (1)$$

where $V_i' = V_i N_s / N_p$ and $R' = R(N_s / N_p)^2$, and when all transistor are off are given by

$$\begin{aligned} L \frac{di_L}{dt} &= -V_F - \frac{R_s}{3} i_L - R_L i_L - v_o \\ C \frac{dv_o}{dt} &= i_L - \frac{v_o}{R_o} \end{aligned} \quad (2)$$

Considering $R_p' = R_s = R_t' / 2$ and the averaged value computed by

$$\bar{x}(t) = \frac{3}{T_s} \int_{t_o}^{t_o + T_s/3} x(t) dt \quad (3)$$

The averaged state-space model referred to secondary side of transformer is given by

$$\begin{aligned} L \frac{d\bar{i}_L}{dt} &= \frac{3}{2} V_i' d(t) - V_F - \left(R_t' + \frac{3R_{on}'}{2} \right) \bar{i}_L d(t) \dots \\ &\quad - \left(\frac{R_t'}{6} + R_L \right) \bar{i}_L \\ C \frac{d\bar{v}_o}{dt} &= \bar{i}_L + \frac{\bar{v}_o}{R_o} \end{aligned} \quad (4)$$

The linearized model is given by

$$\begin{aligned} L \frac{d\hat{i}_L}{dt} &= K_C \hat{d}(t) - R_c \hat{i}_L - R_L \hat{i}_L - \hat{v}_o(t) \\ C \frac{d\hat{v}_o}{dt} &= \hat{i}_L - \frac{\hat{v}_o}{R_o} \end{aligned} \quad (5)$$

where

$$\begin{aligned} K_C &= \frac{3}{2} V_i' - \left(R_t' + \frac{3R_{on}'}{2} \right) I_L \\ R_c &= \left(R_t' + \frac{3R_{on}'}{2} \right) D_o + \frac{R_t'}{6} \end{aligned}$$

The circuit model that represent linearized model given by (5) is shown in Fig. 3.

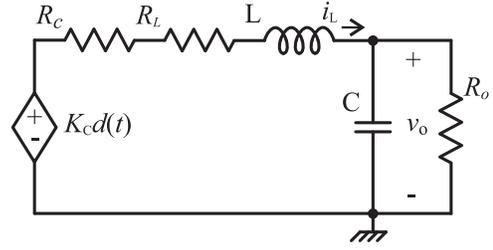


Fig. 3: Linearized circuit model.

IV. CONTROL OF THREE-PHASE DC-DC PUSH-PULL CONVERTER

A. Closed-loop current control

The current control is accomplished by making a direct feedback of sensed current through the duty cycle

$$\hat{d}(t) = \hat{v}_c(t) - k_i \hat{i}_L \quad (6)$$

where k_i is the gain of current sensor. Using (6) into (5) gives

$$\begin{aligned} L \frac{d\hat{i}_L}{dt} &= K_C \hat{v}_c(t) - R_{eq} \hat{i}_L - \hat{v}_o(t) \\ C \frac{d\hat{v}_o}{dt} &= \hat{i}_L - \frac{\hat{v}_o}{R_o} \end{aligned} \quad (7)$$

where

$$\begin{aligned} R_{eq} &= R_i + R_c + R_L; \\ R_i &= K_C k_i. \end{aligned}$$

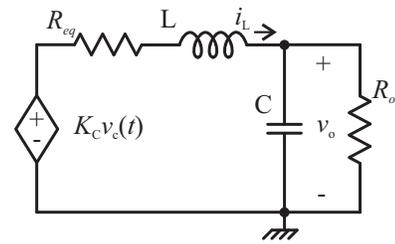


Fig. 4: Equivalent circuit with inner current loop.

According (7), the current loop introduces a fictional resistance R_i to equivalent circuit resistance R_{eq} that allows the inductor current damping at output side. The equivalent circuit is shown in Fig. 4. However, controlling of this output current is not capable to avoid transformer saturation, since magnetization current comes from input power supply. Consequently, a change of monitored current is required. Therefore, in different approach, and in order to avoid transformer saturation, the control loop by transistor current sensing instead the output inductor current is established and related by:

$$\langle i_S \rangle_{T_s} \approx \frac{1}{2} i_L d(t) \quad (8)$$

where

$$\langle i_S \rangle_{T_s} = \frac{1}{T_s} \int_{t_o}^{t_o+T_s} i_S dt \quad (9)$$

Applying (8) and (9) into (6) results

$$\begin{aligned} d(t)^2 &= v_c(t)d(t) - k_i \frac{2}{T_s} \int_c^{c+T_s} i_S dt \\ \frac{2k_i}{T_s} \int_{t_o}^{t_o+T_s} i_S dt &= v_c(t) \frac{t}{T_s} - \left(\frac{t}{T_s} \right)^2 \end{aligned} \quad (10)$$

Eq. (10) is used to define the configuration of modulator which is shown in Fig. 5. The control of transistor current allows to avoid transformer saturation and provide fault protection against short-circuit.

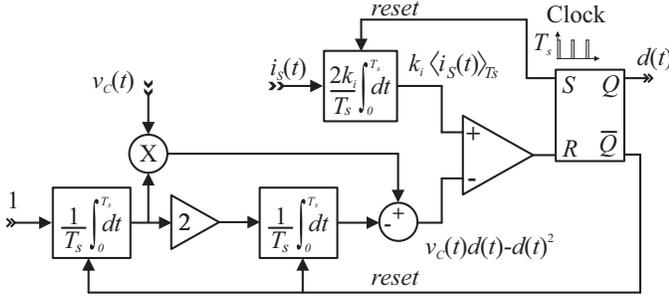


Fig. 5: Modulator diagram.

B. Closed-loop voltage control

Referred to Fig. 4, the voltage transfer function is given by expression (11).

$$\frac{V_o(s)}{V_c(s)} = \frac{K_C}{LCs^2 + \left(\frac{L}{R_o} + R_{eq}C \right) s + \frac{R_{eq}}{R_o} + 1} \quad (11)$$

The voltage loop consists in a classical output voltage control, using the following controller

$$C(s) = \left(K_p + \frac{1}{T_i s} \right) \frac{s + \sigma_z}{s + \sigma_p} \quad (12)$$

V. ANALYSIS IN STEADY STATE: FICTIONAL RESISTANCE

Equation (13) in steady state shown that fictional resistance does not affect static gain of converter.

$$\frac{V_o}{V_i'} = \left(\frac{3D}{2} - \frac{V_F}{V_i'} \right) \left(\frac{R_o}{R_o + R_L + R_t'/6 + D(R_t'/3 + R_{on}'/2)} \right) \quad (13)$$

On the other hand, fictional resistance determines damping of circuit in zero load.

$$\frac{V_o(s)}{V_c(s)} = \frac{K_C}{LCs^2 + R_{eq}Cs + 1} \quad (14)$$

The damping ratio is given by

$$\zeta = \frac{R_{eq}}{2} \sqrt{\frac{C}{L}} \quad (15)$$

Considering inductance and capacitance defined by

$$L = \frac{(1 - 3D_{min})R_o}{3f_s \% \Delta I_L} \quad (16)$$

$$C = \frac{\% \Delta I_L}{24f_s R_o \% \Delta V_o} \quad (17)$$

Thus the impedance of filter can be expressed by

$$\sqrt{\frac{L}{C}} = 2R_o \frac{\sqrt{2(1 - 3D)\% \Delta V_o}}{\% \Delta I_L} \quad (18)$$

Using (15) and (18) can be computed the equivalent resistance to guarantee a damping ratio in zero load.

$$\zeta = R_{eq} \frac{\% \Delta I_L}{4R_o \sqrt{2(1 - 3D)\% \Delta V_o}} \quad (19)$$

VI. SIMULATION RESULTS

Fig. 6 shown the schematic implemented for simulation and control loops block diagrams.

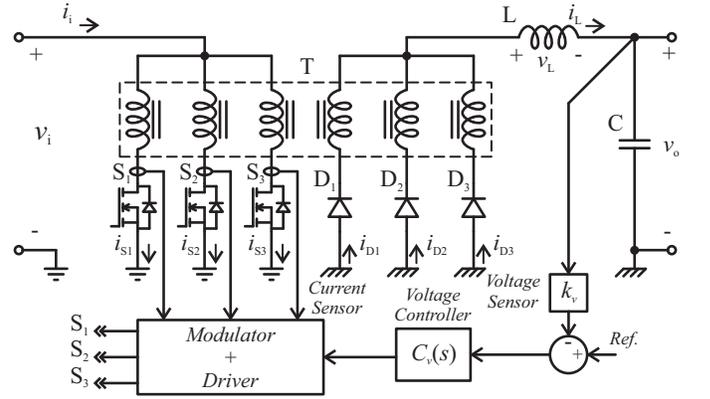


Fig. 6: Converter circuit schematic.

The simulation is performed considering the followed parameters:

$$\begin{aligned} R_{on} &= 0.05 \, \Omega & R_t &= 0.04 \, \Omega & R_L &= 0.03 \, \Omega & R_o &= 4.6 \, \Omega \\ \% \Delta V_o &= 0.2\% & \% \Delta I_L &= 20\% & \zeta &\geq 0.4 & V_F &= 0.8 \, \text{V} \\ N_1/N_2 &= 1 & V_i &= 150 \sim 120 \, \text{V} & V_o &= 48 \, \text{V} & f_s &= 35 \, \text{kHz} \end{aligned}$$

The range of duty cycle is defined by (13).

$$0.220 \leq D \leq 0.275$$

The inductance and capacitance of filter are defined by (16) and (17)

$$L = 74.4 \, \mu\text{H}$$

$$C = 25.8 \, \mu\text{F}$$

From (19) the equivalent resistance results in

$$R_{eq} \geq 0.16\sqrt{3.4}R_o \approx 0.295R_o = 1.359 \, \Omega$$

Thus, gain of current sensor is

$$k_i = \frac{R_{eq} - R_C - R_L}{K_C} = \frac{1.359 - 0.029 - 0.03}{179} \approx 7.3 \cdot 10^{-3}$$

A. Step response with inner loop

Fig. 7 shown step response of converter with current loop and without current loop.

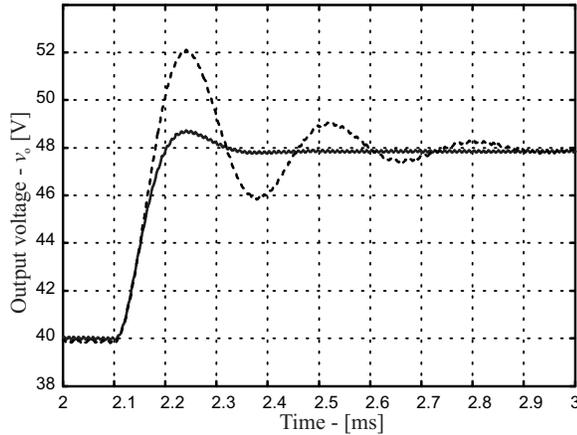


Fig. 7: Step response with inner loop (solid) and without inner loop (dashed).

B. Step response with inner loop and outer loop

Fig. 8 presents the results for step-response at closed loop with and without current loop, it means using only the voltage loop.

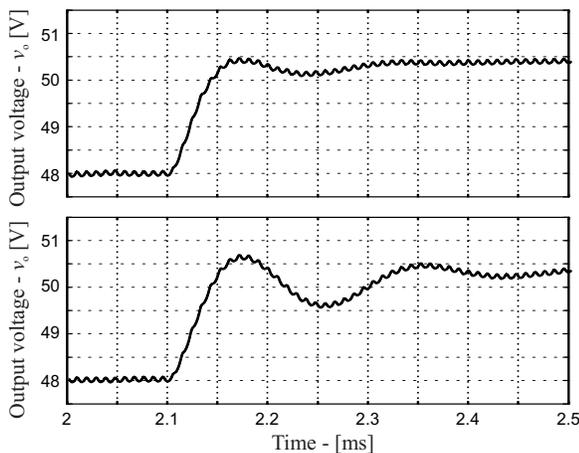


Fig. 8: Above step response with both control loops, and below only voltage loop.

C. Proposal of modulation

Regarding this issue, this proposal reaches an original modulation technique where the integrator blocks, presented in Fig. 5, are essential to promote the waveform in Fig. 9, clearly different of classical modulation of Fig. 10.

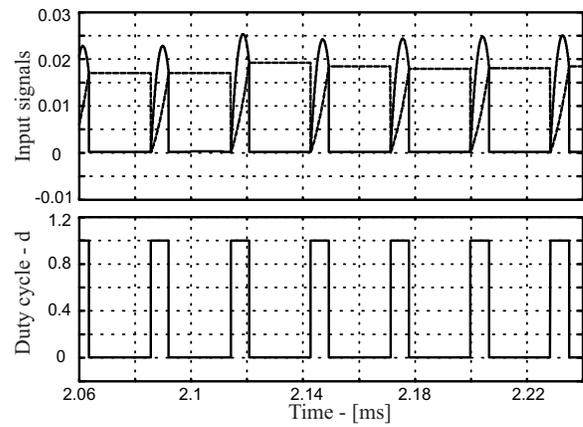


Fig. 9: Comparator and modulation of proposal.

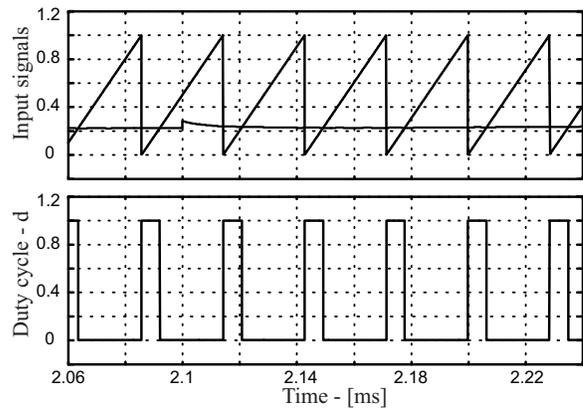


Fig. 10: Comparator and modulation of classical method.

D. Transformer saturation

In order to obtain a realistic behavior for magnetic devices, the simulation was implemented with saturable inductors for three-phase transformer, and B-H curve shown in Fig. 11.

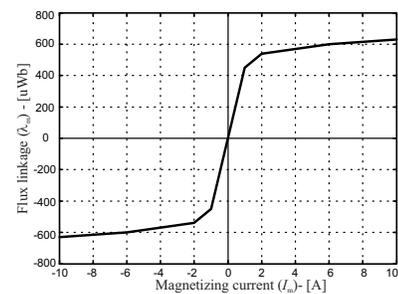


Fig. 11: Saturation curve of transformer.

These saturable inductors and their interaction into the converter were tested through an unbalance performance considering 1 % of difference at the duty cycle in switch S1 which is represented by 1.8 V in series with S1. This assumption promoted an almost saturation condition for transformer and details are shown at Fig. 12 with inner current loop control, and Fig. 13 without inner loop control.

Fig. 12 presents on the upper the output voltage control

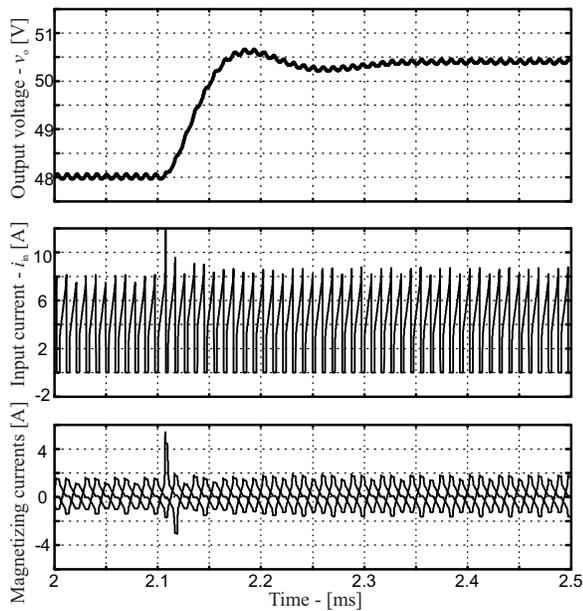


Fig. 12: Step response, input current and magnetizing current with inner current loop.

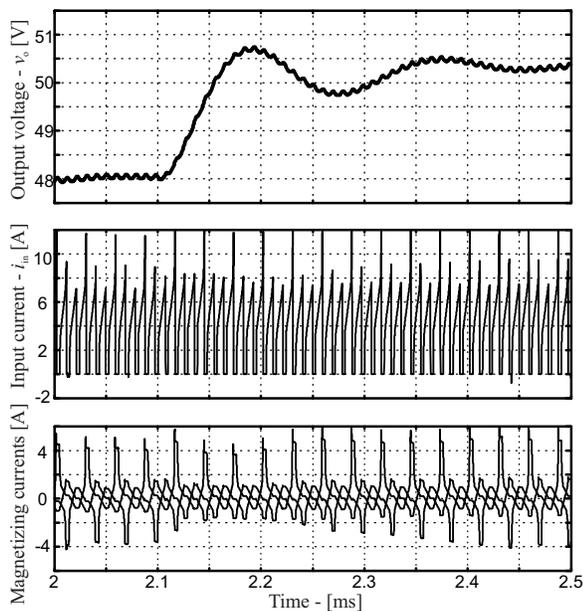


Fig. 13: Step response, input current and magnetizing current without inner current loop.

action for step and input current. Regarding Fig. 13, under presents the modulation voltages for each control condition.

VII. CONCLUSION

In this paper were presented the modeling and control of three-phase push-pull dc-dc converter. The control system is compound by an inner current loop and an outer voltage loop, where the control at power transistors by an inner current control loop allows the current balance per phase of transformer avoiding core saturation, as well as, this inner current control loop is capable to introduces a protection against short-circuit

fault. Moreover, it was presented a non-classic modulation, based at non-linear comparison of transistor currents and duty cycle.

REFERENCES

- [1] J.-M. Kwon, E.-H. Kim, B.-H. Kwon, and K.-H. Nam, "High-efficiency fuel cell power conditioning system with input current ripple reduction" in *IEEE Transactions on Ind. Electronics*, Vol. 56, no. 43, pp. 826-834, Mar. 2009.
- [2] M. Mohr, W. T. Franke, B. Wittig, and F. W. Fuchs, "Converter systems for fuel cells in the medium power range A comparative study" in *IEEE Transactions on Ind. Electronics*, Vol. 57, no. 6, pp. 2024-2032, Jun. 2010.
- [3] H. R. E. Larico, and I. Barbi, "Three-Phase Push-Pull DC-DC Converter: Analysis, Design, and Experimentation" in *IEEE Transactions on Industrial Electronics*, Vol. 59, no. 12, pp. 4629-4636, Dec. 2012.
- [4] K.M. Smedley, and S.Cuk, "One-Cycle Control of Switching Converters" in *IEEE Transactions on Power Electronics*, Vol. 10, no. 6, pp. 625-633, Nov. 1995.
- [5] M. L. Heldwein, and J. W. Kolar, "Light Load Stability Improvement for Single-Phase Boost PFC Rectifier Using Input Current Self-Control Technique" in *Power Electronics Conference (COBEP), 2011 Brazilian*, pp. 61-67, Sept. 2011.