EXTENSION OF THE OPERATING REGION OF A NINE-LEVEL ASYMMETRICAL FLYING CAPACITOR INVERTER

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***Abstract* – This paper presents methods to extend the operating range of a nine-level asymmetrical flying capacitor inverter. The asymmetrical operation is proposed to increase the number of output levels for the same number of semiconductors. A dissipative circuit is analyzed to overcome the converter unbalance problem. The space vector modulation is also verified, replacing the uncontrollable vector by controllable ones. Simulation and experimental results are included to demonstrate the performance of the inverter.**

***Keywords* – Asymmetrical inverter, Flying capacitor, Multilevel converter, Voltage regulation.**

I. INTRODUCTION

Multilevel converters have been used in many applications in the last years due to their capacity to operate with high voltage levels employing low voltage semiconductors [1]–[3]. Additionally, multilevel converters can produce an output waveform with lower harmonic distortion, when compared to classical two level converters [4]–[6].

However, the number of output levels synthesized by a multilevel converter is usually proportional to its number of switches. Therefore, several topologies have been introduced in the last years, with the aim of reducing the number of switches and establishing the best cost-benefit ratio for different applications.

In this sense, an alternative to synthesize a higher number of levels without increasing the number of components is the use of asymmetrical multilevel converters. However, the asymmetric operation has a greater complexity, since it employs distinct values for the dc voltage sources and/or capacitor voltages [7], [8]. Among several topologies, the flying capacitor multilevel converter is specially interesting for asymmetrical operation, since it presents redundant states, which can synthesize the same output levels with different effects for the flying capacitors [9], [10].

The topology proposed in [11] consists of a nine-level asymmetrical single-phase full-bridge flying capacitor converter under distinct flying capacitor voltages. For this configuration, the number of redundant states is not enough to perform the voltage balance of the flying capacitors for a certain range of load angles and amplitude modulation indexes. In order to overcome this problem, this paper presents alternatives to increase the operational range of a nine-level asymmetrical flying capacitor topology. A circuit configuration with a discharging resistor is explored to maintain the converter voltages balance. An alternative space vector modulation strategy is also addressed, gradually replacing the uncontrollable vector by an arrangement of controllable vectors.

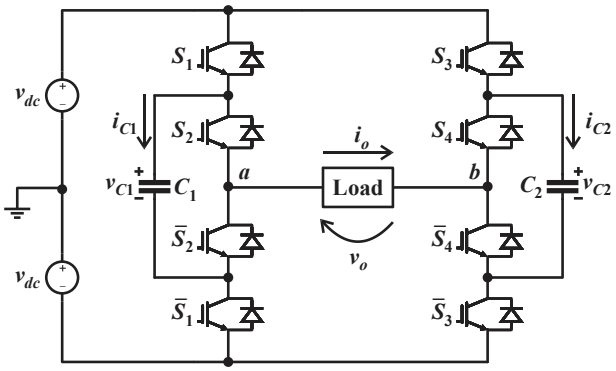

Fig. 1. Inverter topology.

This paper is organized as follows: Section II describes the asymmetrical topology. Section III performs an analysis of the flying capacitor voltage balance problem. Some methods to overcome this problem are proposed in Section IV. Finally, some simulation and experimental results are included in section V to verify the operation of the asymmetrical flying capacitor inverter with the proposed solutions.

II. DESCRIPTION OF THE TOPOLOGY

The single-phase full-bridge topology under study is shown in Figure 1. Each leg of the flying capacitor converter is composed of a capacitor and four active switches. A flying capacitor converter leg can generate up to four different voltage levels, resulting in sixteen possible combinations for the output voltage of the converter in Figure 1. Therefore, the large number of redundant states of this topology allows the balance of the flying capacitors and a larger flexibility in the control strategies.

Considering v_{dc} = 1 pu, the classical symmetrical topology is obtained adopting v_{C1} = v_{C2} = 1 pu. In this case, all the semiconductors are subjected to the same voltage levels and the output voltage presents up to five levels. For this case, the phase-shift modulation is specially interesting. The adoption of this modulation ensures that the flying capacitors operate in a process called natural balancing [12].

For symmetrical multilevel converters, the number of output voltage levels is proportional to the number of semiconductors of the circuit. On the other hand,

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TABLE I
Capacitors voltages v_{C1} and v_{C2} as a function of the number of levels m

m	v_{C1} (pu)	v_{C2} (pu)
5	1	1
7	2/3	2/3
	4/3	2/3
9	1/2	1/2
	1	1/2
11	4/5	2/5
13	2/3	1/3

asymmetrical multilevel converters, in which at least one semiconductor device is subjected to a distinct blocking voltage, are an interesting alternative since they can increase the number of output levels without increasing the number of components of the converter.

Flying capacitor converters are specially attractive for asymmetrical operation, since there are some redundant switching states to synthesize some voltage levels. This feature can be used to provide the balance of the flying capacitors. Depending on the chosen values for the flying capacitor voltages v_{C1} and v_{C2}, different voltage levels can be synthesized, increasing the number of levels of the converter. Some of the possible combinations for the normalized capacitor voltages in function of the number of levels are given in Table I, for equally spaced output levels.

As a result, depending on the capacitor voltages values, semiconductor blocking voltages are different. For example, in the symmetrical topology, all the semiconductors are submitted to the same voltage levels. Among the asymmetrical configurations given in Table I, the nine-level topology with v_{C1} = 1 pu and v_{C2} = 1/2 pu is specially interesting, since the number of levels is increased to nine and one of the converter legs maintains the symmetrical feature. Therefore, this capacitors voltages configuration will be used hereinafter.

III. VOLTAGE BALANCE OF THE FLYING CAPACITORS

It is imperious that the flying capacitors voltages remain regulated under their nominal values for the correct operation of the converter. For asymmetric flying capacitor converters, the phase-shift modulation is no longer adequate for the flying capacitors balance, since there are fewer redundant states compared to the symmetrical topology.

On the other hand, the space vector modulation is specially interesting for this topology, as the desired output voltage levels ($v_{o,ref}$) can be synthesized by algebraic equations that can define the duty cycles of the semiconductors. Therefore, applying the space vector modulation concept for the nine-level flying capacitor topology one can observe four positive (v_{p4}, v_{p3}, v_{p2}, v_{p1}), four negative (v_{n4}, v_{n3}, v_{n2}, v_{n1}) and one zero (v_0) vectors, originating eight different sectors, as shown in Figure 2, considering v_{dc} = 1 pu. So, after the sector determination of the reference voltage, its average value can be synthesized by the use of the two nearest vectors to the reference voltage, in one switching period T_S.

Without loss of generality, only the positive vectors are analyzed for the voltage balance problem, since positive and negative vectors are symmetrical. Based on this affirmation,

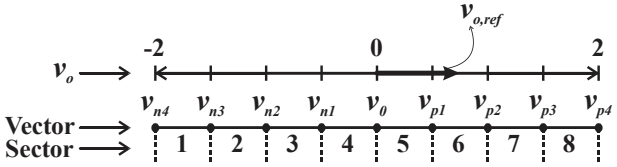

Fig. 2. Output voltage space for m = 9.

TABLE II
Impact of the positive vectors on the flying capacitors voltages, considering $i_o > 0$, m = 9, v_{C1} = 1 and v_{C2} = 1/2

Vector	State	(v_a, v_b) (pu)	C_1	C_2	v_o (pu)
v_0	v_0^1	(-1,-1)	—	—	0
	v_0^2	(1,1)	—	—	
v_{p1}	v_{p1}^1	(1-v_{C1},v_{C2}-1)	↑	↑	1/2
	v_{p1}^2	(v_{C1}-1,v_{C2}-1)	↓	↑	
	v_{p1}^3	(1,1-v_{C2})	—	↓	
v_{p2}	v_{p2}^1	(1-v_{C1},-1)	↑	—	1
	v_{p2}^2	(v_{C1}-1,-1)	↓	—	
v_{p3}		(1,v_{C2}-1)	—	↑	3/2
v_{p4}		(1,-1)	—	—	2

↑ (charging), ↓ (discharging), — (unchanged)

the positive vectors and their contribution to the flying capacitors voltages are presented in Table II.

Although the vector v_0 has two redundant states (v_0^1, v_0^2), it does not affect the flying capacitors currents. On the other hand, vector v_{p1} has three redundant states (v_{p1}^1, v_{p1}^2, v_{p1}^3) and vector v_{p2} has two redundant states (v_{p2}^1, v_{p2}^2). Vector v_{p3} does not have any redundant state and affects the current in the capacitor C_2. Finally, vector v_{p4} does not affect the current in both flying capacitors.

One can verify from Table II that the flying capacitor C_1 does not have problems regarding voltage balance, since it is possible to eliminate its low frequency ripple by maintaining its average current contribution at zero [11]. On the other hand, the voltage balance of capacitor C_2 presents some peculiarities. The main source of unbalance for capacitor C_2 is the use of the vector v_{p3}, since it affects the capacitor current and does not have any redundant state. Therefore, the capacitor C_2 voltage is not controllable in the sectors 7 and 8 and this capacitor always tends to charge in these sectors. Assuming that the reference voltage is located in sector 8, the vectors v_{p3} and v_{p4} are used to synthesize the output voltage. Since the vector v_{p4} does not have any influence on the capacitor C_2 current, the average current on capacitor C_2, in a switching period, $\overline{i_{C2}}$ is only affected by the vector v_{p3}, as given by:

$$\overline{i_{C2}} = i_o d_{p3}, \tag{1}$$

where i_o is the instantaneous value of the output current and d_{p3} is the duty cycle associated to the vector v_{p3}.

For the sector 7, the vectors v_{p2} and v_{p3} are used, resulting in the same value obtained in (1). On the other hand, the vectors v_{p1} and v_{p2} are used in the case the reference voltage is located in sector 6. In this sector there is a certain degree of freedom for the voltage balance of the capacitor C_2, since there are three redundant states associated to v_{p1}. Therefore, the

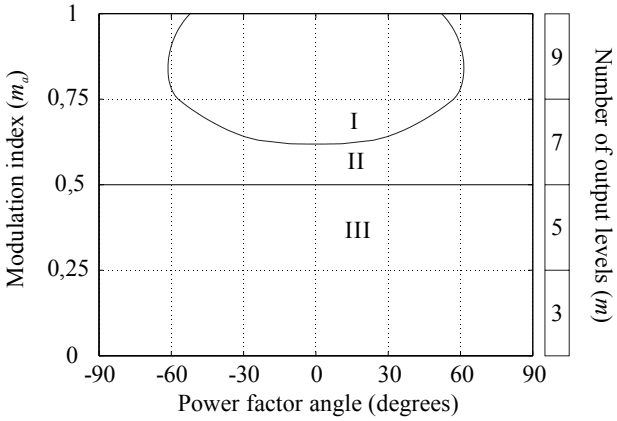

Fig. 3. Space solution where is possible to make the voltage balance on capacitor C_2.

average value of the capacitor current can be controlled in this sector using three redundant states, so that:

$$\overline{i_{C2}} = |i_o| d_{p1}\delta, \qquad -1 \le \delta \le 1, \tag{2}$$

where the variable d_{p1} is the duty cycle associated to the vector v_{p1} and δ is the control variable, which is used for the average current control of the capacitor C_2 in a switching period. For the sector 5, the vectors v_0 and v_{p1} are used and the average value of the current is also given by (2). Thus, it is possible to conclude that the average value of the capacitor C_2 current is composed of two parts: a controllable (sectors 5 and 6) and an uncontrollable one (sectors 7 and 8).

Thereby, to obtain the operation region of the converter (where the controllable part must be capable to compensate the uncontrollable part), the maximum value of the capacitor C_2 charge at sectors 5 and 6 must be higher than the charge at sectors 7 and 8. Based on this concept, the operating regions of the nine-level flying capacitor inverter are shown in Figure 3 [11]. Regions II and III present the controllable operating regions, where the voltage balance is practicable. In region III, the low-frequency voltage ripple on capacitor C_2 can also be eliminated, since the vector v_{p3} is not used. On the contrary, according to Figure 3, the voltage balance is not possible for region I. Consequently, the capacitor C_2 voltage will diverge from its nominal value.

IV. EXTENSION OF THE CONVERTER OPERATING REGION

As can be observed in Figure 3, the asymmetrical nine-level flying capacitor converter under study in this paper presents a limited operating region. Therefore, this section presents some solutions in order to overcome this problem.

A. Vector v_{p3} removal

The vector v_{p3} is the main source of unbalance for the operation of the converter. This occurs because this vector affects the current on the flying capacitor C_2, but has no redundant states.

Figure 4 shows the total energy E_{p3} processed by the vector v_{p3}, and the total energy E_{p1} processed by the vector v_{p1}, in a

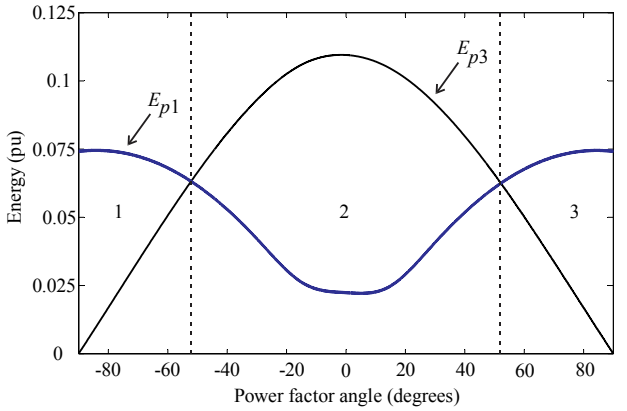

Fig. 4. Total energy produced by the vector v_{p1} and v_{p3}, considering $\delta = 1$, an unitary modulation index, $v_{dc} = 100$ V and output peak current equal to 10 A.

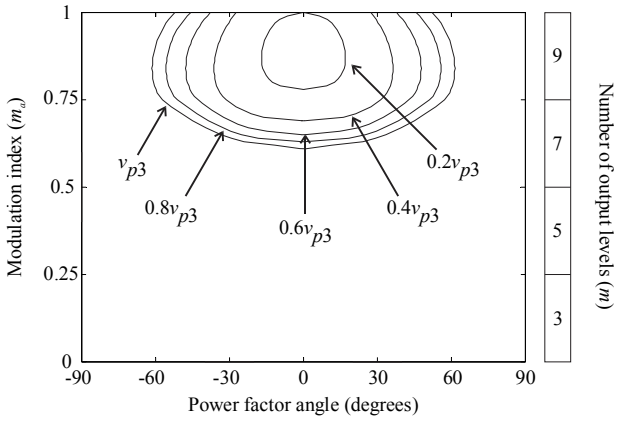

Fig. 5. Space solution reducing the duty cycle of the vector v_{p3}.

fundamental period, considering $\delta = 1$, an unitary modulation index, $v_{dc} = 100$ V and output peak current equal to 10 A. It is possible to notice from Table II that the vector v_{p3} always increases the capacitor voltage, independent of the load angle. On the other hand, the vector v_{p1} can either charge or discharge the flying capacitor C_2, depending on the circuit needs. Therefore, the voltage balance can be obtained on regions 1 and 3, since the maximum energy associated to the controllable vector is greater than the energy associated to the uncontrollable vector.

Since it is possible to synthesize the average value of the vector v_{p3} using the vectors v_{p2} and v_{p4}, in a switching period, it is possible to decrease the duty cycle associated to the vector v_{p3} to extend the operating region of the multilevel converter. For example, Figure 5 presents a new space solution for the operation region of the converter, reducing the duty cycle associated to the vector v_{p3}. It is possible to notice that, for each decrease in the use of this vector, the functional area of the converter increases, until the case which $v_{p3} = 0$, when the converter can operate for any load power and amplitude modulation index. On the other hand, by decreasing the application time of the vector v_{p3}, the output voltage level tends to distort and the total harmonic distortion and the weighted total harmonic distortion in the output voltage will increase, as stated in Figure 6 and in Figure 7.

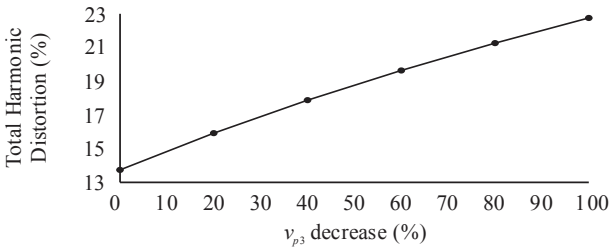

Fig. 6. Effect of the reduction of the vector v_{p3} on the converter total harmonic distortion.

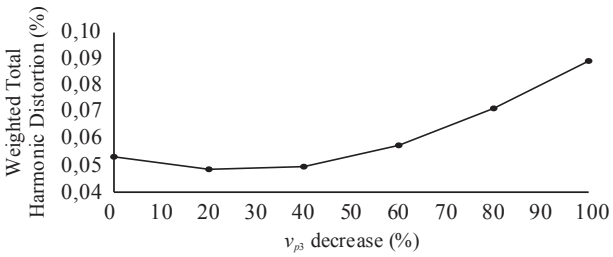

Fig. 7. Effect of the reduction of the vector v_{p3} on the converter weighted total harmonic distortion.

B. Inclusion of a switched resistor

The inclusion of a switched resistor in parallel with the capacitor is another option to extend the operating region of the inverter, as illustrated on Figure 8. From Figure 4, it is possible to notice that the maximum value of the energy in the capacitor C_2, during a fundamental period T, occurs when the load angle is zero. Based on this affirmation, it is possible to calculate the value of the energy that the resistor must dissipate for this point, as given by:

$$\frac{1}{T}\int_0^T v_{C2}(t)\,i_{C2}(t)\,dt = \frac{1}{T}\int_0^T v_R(t)\,i_R(t)\,dt\,, \qquad (3)$$

where $v_R(t)$ and $i_R(t)$ are the voltage and the current in the dissipation resistor, over a period of time, respectively.

Since the energy for load angles different than zero will be always smaller than the dissipation energy of the resistor, the capacitor will always tend to discharge if the resistor switch is turned on during the whole fundamental period. Note that if the output current increases, the energy on capacitor C_2 also increases and the dissipation energy of the resistor must be recalculated.

V. RESULTS

A. Simulation results

Simulation results were obtained to verify the operation of the proposed inverter. The parameters adopted for the inverter are described in Table III. A digital proportional- integral (PI) controller was employed to obtain the control variable δ to perform the voltage balance of the capacitor C_2. Two resistive-inductive loads were tested to validate the inverter operation region: low power factor (load 1) and high power factor (load 2), as shown in Table III.

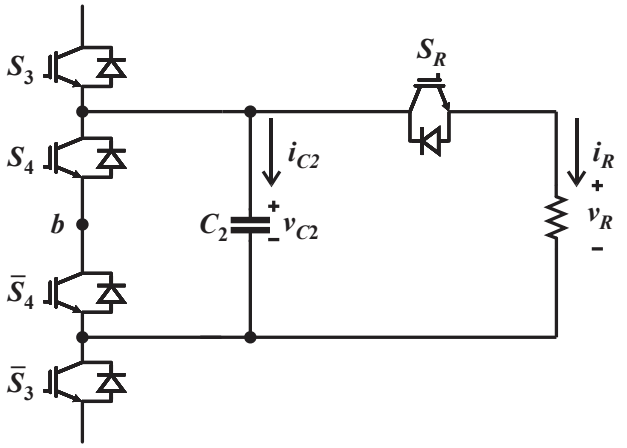

Fig. 8. Inclusion of a switched resistor.

A simulation result for the converter operating with unit modulation index m_a, using the load 1, is presented in Figure 9. One can verify the nine levels generated at the inverter output and the voltage in the flying capacitors. As expected, the voltage in capacitor C_2 presents some low frequency ripple in this operation point. Moreover, the voltage balance in capacitor C_1 is also achieved with the proposed modulation strategy.

On the other hand, considering the load 2, the voltage balance of the flying capacitor C_2 is achieved for lower values of modulation index, as shown in Figure 10. In this result, a modulation index step is performed at 850 ms ($m_a = 0.5 \rightarrow m_a = 1.0$), where it is possible to verify that the voltage in the capacitor C_2 diverges from its nominal value, since this operation point is inside region I, shown in Figure 3.

Figure 11 presents the output voltage if the duty cycle set to vector v_{p3} is zero, for the load 2, for a high power factor. Since there is no non-operational area for this case, the voltage in capacitor C_2 remains balanced. Even so, a seven level output voltage is still guaranteed.

Lastly, the output voltage for the case which a switched resistor of 14.3 Ω is placed in the circuit is shown in Figure 12, in order to discharge the exceeding energy 0.72 J of the capacitor C_2. In this case, the resistor consumes 6.32 % of the total average power of the converter, in a fundamental period. This resistor is only inserted on the circuit when the vector v_{p4} is applied, since the capacitor is in an open circuit condition for this vector. The figure also presents the capacitor C_2 voltage, which can be controlled by the insertion of the dissipation resistor.

TABLE III
Inverter parameters

Parameter	Value
DC bus voltage (v_{dc})	100 V
Voltage in capacitor C_1	100 V
Voltage in capacitor C_2	50 V
Capacitor C_1	1 mF
Capacitor C_2	4.7 mF
Fundamental frequency (f_1)	50 Hz
Switching frequency (f_s)	2.6 kHz
Load 1	1.8 + 14.13j Ω
Load 2	31.4 + 14.13j Ω

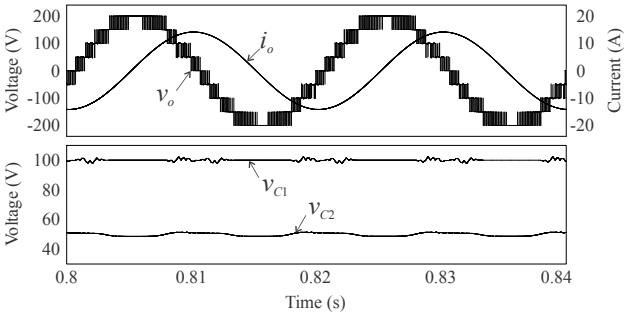

Fig. 9. Simulation results for load 1 and $m_a = 1$.

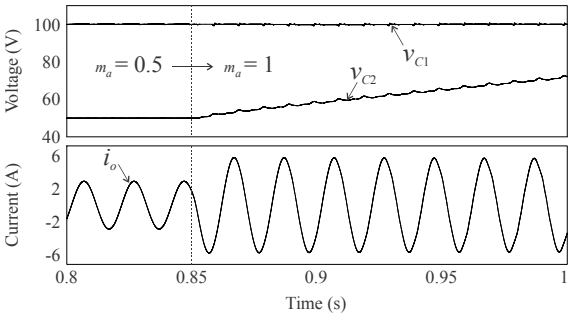

Fig. 10. Simulation results for modulation index step (load 2).

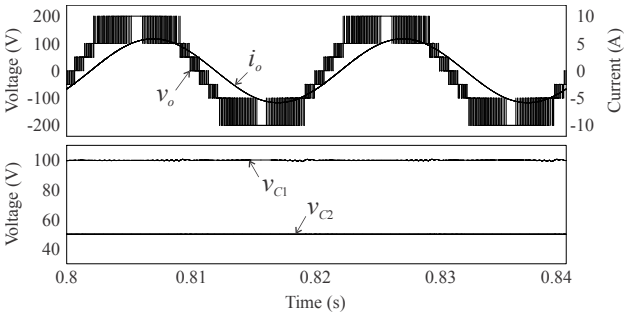

Fig 11. Simulation results if the duty cycle of the vector v_{p3} is zero, for load 2.

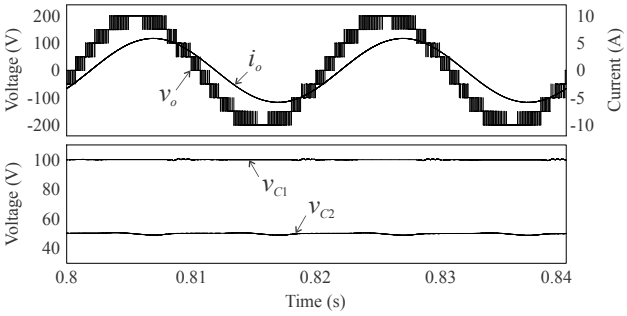

Fig. 12. Simulation results for the inclusion of a switched resistor in parallel with the capacitor C_2, for load 2.

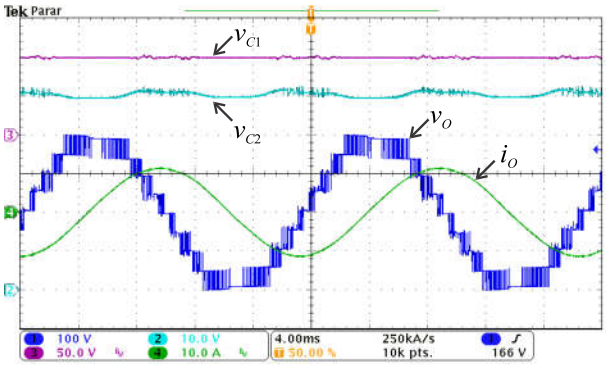

Fig. 13. Experimental results for load 1 and $m_a = 1$.

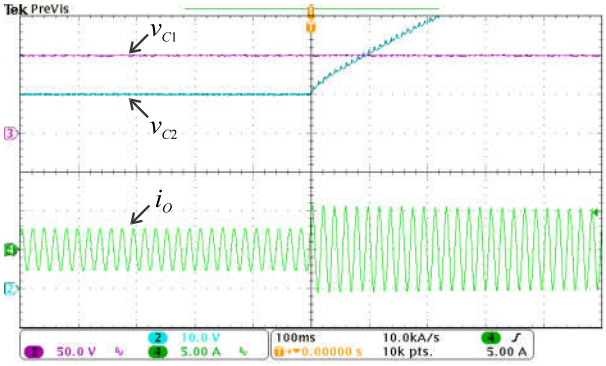

Fig. 14. Experimental result for modulation index step (load 2).

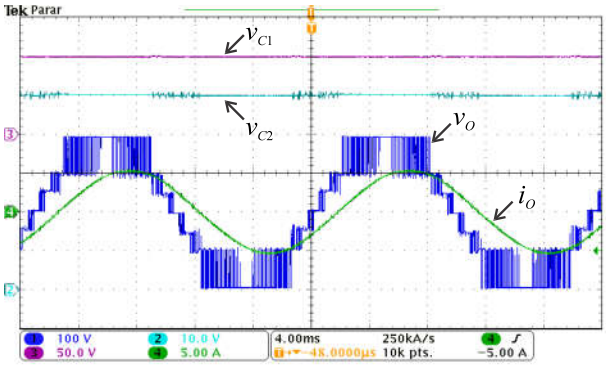

Fig. 15. Experimental result if duty cycle of the vector v_{p3} is zero, for load 2.

B. Experimental results

Experimental results for $m_a = 1$ using load 1 are shown in Figure 13. It is possible to verify the nine-level voltage generated in the inverter output as well as the balanced voltages on the flying capacitors C_1 and C_2. The voltage v_{C1} is free of low-frequency ripple while the voltage v_{C2} has low-frequency components originated from the necessity of voltage balance strategy.

The inverter voltage balance capability can be verified in Figure 14, where a modulation index step was performed. Considering the load 2, the voltage balance is achieved only for low values of modulation index. Figure 15 presents the

output waveforms setting $d_{p3} = 0$, for the load 2. The voltages on the flying capacitors remain balanced even for high power factors for this modulation strategy.

VI. CONCLUSION

This work presented some solutions to extend the operating region of a nine-level flying capacitor converter. The main advantage of the asymmetrical operation is the increase in the number of output levels without increasing the number of semiconductors. This was achieved by adopting unconventional values for the capacitors voltages. The problem of the voltage balance of the flying capacitors was addressed from the space vector modulation concept, demonstrating that the voltage regulation of the flying capacitors could be only achieved for limited load power factors and amplitude modulation index points. In order to overcome this problem, some solutions were presented on this paper, either modifying the application time of some vectors or including dissipating resistors. In addition, these solutions can be used in a hybrid alternative to reduce the negative impact in voltage distortion and efficiency.

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