Evaluation of the Hybrid Four-level Converter Employing Half-Bridge Modules for Two Different Modulation Schemes

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***Abstract*—A novel hybrid three-phase multilevel converter is proposed for medium-voltage applications. The converter employs a conventional three-phase voltage source inverter (VSI) linking series connected half-bridge modules at each phase. With the proposed connection, a large portion of energy can be processed by the VSI without the need for insulation or by employing a single transformer, while smaller power shares are processed within the half-bridge modules. Thus, the requirements for galvanically insulated dc sources are reduced. Modularity is naturally achieved. A modulation scheme for a four-level version is proposed and analyzed in detail. This scheme allows unidirectional power flow in all dc sources and, consequently enables diode bridges to be employed in the rectification input stage for unidirectional applications.**

I. Introduction

Multilevel topologies are a major part of medium voltage power electronics equipment and research in this field has led to various solutions [2]–[9]. Hybrid multilevel topologies based on the series connection of three-phase VSI or NPC with full-bridge modules (H3phCFB) have been proposed [5], [8], [10]–[12] as alternative to the Cascaded Full-Bridge (CFB) converters [4], [13]. Following the hybridization approach a multilevel converter topology has been introduced in [1]. This hybrid topology (H3phCHB) utilizes a three-phase inverter (cf. Fig. 1) with its output terminals connected in series to a pair, or multiple pairs (cascade), of half-bridge converters connected with inverse polarity.

The demand for medium voltage converters grows based on the lowering costs for the technology and the necessity of areas such as high power drives, renewable energy generation, power quality and naval propulsion. In this context, the search for solutions in this field becomes important as does the need for a careful evaluation of the proposed topologies. This work aims at a thorough evaluation of the four-level converter shown in (cf. Fig. 1) [1] regarding two possible modulation strategies. The first strategy is based on the switching of all turn-off devices at the switching frequency, while in the second modulation strategy only the devices of the half-bridge converters operate at the switching frequency. In the second strategy, the semiconductors of the VSI switch at the fundamental output frequency or do not switch at all for low modulation indexes. These modulation strategies are explained in section II. The computation of current stresses, conduction and switching losses is introduced in section III. Finally a comparison of both schemes regarding current efforts and losses is performed and experimental results are presented.

II. Modulation Strategies

Two modulation schemes for the four-level H3phCHB are presented in this section. The first scheme is based on conventional carrier based PWM signals for all switches, here named CONVENTIONAL modulation. The PWM signals generation logic for this scheme is depicted in Fig. 2(b). In the second modulation scheme, named HYBRID modulation (described in details in [1]), the semiconductors of the three-phase VSI switch at low frequency in order to reduce the VSI switching losses. Thus, only the half-bridge modules switch at the switching frequency. Switches S_{jo} and $S_{jo'}$, with $o = A, B, C$ and $j = 1, 2, 3$, are switched in a complementary way. This modulation scheme is further divided into two operation modes *LM* and *HM* depending on the modulation index M and described in the following:

- $\mathbf{0 \leq M \leq 0.5}$ (*LM*): the VSI has all switches either clamped to the positive or the negative rail. The clamping can be changed at every modulation cycle in order to balance the losses at all semiconductors. The half-bridge modules process all the active power transferred to the load.
- $\mathbf{M > 0.5}$ (*HM*): each VSI leg switches a single time per modulation period (cf. Fig. 2(c)) and the half-bridge modules handle a smaller power share.

III. Semiconductor Current Efforts

Based on the modulation strategy presented in section II the methodology for the computation of current efforts in all semiconductors is introduced in the following. The considerations are made for a phase-leg comprising two half-bridge modules and a VSI leg, exemplarily for phase A. Furthermore, the modulation index is limited to $M > 2/(3\sqrt{3})$ and only the HYBRID modulation derivation is shown for the sake of brevity. The same methodology can be applied for the other modulation schemes.

Neglecting the output current ripple, possible high frequency harmonic contents and assuming balanced loads, the phase current is defined as $i_A(\varphi) = I_p \sin(\varphi - \Phi)$, where Φ is the load phase displacement angle limited from 0 to $+\pi/2$ in the analysis (inductive loads). The angles where the modulating function has its values on the limit between two different carriers are defined with $\theta_M = \arcsin\left(\frac{1}{3M}\right)$.

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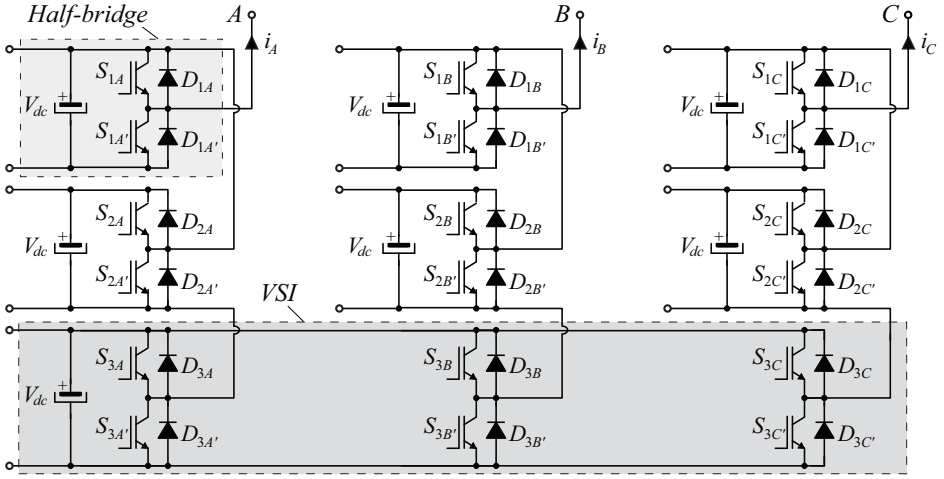


Fig. 1. Circuit schematic of the hybrid four-level converter employing half-bridge modules and a three-phase inverter [1].

Given the modulation pattern *HM*, the duty-cycle for switch S_{1A} is exemplarily given by

$$d_{S1A}(\varphi) = \begin{cases} \frac{1}{2} + \frac{3}{2}M\sin(\varphi) & ;0 \le \varphi \le \theta_M \\ 1 & ;\theta_M \le \varphi \le \pi - \theta_M \\ \frac{1}{2} + \frac{3}{2}M\sin(\varphi) & ;\pi - \theta_M \le \varphi \le \pi \\ 1 & ;\pi \le \varphi \le \pi + \theta_M \\ \frac{3}{2} + \frac{3}{2}M\sin(\varphi) & ;\pi + \theta_M \le \varphi \le 2\pi - \theta_M \\ 1 & ;2\pi - \theta_M \le \varphi \le 2\pi \end{cases}. \tag{1}$$

for switch S_{2A} by

$$d_{S2A}(\varphi) = \begin{cases} 0 & ;0 \le \varphi \le \theta_M \\ -\frac{1}{2} + \frac{3}{2}M\sin(\varphi) & ;\theta_M \le \varphi \le \pi - \theta_M \\ 0 & ;\pi - \theta_M \le \varphi \le \pi \\ \frac{1}{2} + \frac{3}{2}M\sin(\varphi) & ;\pi \le \varphi \le \pi + \theta_M \\ 0 & ;\pi + \theta_M \le \varphi \le 2\pi - \theta_M \\ \frac{1}{2} + \frac{3}{2}M\sin(\varphi) & ;2\pi - \theta_M \le \varphi \le 2\pi \end{cases} \tag{2}$$

and for the VSI switch switch S_{3B} by

$$d_{S3A}(\varphi) = \begin{cases} 1 & ;0 \le \varphi \le \pi \\ 0 & ;\pi \le \varphi \le 2\pi \end{cases}. \tag{3}$$

For the complementary switches, the duty-cycle is generally defined as $d_{SjA'}(\varphi) = 1 - d_{SjA}(\varphi)$, with $j = 1, 2, 3$.

Thus, the average values for the semiconductor currents are computed with

$$I_{SjA,avg} = \frac{1}{2\pi}\int_0^{2\pi} i_o(\varphi) \cdot d_{SjA}(\varphi) d\varphi \tag{4}$$

$$I_{DjA',avg} = \frac{1}{2\pi}\int_0^{2\pi} i_o(\varphi) \cdot d_{SjA'}(\varphi) d\varphi, \tag{5}$$

and the RMS values with

$$I^2_{SjA,rms} = \frac{1}{2\pi}\int_0^{2\pi} d_{SjA}(\varphi) \cdot (i_o(\varphi))^2 d\varphi \tag{6}$$

$$I^2_{DjA',rms} = \frac{1}{2\pi}\int_0^{2\pi} d_{SjA'}(\varphi) \cdot (i_o(\varphi))^2 d\varphi. \tag{7}$$

The integration limits for switches S_{1A} and S_{2A} can be divided into the intervals given in (1). However, a further subdivision is necessary due to the load phase displacement Φ. Therefore, two cases must be analyzed, namely: Case I :$0 < \Phi < \theta_{\mathrm{M}}$ and Case II :$\theta_{\mathrm{M}} < \Phi < \frac{\pi}{2}$. These two cases are irrelevant for the derivations regarding S_{3A} as long as the VSI switches at low frequency. In this case, the average currents across the semiconductors of the three-phase VSI are

$$I_{S3,avg} = I_{S3',avg} = \frac{Ip}{2\pi}\left[1 + \cos(\Phi)\right] \tag{8}$$

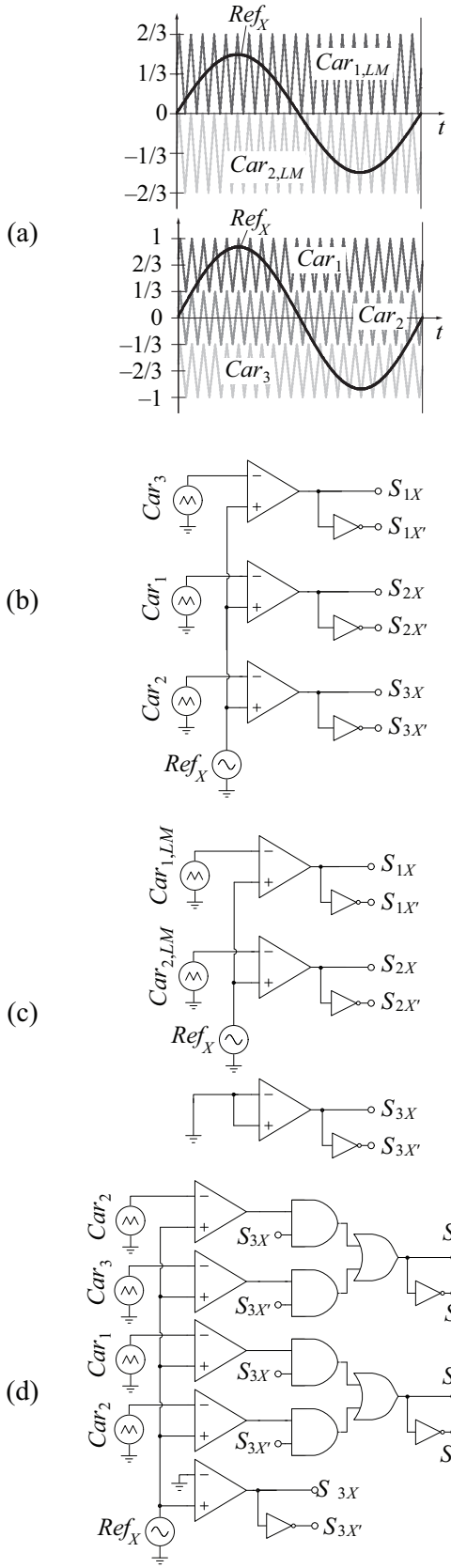
$$I_{D3,avg} = I_{D3',avg} = \frac{Ip}{2\pi}\left[1 - \cos(\Phi)\right], \tag{9}$$

and the RMS values are given by

$$I_{S3,rms} = I_{S3',rms} = \frac{Ip}{2}\sqrt{\frac{\sin(2\Phi)}{2\pi} + 1 - \frac{\Phi}{\pi}} \tag{10}$$

$$I_{D3,rms} = I_{D3',rms} = \frac{Ip}{2}\sqrt{\frac{\Phi - \sin(2\Phi)}{\pi}}. \tag{11}$$

The integration of the local average/rms values of the semiconductors current lead to involved expressions for the devices of the half-bridge modules. However, normalizing the current values by dividing them by the current peak value I_p and plotting against the variations of modulation index M and phase angle ϕ gives insight on the behavior of the currents. This is done in Fig. 3, where Fig. 3(a) and (b) show the current efforts for the switches and Fig. 3(c) and (d) for the anti-parallel diodes. It is noticed that switches S_{jo}



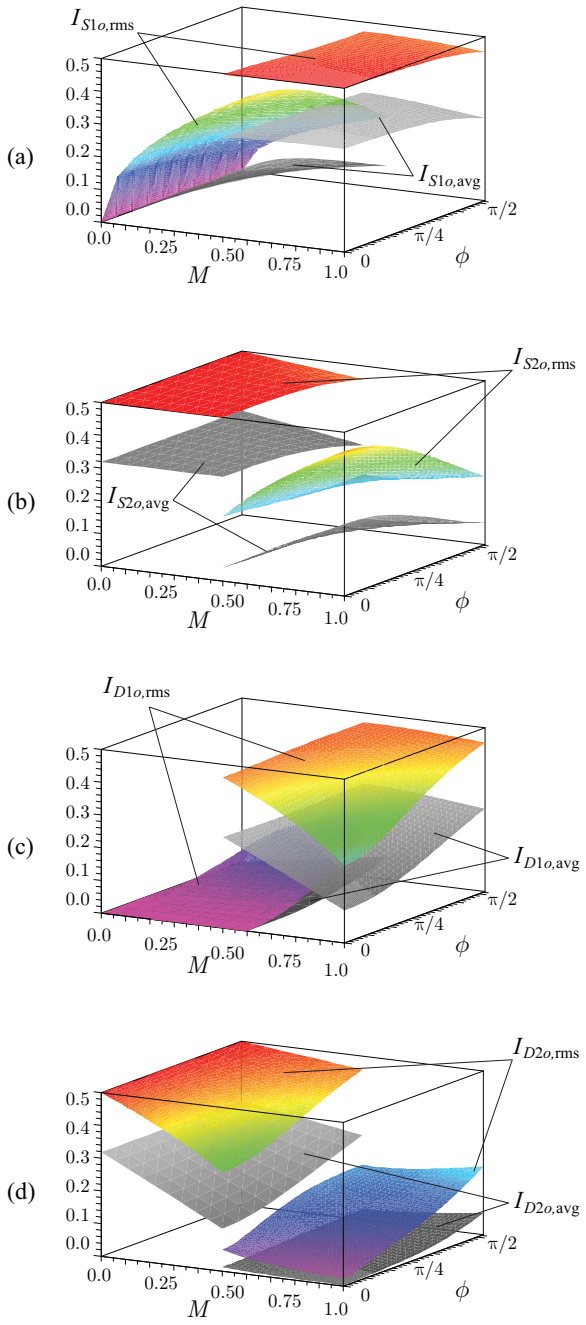


Fig. 2. PWM generation logic for modulation strategies: (a) carrier signals; (b) CONVENTIONAL; (C) HYBRID modulation with *LM* ($M \leq 1/2$), and; (d) HYBRID modulation with *HM* ($M > 1/2$).

Fig. 3. Normalized current ($1/I_p$) efforts in the half-bridge modules semiconductors.

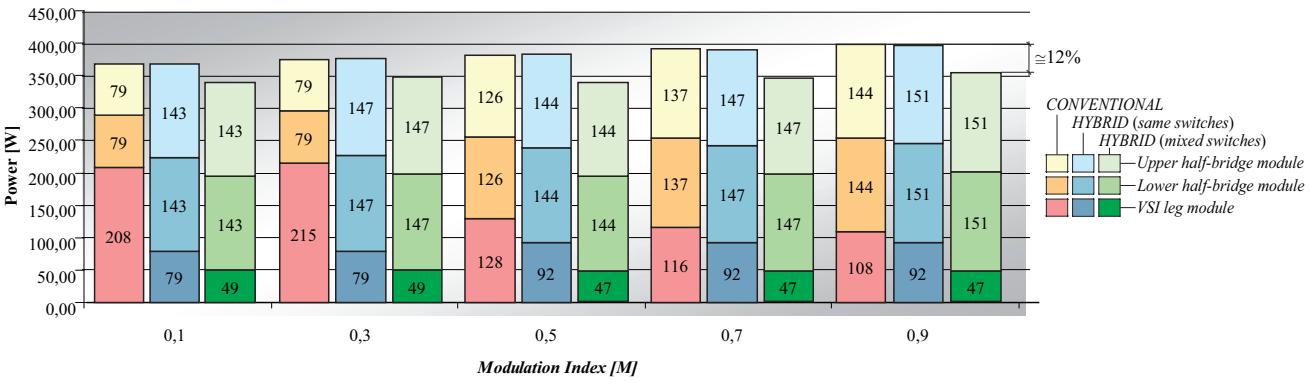


Fig. 4. Comparison of estimated losses and loss distribution for both modulation strategies for a single converter phase-leg comprising two half-bridge modules and a VSI leg. First (yellows) and second (blues) bars are computed with the complete converter based on SKM75GB063D. Third (greens) bar refers to a converter employng low speed IGBTs SKM145GB066D on the VSI module. Conditions: $I_p = 70$ A, $V_{dc} = 400$ V, $f_o = 50$ Hz, $f_s = 20$ kHz and $\Phi = 0°$.

($o = A, B, C$) present higher currents than switches $S_{jo'}$ for higher modulation indexes. On the other hand, diodes D_{jo} present lower currents than diodes $D_{jo'}$ for $M \geq 0.5$. The opposite behaviour is observed for low modulation indexes. Thus, losses are reasonably balanced for a switch comprising an IGBT and its diode, even though the IGBTs, or the diodes, for a half-bridge module can present distinct current demands. The calculations results have been validated for multiple operation points through computational simulation results obtained from the software PSIM. The observed errors have been smaller than 0.5% for all simulation conditions.

A. Losses Comparison

Conduction losses P_{con} are computed with the derived RMS and average current values, so that

$$P_{con} = V_{con} I_{S/D,avg} + r_{con} I^2_{S/D,rms}, \tag{12}$$

where V_{con} is the forward voltage drop of the respective switch S or diode D and r_{con} its resistance.

Following the approach presented in reference [14], the switching loss energy is approximated with a second order polynomial. A further simplification adds the switching loss energy contributions for all switches into only three coefficients κ_0, κ_1 and κ_2, which represent the sum of the coefficients that model the switch turn-on and turn-off losses and the diodes' reverse recovery. The switching loss energy as a function of the switched current is given by

$$W_{sw}(I_{sw}) = \kappa_0 + \kappa_1 I_{sw} + \kappa_2 I^2_{sw}. \tag{13}$$

The total switching losses are

$$P_{sw,tot} = \frac{1}{2\pi} \int_0^{2\pi} f_s \, W_{sw}(i_g) \, d\omega t. \tag{14}$$

In order to properly compare both modulation strategies the inverter conduction and switching losses are computed for an exemplary design. The output current peak is set at 70 A, with a dc-link voltage of $V_{dc} = 400$ V, $f_o = 50$ Hz, $f_s = 20$ kHz and a null load displacement angle. In this context, the output power varies with the modulation index. Fig. 4 shows the comparison results for a four-level converter phase-leg. In this graph, the two first bars for each modulation index represent the losses for the converter when employing IGBT model SKM75GB063D for the switches in, both, half-bridge and VSI modules. It is observed that the total losses are very similar for all modulation indexes. However, the loss distribution among the half-bridge and VSI modules present large variation. With the CONVENTIONAL modulation the loss distribution for high modulation indexes is more favorable, while it is seen that for $M < 1/3$ the VSI semiconductors are highly overloaded presenting a loss peak much higher than for any other operating condition with the HYBRID modulation. Since the VSI semiconductors switch at low frequency, low speed IGBTs are a better choice for the converter employing the HYBRID modulation. With this, a further design has been performed utilizing IGBT model SKM145GB066D, which is a trench device with much lower forward conduction voltage drop. The losses for this design are shown in the third bar of Fig. 4 and indicate that a total loss reduction around 10% is achieved at all modulation indexes. Thus, reducing cooling efforts and increasing overall efficiency.

IV. Experimental Verification

Experimental verification is carried out in lab prototype based on nine IGBT (Semikron SKM75GB063D) half-bridge modules (cf. Fig. 1). The dc sources are insulated through three-phase transformers with the secondaries connected to diode bridges and electrolytic capacitors. The average dc supply value is around 400 V. The switching frequency is set to 4.08 kHz and the output fundamental voltage is 60 Hz. The hardware has been built to offer safe operation margins and flexibility and, thus, is not optimized for specific operation points. The employed RL load presents $R = 740$ Ω and $L = 111$ mH connected in delta, leading to a current displacement angle around 4°@60 Hz. Both modulation strategies are implemented in a DSP (TMS320F2812) in

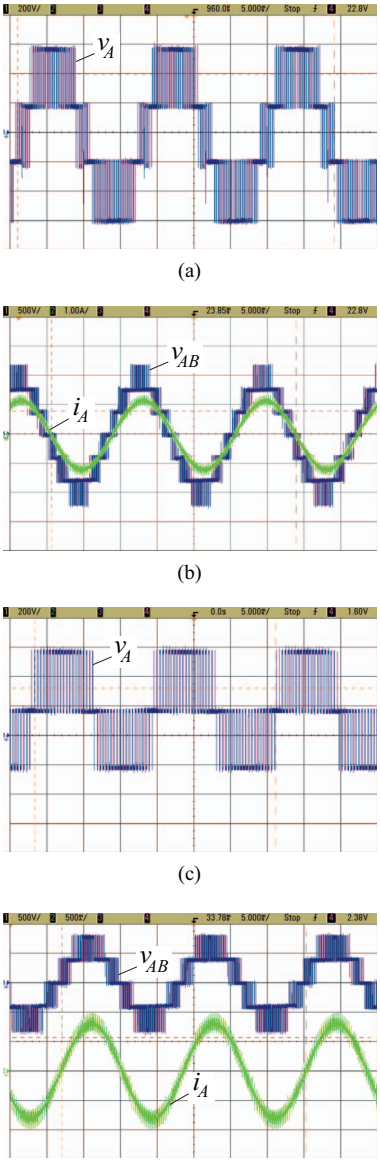


Fig. 5. Experimental results for $f_o \cong 60Hz$ and $f_s \cong 4kHz$: (a) phase voltage v_A for $M = 0.9$ (*HM*); (b) line voltage v_{AB} and phase current i_A for $M = 0.9$ (*HM*)); (C) phase voltage v_A for $M = 0.5$ (*LM*); (b) line voltage v_{AB} and phase current i_A for $M = 0.5$ (*LM*)).

an open-loop scheme. The phase and line voltages for low and high modulation indexes are shown in Fig. 5 for the HYBRID modulation scheme. The line voltage waveforms for the CONVENTIONAL modulation are strictly the same as the shown in Fig. 5.

Measurements displaying different operating conditions, i.e. modulation index and load displacement angle, are displayed in Fig. 6. This figure shows the measured switch and diode currents RMS and average values for the given operating conditions along with the respective waveform.

Fig. 7 shows a comparison between the theoretical analysis based current efforts and experimentally measured values. The

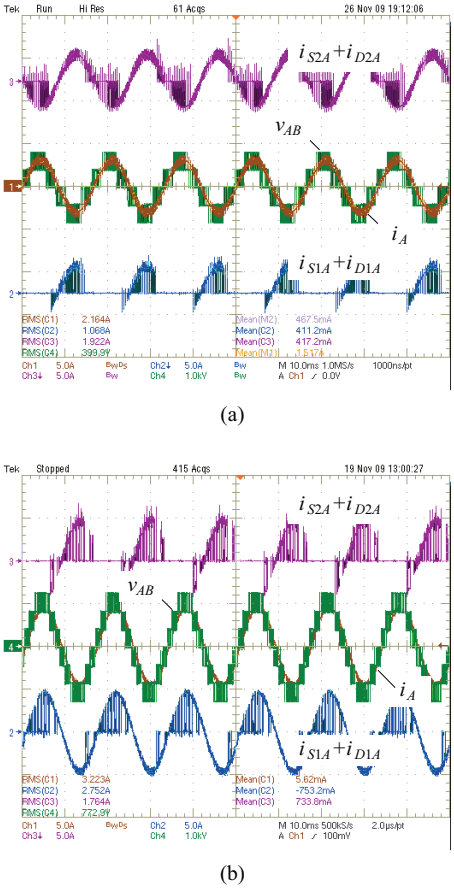


Fig. 6. Experimental results for $f_o \cong 60Hz$ and $f_s \cong 4kHz$: (a) phase voltage v_A for $M = 0.9$ (*HM*); (b) line voltage v_{AB} and phase current i_A for $M = 0.9$ (*HM*)); (C) phase voltage v_A for $M = 0.5$ (*LM*); (b) line voltage v_{AB} and phase current i_A for $M = 0.5$ (*LM*)).

current values are given as fuctions of the load RMS value (100%) for a modulation index $M = 1.0$. The modulation index is varied from $M = 0.1$ up to $M = 1.0$ and three different loads have been tested with phase displacement angles of $\Phi = 10°$, $45°$ and $85°$. The currents have been measured at the power module's input, so that IGBT and diode current are combined accordingly. It is seen that a very good agreement is achieved for all tested conditions, thus, certifying the validity of the performed theoretical analysis.

V. Conclusions

The analysis of the semiconductor efforts and losses oriented to the design of the newly proposed four-level hybrid converter has been performed. The computation of current efforts has been presented, where experimental results based on a built prototype have been shown certifying the validity of the theoretical analysis. It was shown that the proposed hybrid modulation is able to provide better losses distribution among the power semiconductors and to limit the maximum device loss to a lower level when compared to a fully high frequency switched converter. Furthermore, it was shown that

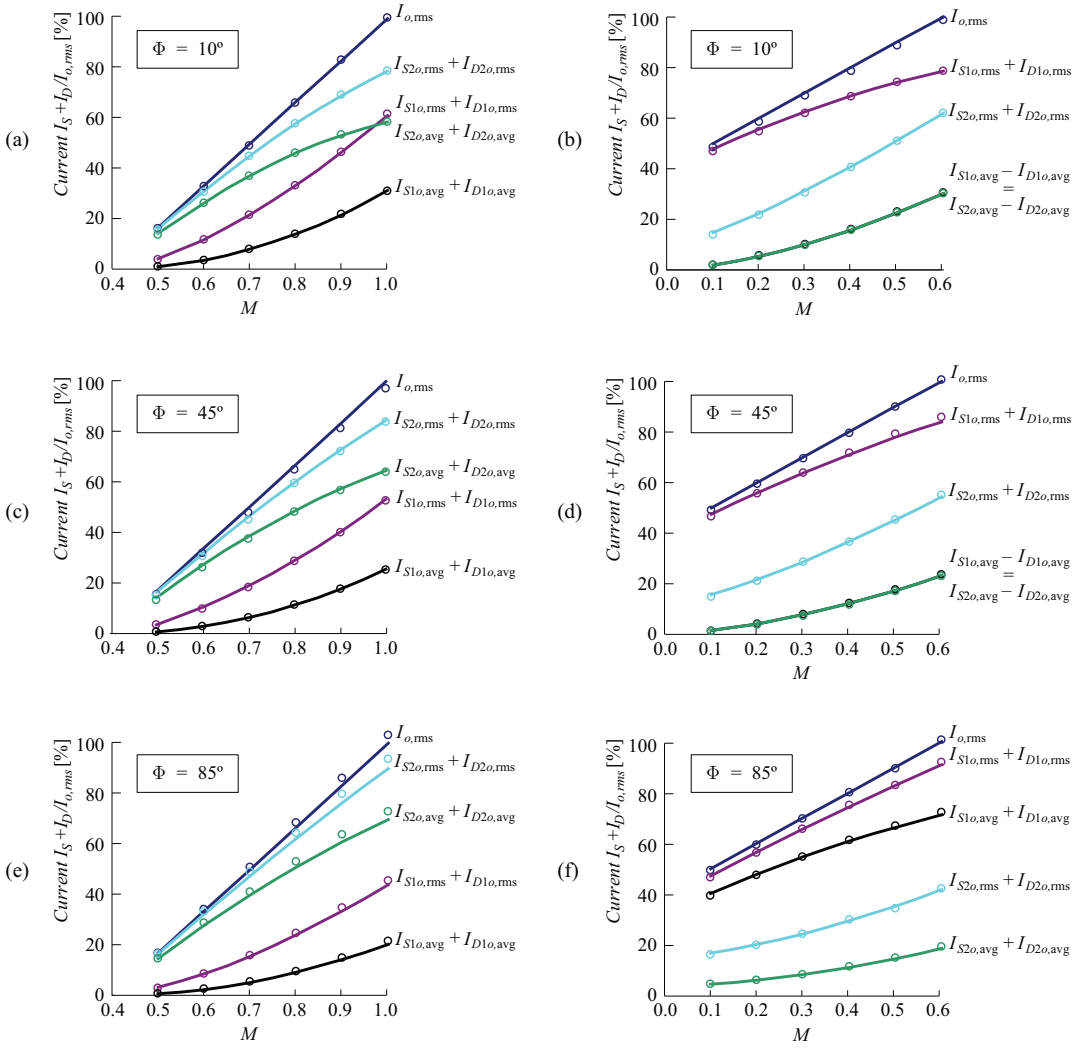


Fig. 7. Comparison between measured and theoretical values for the current efforts across the power semiconductors of the half-bridge module. Current values for: (a) and (b) load displacement angle $\Phi = 10°$; (c) and (d) load displacement angle $\Phi = 45°$; (e) and (f) load displacement angle $\Phi = 85°$.

for the case where the VSI devices are replaced with lower speed and lower forward voltage drop IGBTs, the four-level hybrid converter is able to achieve higher efficiency figures.

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