DIGITAL CONTROL OF A FULL-BRIDGE–FLYBACK ISOLATED CURRENT RECTIFIER WITH POWER FACTOR CORRECTION

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***Abstract* – This paper presents the modeling and control of a single-stage isolated current rectifier with power factor correction based on Full-Bridge and Flyback topologies. The state-space averaged model of the converter for step-down and step-up operation modes is presented, as well as the design and analysis of the digital control system. Experimental results based on a 3.5 kW prototype are presented to verify the performance of the proposed control system.**

***Keywords* – Modeling and control of static converters, Digital control, Power factor correction.**

I. INTRODUCTION

Switching-mode power converters with power factor correction (PFC) have been widely used to supply a stable voltage for electronic equipment [1],[2]. These converters are designed to guarantee a regulated output voltage as well as to draw an input current with sinusoidal waveform, in order to comply with the international standards [3].

Many PFC converter applications require galvanic isolation between the mains and the load. These applications normally employ two-stage converters, where a boost PFC pre-regulator converter is cascaded to a dc-dc isolated converter [4]–[6]. Although two-stage PFC circuits offer excellent performance in terms of input power factor, holdup time capability and low-frequency ripple in the output voltage, they have the disadvantages of low-power density. In order to provide a cost effective and high-density solution for PFC rectifiers, several single-stage PFC converters have been proposed, such as the Flyback-Push-Pull [7], Full-Bridge Boost [8], [9] topologies, among others.

The Full-Bridge-Flyback topology [10] was proposed to overcome some drawbacks of the Flyback-Push-Pull and Full-Bridge-Boost topologies. The main features of this converter are the constant switching frequency, step-down or step-up operation, high power level capability and the absence of an auxiliary pre-loading circuit to control the inrush current. On the other hand, the efficiency of this converter is highly dependent on the leakage inductance. As a result, this topology has several advantages that make it attractive for many applications, in particular if planar transformers are available to mitigate it main drawback.

This paper presents the modeling and digital control of an ac-dc power factor correction (PFC) circuit based on the isolated Full-Bridge–Flyback topology. The control scheme uses two cascaded control loops: a current loop, which is used to track the input current reference; and a voltage loop to obtain a regulated output voltage. The design of the controllers is based on frequency response techniques, using the small-signal averaged models of the converter presented in the paper. Experimental results for a 3.5kVA converter are provided to validate the proposed control technique.

The paper is organized as follows. Section II presents the system description, including the converter features and control loop structure. Section III presents the small signal averaged model of the duty-cycle to input current in both operating modes, while the small-signal input current to output voltage model is shown in Section IV. Section V presents the design procedure for both control loops. Section VI presents the experimental results to validate the proposed control scheme.

II. SYSTEM DESCRIPTION

Fig. 1 shows the digitally controlled PFC converter. The circuit is composed of a line diode rectifier (D_1, D_2, D_3 and D_4), a Flyback coupled inductor (L_c), four main switches (S_1, S_2, S_3 and S_4), a Full-Bridge transformer (T_1), two Flyback diodes (D_5 and D_6), four Full-Bridge diodes (D_7, D_8, D_9 and D_{10}) and an output filter capacitor (C_o). It is assumed unitary turn ratio for both transformer T_1 and coupled inductor L_c.

This converter can operate in two different modes, according to the input and output voltage levels, as can be observed in Fig. 2. When the rectified input voltage (v_{in}) is lower than the output voltage referred to the transformer primary (v_o') the converter operates in step-up mode. On the other hand, the converter operates in step-down mode when v_{in} is higher than v_o'. Assuming a unitary turn ratio in T_1 and L_c the transition between the operation modes occurs when the duty cycle is equal to 0.5.

The PWM switching strategy uses two comparators and two sawtooth waveforms with a 180° phase-shift between them, as shown in Fig. 1. In this strategy, the control action d is sampled once in each sawtooth cycle for the digital implementation of the pulse-width modulator. The command signals of S_1 and S_4 are obtained from the comparison of the control action d with one sawtooth waveform (v_x), while the command signal of S_2 and S_3 are obtained from the comparison of d with the other one (v_y). The pulse-width modulation pattern for the main switches is illustrated in Fig. 3. As can be seen, the modulation strategy is the same in both conduction modes but the resulting PWM pattern is different.

Considering that the switching frequency is much higher than the fundamental frequency, the input voltage is constant and the proposed converter can be analyzed as a dc-dc converter. Assuming the continuous conduction mode (CCM), the converter has four stages in a switching period for each operation mode [10]. From these considerations, the dc voltage gain of the converter in step-up and step-down

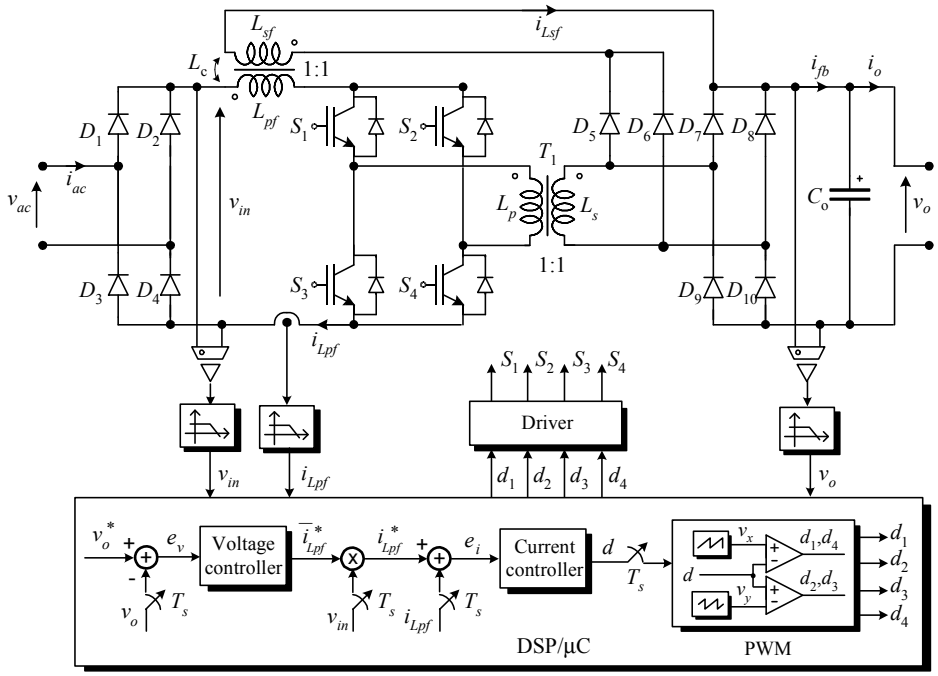


Fig. 1 Ac-dc converter with digital control.

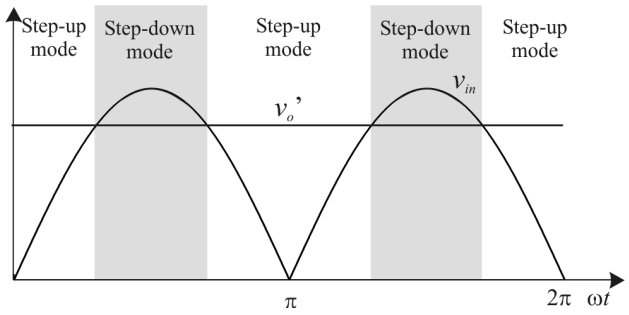


Fig. 2 Operation modes of the ac-dc converter.

operation modes, respectively, can be derived:

$$M_{up} = \frac{V_o}{V_{in}} = \frac{D}{1-D} \quad (1)$$

$$M_{down} = \frac{V_o}{V_{in}} = 2D \quad (2)$$

where V_o is the output voltage, V_{in} the input voltage and D is the duty cycle.

As can be seen in (1) and (2), both operation modes in CCM present the same dc voltage gain when the duty cycle reaches 0.5. Consequently, this converter presents a smooth transition between operating modes.

The digital average current mode control used on this project is shown in Fig. 1. This control technique uses two cascaded control loops: a current loop, which is used to track the input current reference; and a voltage loop that is used to obtain a regulated output voltage. Fig. 4 shows the block diagram of cascaded control loop, where $T_s = 1 / f_s$ is the sampling period.

For proper operation of both control loops, it is presumed the dynamic decoupling (time-scale separation) between the current and voltage dynamics. In PFC converters, the condition for timescale separation is guaranteed with a small input inductance L_c and a large output capacitor C_o, as

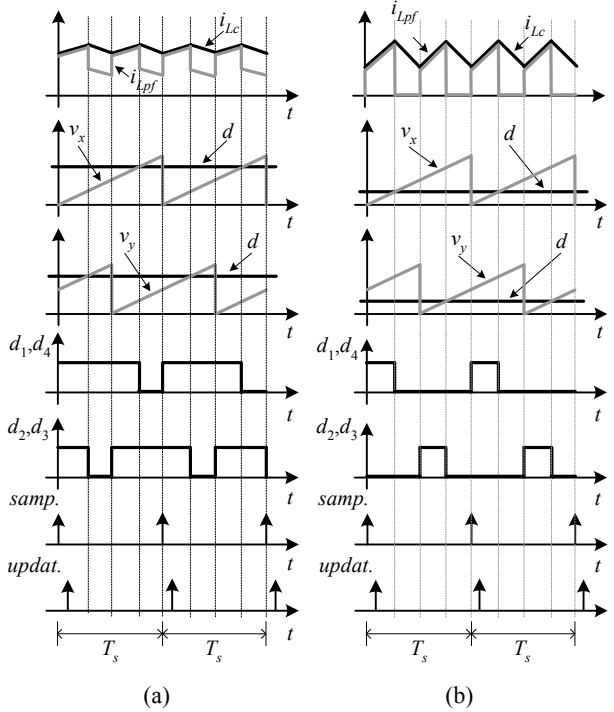


Fig. 3 PWM pattern. (a) Step-up mode. (b) Step-down mode.

demonstrated in [13]. In this case, the input current has a dynamic behavior much faster than the output voltage.

The design of the current loop is based on the small-signal ac model of the converter. This model considers the duty-cycle to input current characteristic of the rectifier. On the other hand, the model used to design the voltage loop is based on the transconductance of the converter. This small-signal model considers the input current to output voltage characteristic of the converter.

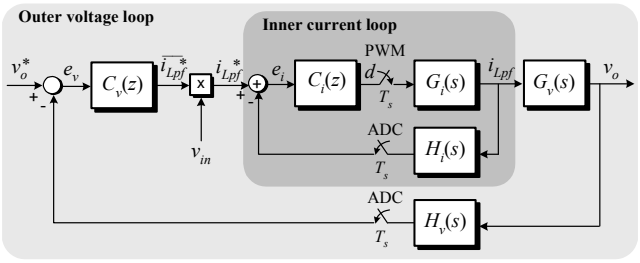


Fig. 4 Digital control structure.

III. DUTY-RATIO TO INPUT CURRENT STATE-SPACE AVERAGED MODEL

A. Step-up Mode

This section presents the ac small-signal model of the CCM Full-Bridge-Flyback isolated current converter shown in Fig. 1 in step-up mode. The objective is to derive the transfer function from duty-ratio to inductor current, using the state-space averaging technique [11], [12].

This modeling technique is based on the piecewise-linear model of the converter. This converter has four operation stages that are represented by two equivalent circuits shown in Fig. 5. The equivalent circuit shown in Fig. 5(a) describes the converter when all switches are simultaneously on, while Fig. 5 (b) presents the equivalent circuit when S_1 and S_4, or S_2 and S_3 are switched off. The duty-cycle used to match the equivalent circuit with the converter is given by:

$$D_{up} = 2D - 1 \tag{3}$$

The state-space averaging approach requires a common set of state variables for all equivalent circuits. Both equivalent circuits have dimension two if T_1 is assumed as an ideal transformer.

The magnetizing current $i_{Lc}(t)$ of the coupled inductor has been considered as state variable to derive the CCM state-space averaged model of the converter. The input current $i_{Lpf}(t)$ cannot be directly used because the small-ripple approximation cannot be considered [11], as can be seen in Fig. 3. As a result, the state variables, inputs and outputs are defined, respectively, as follows:

$$\mathbf{x}(t) = \left[i_{Lc}(t) \quad v_o(t) \right]^T \tag{4}$$

$$\mathbf{u}(t) = \left[v_{in}(t) \right] \tag{5}$$

$$\mathbf{y}(t) = \left[i_{Lc}(t) \right] \tag{6}$$

where the magnetizing current is given by:

$$i_{Lc}(t) = i_{Lpf}(t) + i_{Lsf}(t) \tag{7}$$

The linear state-space models are given by:

$$\begin{cases} \mathbf{K}\,\dfrac{d\mathbf{x}(t)}{dt} = \mathbf{A}_i\,\mathbf{x}(t) + \mathbf{B}_i\,\mathbf{u}(t) \\ \mathbf{y}(t) = \mathbf{C}_i\,\mathbf{x}(t) + \mathbf{E}_i\,\mathbf{u}(t) \end{cases}, \quad i = 1, 2 \tag{8}$$

where i represents the operating stage and:

$$\mathbf{K} = \begin{bmatrix} L_c & 0 \\ 0 & C_o \end{bmatrix} \tag{9}$$

The state-space representation for stage 1 is given by:

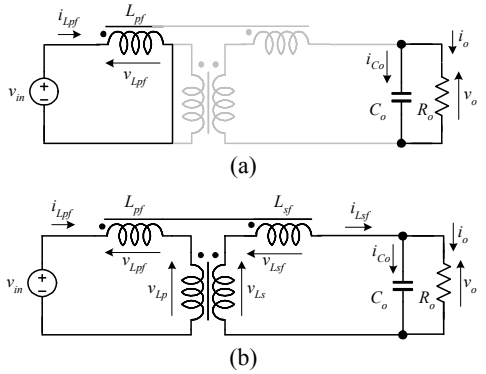


Fig. 5 Equivalent model of the converter operating in step-up mode. (a) Stage 1. (b) Stage 2.

$$\mathbf{A}_1 = \begin{bmatrix} 0 & 0 \\ 0 & -1/R_o \end{bmatrix} \quad \mathbf{B}_1 = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \tag{10}$$
$$\mathbf{C}_1 = \begin{bmatrix} 1 & 0 \end{bmatrix} \qquad \mathbf{E}_1 = \begin{bmatrix} 0 \end{bmatrix}$$

On the other hand, for stage 2, the model is given by:

$$\mathbf{A}_2 = \begin{bmatrix} 0 & -1/2 \\ 1/2 & -1/R_o \end{bmatrix} \quad \mathbf{B}_2 = \begin{bmatrix} 1/2 \\ 0 \end{bmatrix} \tag{11}$$
$$\mathbf{C}_2 = \begin{bmatrix} 1 & 0 \end{bmatrix} \qquad \mathbf{E}_2 = \begin{bmatrix} 0 \end{bmatrix}$$

The linearized small-signal ac averaged model of the converter for quiescent operating point is given by [11]:

$$\begin{cases} \mathbf{K}\,\dfrac{d\hat{\mathbf{x}}(t)}{dt} = \mathbf{A}\,\hat{\mathbf{x}}(t) + \mathbf{B}\,\hat{\mathbf{u}}(t) + \mathbf{B}'\hat{d} \\ \mathbf{y}(t) = \mathbf{C}\,\hat{\mathbf{x}}(t) + \mathbf{E}\,\hat{\mathbf{u}}(t) + \mathbf{E}'\hat{d} \end{cases} \tag{12}$$

where:

$$\mathbf{A} = (2D-1)\,\mathbf{A}_1 + (2-2D)\,\mathbf{A}_2 \tag{13}$$

$$\mathbf{B} = (2D-1)\,\mathbf{B}_1 + (2-2D)\,\mathbf{B}_2 \tag{14}$$

$$\mathbf{C} = (2D-1)\,\mathbf{C}_1 + (2-2D)\,\mathbf{C}_2 \tag{15}$$

$$\mathbf{E} = (2D-1)\,\mathbf{E}_1 + (2-2D)\,\mathbf{E}_2 \tag{16}$$

$$\mathbf{B}' = 2(\mathbf{A}_1 - \mathbf{A}_2)\,\mathbf{X} + 2(\mathbf{B}_1 - \mathbf{B}_2)\,\mathbf{U} \tag{17}$$

$$\mathbf{E}' = 2(\mathbf{C}_1 - \mathbf{C}_2)\,\mathbf{X} + 2(\mathbf{E}_1 - \mathbf{E}_2)\,\mathbf{U} \tag{18}$$

$$\mathbf{X} = -\mathbf{A}^{-1}\mathbf{B}\,\mathbf{U} \tag{19}$$

This model is valid for small ac variations around an equilibrium point, where the steady-state values for D, $\mathbf{U}$ and $\mathbf{X}$ are known. So the transfer function from control to inductor current is given by:

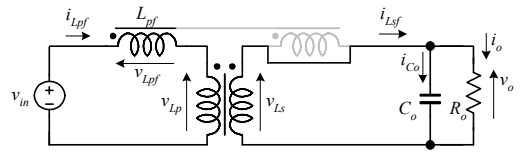
$$\mathbf{y}(s) = \left[\mathbf{C}\left(s\mathbf{I} - \mathbf{K}^{-1}\mathbf{A}\right)^{-1}\mathbf{K}^{-1}\mathbf{B}' + \mathbf{E}' \right]\hat{d}(s) \tag{20}$$

As a result, the model is given by:

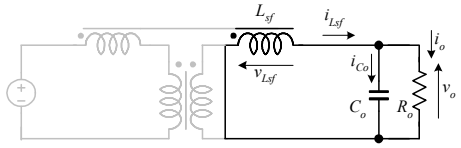
$$G_{Lcd}(s) = \frac{\hat{i}_{Lc}(s)}{\hat{d}(s)} = k \cdot \frac{b_1 s + b_0}{s^2 + a_1 s + a_0} \tag{21}$$

where:

$$k = \frac{V_{in}}{R_o(1-D)^2} \qquad a_2 = L_c R_o C_o$$
$$b_1 = C_o R_o\left[R_o(1-D)\right] \qquad a_1 = L_c \tag{22}$$
$$b_0 = R_o\left(1-D^2\right) \qquad a_0 = R_o(1-D)^2$$



(a)



(b)

Fig. 6 Equivalent model of the converter operating in step-down mode. (a) Stage 1. (b) Stage 2.

The relation between the averaged input current $i_{Lpf}(t)$ and averaged magnetizing current $i_{Lc}(t)$ is given by:

$$\left\langle i_{Lpf}(t)\right\rangle = \left[2d(t)-1\right]\left\langle i_{Lc}(t)\right\rangle + \frac{\left[2-2d(t)\right]}{2}\left\langle i_{Lc}(t)\right\rangle \quad (23)$$

Applying the small perturbation analysis in (23) and neglecting the dc and second-order terms of the resulting equation [11], we obtain the following linearized ac equation:

$$\hat{i}_{Lpf}(s) = D\hat{G}_{Lcd}(s)\hat{d}(s) + I_{Lc}(D)\hat{d}(s) \quad (24)$$

where:

$$I_{Lc}(D) = \frac{2V_o^{\,3}}{R_o V_{in\max}^{\,2}}\frac{1-D}{D^2} \quad (25)$$

The substitution of (21) and (25) into (24) results:

$$G_i(s) = \frac{\hat{i}_{Lpf}(s)}{\hat{d}(s)} = \frac{c_2 s^2 + c_1 s + c_0}{s^2 + a_1 s + a_0} \quad (26)$$

where:

$$c_2 = a_2 I_{Lc}(D), \quad c_1 = D k b_1 + a_1 I_{Lc}(D), \quad c_0 = D k b_0 + a_0 I_{Lc}(D) \quad (27)$$

B. Step-down Mode

This section presents the ac small-signal model of the CCM Full-Bridge-Flyback isolated current converter shown in Fig. 1 in step-down mode. The objective is to derive the transfer function from duty-ratio to inductor current, using the state-space averaging technique.

This converter is represented by the equivalent circuits shown in Fig. 6. The equivalent circuit shown in Fig. 6 (a) describes the converter when S_1 and S_4, or S_2 and S_3 are switched on, while Fig. 6 (b) presents the equivalent circuit when all switches are simultaneously off. The duty-cycle used to match the equivalent circuit with the converter is given by:

$$D_{down} = 2D \quad (28)$$

The state-space averaged model in step-down mode is also derived from the magnetizing current $i_{Lc}(t)$ of the coupled inductor. As a result, the state variables, inputs and outputs are given by (4)-(6).

The linear state-space model in the stages 1 and 2, respectively, are given by:

$$\mathbf{A}_1 = \begin{bmatrix} 0 & -1 \\ 1 & -1/R_o \end{bmatrix} \quad \mathbf{B}_1 = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \quad (29)$$

$$\mathbf{C}_1 = \begin{bmatrix} 1 & 0 \end{bmatrix} \quad \mathbf{E}_1 = \begin{bmatrix} 0 \end{bmatrix}$$

$$\mathbf{A}_2 = \begin{bmatrix} 0 & -1 \\ 1 & -1/R_o \end{bmatrix} \quad \mathbf{B}_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad (30)$$

$$\mathbf{C}_2 = \begin{bmatrix} 1 & 0 \end{bmatrix} \quad \mathbf{E}_2 = \begin{bmatrix} 0 \end{bmatrix}$$

where **K** is given by (9).

The linearized small-signal ac averaged model of the converter for the quiescent operating point is described by (12), where:

$$\mathbf{A} = 2D\,\mathbf{A}_1 + (1-2D)\,\mathbf{A}_2 \quad (31)$$

$$\mathbf{B} = 2D\,\mathbf{B}_1 + (1-2D)\,\mathbf{B}_2 \quad (32)$$

$$\mathbf{C} = 2D\,\mathbf{C}_1 + (1-2D)\,\mathbf{C}_2 \quad (33)$$

$$\mathbf{E} = 2D\,\mathbf{E}_1 + (1-2D)\,\mathbf{E}_2 \quad (34)$$

and **B'**, **E'**, **X** are given by (17)-(19), respectively.

From (12), we obtain the small-signal averaged model from duty-cycle to magnetizing current. This model is given by (21), where:

$$k = V_o/(L_c D) \qquad a_2 = 1$$

$$b_1 = 1 \qquad a_1 = \frac{1}{R_o C_o} \quad (35)$$

$$b_0 = \frac{1}{R_o C_o} \qquad a_0 = \frac{1}{L_c C_o}$$

The relation between the input current $i_{Lpf}(t)$ and magnetizing current $i_{Lc}(t)$ is given by:

$$\left\langle i_{Lpf}(t)\right\rangle = 2\left\langle d(t)\right\rangle\left\langle i_{Lc}(t)\right\rangle \quad (36)$$

Applying the small perturbation analysis in (36) and neglecting the dc and second-order nonlinear terms of the resulting equation, we obtain the following linearized ac relation:

$$\hat{i}_{Lpf}(s) = 2D\hat{G}_{Lcd}(s)\hat{d}(s) + 2I_{Lc}(D)\hat{d}(s) \quad (37)$$

where:

$$I_{Lc}(D) = \frac{V_o^{\,3}}{2R_o D^2 V_{in\max}^{\,2}} \quad (38)$$

The substitution of (35) and (38) into (37) results:

$$G_i(s) = \frac{\hat{i}_{Lpf}(s)}{\hat{d}(s)} = \frac{c_2 s^2 + c_1 s + c_0}{s^2 + a_1 s + a_0} \quad (39)$$

where:

$$c_2 = 2I_{Lc}(D), \quad c_1 = 2Dkb_1 + 2a_1 I_{Lc}(D), \quad c_0 = 2Dkb_0 + 2a_0 I_{Lc}(D) \quad (40)$$

IV. INPUT CURRENT TO OUTPUT VOLTAGE SMALL-SIGNAL AVERAGED MODEL

This section presents the small-signal averaged model from input current to output voltage of the Full-Bridge-Flyback isolated current converter shown in Fig. 1. Due to the nonlinear characteristic of the converter, the linear transfer function is derived for a quiescent operating point.

The model utilizes power balance equations that are averaged over a semi-cycle of the input voltage. As a result,

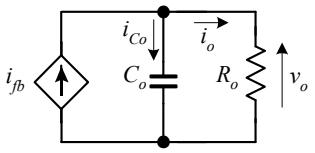


Fig. 7 Equivalent circuit used to derive the input current to output voltage model

the frequency range of this model is only accurate from dc to $2f_1$, where f_1 is the input voltage frequency.

Fig. 7 shows the equivalent circuit representation of the output stage of the converter. The transfer function from the full-bridge converter current i_{fb} to the output voltage v_o is given by:

$$\frac{v_o(s)}{i_{fb}(s)} = \frac{1/C_o}{s+1/R_oC_o} \tag{41}$$

The relation between the current i_{fb} and the i_{Lpf} is non-linear. The linearization for the nominal quiescent operating point is performed considering the power balance of the converter:

$$P_o = P_{in}\eta, \tag{42}$$

where η is the efficiency of the converter.

Assuming a unitary power factor and that the capacitor C_o is large enough to produce an output voltage with small ripple, we can rewrite (42) as:

$$I_o V_o = I_{ac} V_{ac} \eta \tag{43}$$

where I_{ac} and V_{ac} are the rms values of the input current (i_{ac}) and input voltage (v_{ac}), respectively, and I_o and V_o are the dc values of the output current and output voltage, respectively.

Assuming the relation between the rms value of the input current and the average current in the inductor L_{pf} is:

$$\overline{I_{Lpf}} = \frac{1}{\pi}\int_0^{\pi}\sqrt{2}I_{ac}\sin(\omega t)\,d\omega t = \frac{2\sqrt{2}I_{ac}}{\pi} \tag{44}$$

and $I_o = \overline{I_{fb}}$ and $m_a = \sqrt{2}V_{ac}/V_o$, we obtain the following relation:

$$\overline{I_{fb}} = \frac{\pi m_a \eta \overline{I_{Lpf}}}{4} \tag{45}$$

The quiescent operating point averaged model is derived replacing (45) in (41):

$$G_v(s) = \frac{\overline{v_o}(s)}{\overline{i_{Lpf}}(s)} = \frac{\pi m_a \eta}{4}\cdot\frac{1/C_o}{s+1/R_oC_o} \tag{46}$$

V. CONTROL DESIGN

This section presents a digital control design for the converter parameters given in Table 1. In this case, this converter is used in the input stage of a double-conversion UPS, whose dc bus voltage is higher than the input voltage. As a result, the converter only operates in step-up mode.

The digital control system has been implemented in the DSP TMS320F2812, and then the design methodology of the current and voltage controllers considers the main characteristics of this DSP [14]. The crossover frequency of the current loop gain was chosen as 7.5 kHz to achieve a good dynamic performance and the crossover frequency of the voltage loop gain was chosen as 12 Hz to synthesize low-THD input currents. Consequently, the input current has a dynamic behavior much faster than the output voltage and the control loops are dynamically decoupled [13].

Table 1
Converter parameters

P_o = 3.5 kW	Nominal output power
V_o = 400 V	Nominal output voltage
V_{ac} = 220 V_{rms}	Nominal input voltage
f_1 = 60 Hz	Input voltage frequency
f_s = 75 kHz	Switching frequency
R_o = 45.7 Ω	Nominal load resistance
C_o = 2.9 mF	Output converter capacitance
$L_{pf} = L_{sf} = L_c$ = 200 μH	Input converter inductance
η = 0.9	Efficiency of the converter

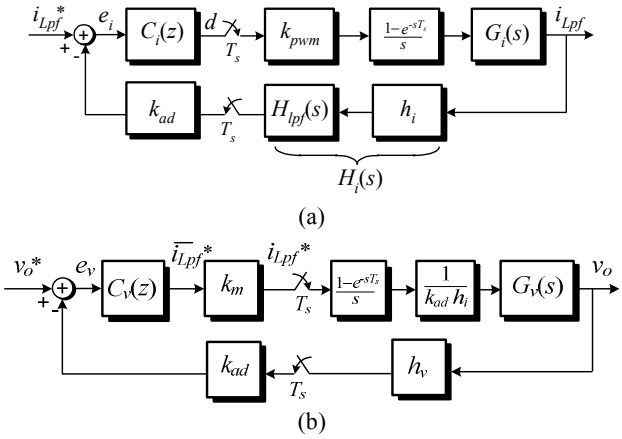


Fig. 8 Detailed digital control structure.
(a) Current loop. (b) Voltage loop.

A. Current Loop

A block diagram of the digital system used to control the input current is presented in Fig. 8(a), where $C_i(z)$ is a digital proportional-integral (PI) controller.

A first-order low pass filter was included in the feedback path to obtain the average value of the current i_{Lpf}:

$$H_i(s) = h_i H_{lpf}(s) = h_i\frac{1/R_{lp}C_{lp}}{s+1/R_{lp}C_{lp}} \tag{47}$$

where h_i is the current sensor gain. The parameters of this filter are shown in Table 2.

The pulse-width modulator can be approximated by a zero-order hold (ZOH) because the switching frequency is much higher than the reference signal frequency [15]. Therefore, the discrete-time transfer function of $G_iH_i(s)$ is given by:

$$G_iH_i(z) = Z\left\{\left(\frac{1-e^{-sT_s}}{s}\right)G_i(s)H_i(s)\right\} \tag{48}$$

The design of the digital PI controller was based on the frequency response method using the w-plane methodology [15]. Consequently, it is necessary to obtain the open-loop transfer function $T_i(w)$ in w-domain. For the system shown in Fig. 8(a), this transfer function is given by:

$$T_i(w) = k_{pwm}k_{ad}C_i(w)G_iH_i(w) \tag{49}$$

Table 2
Control system parameters

f_s = 75 kHz	Sampling frequency
R_{lp} = 1 kΩ	Resistance of low-pass filter
C_{lp} = 10 nF	Capacitance of low-pass filter
h_i = 0.1	Current sensor gain
h_v = 0.005	Output voltage sensor gain
h_{vin} = 0.0042	Input voltage sensor gain
$k_{ad} = 2^{12}/3$	A/D converter gain
k_{pwm} = 1/2000	PWM gain

where k_{pwm} is the PWM gain, k_{ad} is the A/D converter gain and:

$$z = \frac{1+\frac{T_s}{2}w}{1-\frac{T_s}{2}w} \tag{50}$$

Applying the w-plane transform (50) to the transfer function $C_i(z)$, the w-domain transfer function of the PI controller can be given by:

$$C_i(w) = k_i \frac{w+\omega_i}{w} \tag{51}$$

where k_i and ω_i are the parameters to be designed.

From (26) and (27), one can verify that the duty-ratio to input current transfer function $G_i(s)$ depends on the duty-cycle. Therefore, the transfer function $G_iH_i(w)$ also depends on the operating point. This is particularly important for PFC converters, because the input voltage is variable. Fig. 9 shows the frequency response of $G_iH_i(w)$ for two distinct input voltage levels: V_{in} = 1 V (slightly higher than lower value) and V_{in} = 311 V (peak value). One can observe that this transfer function present larger phase-shift and smaller magnitude at high frequencies when V_{in} = 1 V. Consequently, the current compensator was designed for this operating point (V_{in} = 1 V) to ensure minimum values of phase margin and crossover frequency at all operating points.

The specifications imposed to the digital control system are a minimum phase margin equal to 45° and a minimum crossover frequency equal to 7.5 kHz, which results in a crossover frequency equal to 7.75 kHz in the w-plane [15]. As a result, the transfer function of the PI current controller is:

$$C_i(w) = \frac{0.39w + 753.5}{w} \tag{52}$$

The discrete-time current controller is derived from w-plane to z-plane transform:

$$C_i(z) = \frac{0.395z - 0.385}{z-1} \tag{53}$$

whose discrete-time differences equation results in:

$$d(k) = d(k-1) + 0.395e_i(k) - 0.385e_i(k-1) \tag{54}$$

Fig. 10 presents the frequency response of the open-loop transfer function $T_i(w)$ with the compensator shown in (52).

B. Voltage loop

A block diagram of the digital control system used to regulate the output voltage is shown in Fig. 8(b), where $C_v(z)$ also is a digital PI controller.

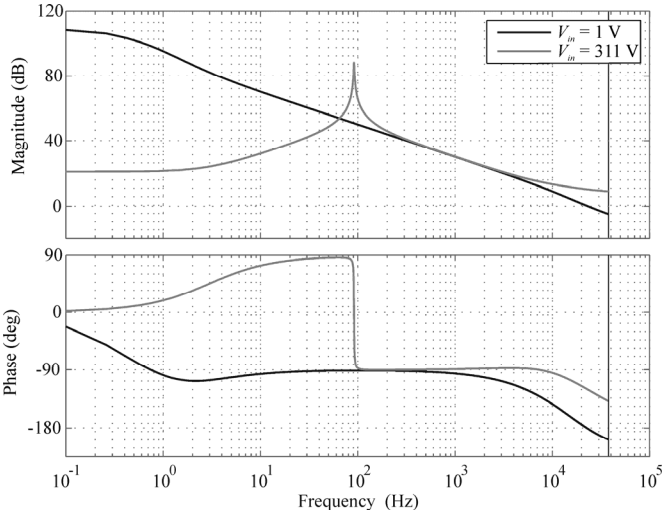


Fig. 9 Frequency response of $G_iH_i(w)$.

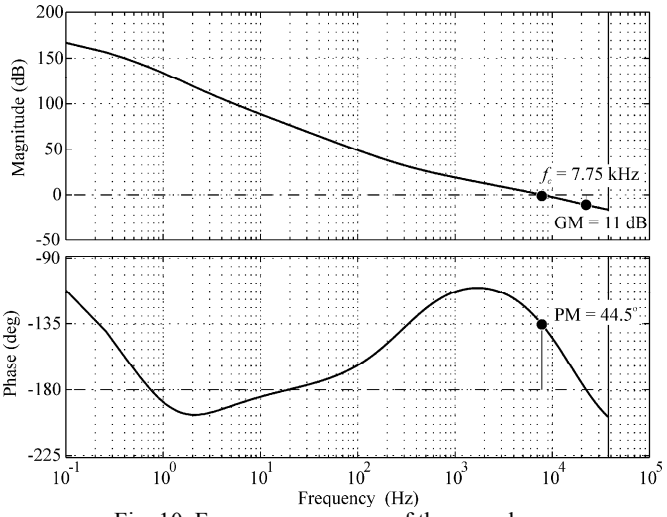


Fig. 10 Frequency response of the open-loop transfer function $T_i(w)$.

It is assumed that the input current is constant over a switching period to derive the discrete-time transfer function of $G_v(s)$, then:

$$G_v(z) = Z\left\{\left(\frac{1-e^{-sT_s}}{s}\right)G_v(s)\right\} \tag{55}$$

Fig. 11 shows the frequency response of $G_v(w)$, which is obtained by applying the w-plane transform (50) in $G_v(z)$, with nominal load and nominal amplitude modulation depth (m_a).

For the system presented in Fig. 8(b), the w-domain open-loop transfer function $T_v(w)$, utilized to design the voltage controller, is given by:

$$T_v(w) = k_m k_{ad} h_v \frac{1}{k_{ad} h_i} C_v(w) G_v(w) \tag{56}$$

where h_v is the voltage sensor gain, $1/(k_{ad}h_i)$ is the low-frequency gain of the current loop, and k_m is the equivalent multiplier gain, given by:

$$k_m = h_{vin} k_{ad} \overline{V_{in}} \tag{57}$$

where $\overline{V_{in}} = 2V_{in\max}/\pi$.

Applying the w-plane transform (50) to the transfer function $C_v(z)$, the w-domain transfer function of the PI voltage controller can be given by:

$$C_v(w) = k_v \frac{w + \omega_v}{w} \quad (58)$$

where k_v and ω_v are the parameters to be designed.

The zero ω_v of the PI controller is placed to cancel the pole of $G_v(w)$. The gain k_v is adjusted to obtain the specified crossover frequency of $T_v(w)$.

As a result, the transfer function of the PI voltage controller is:

$$C_v(w) = 7.04197 \cdot 10^{-3} \frac{w + 7.5431}{w} \quad (59)$$

Then, the discrete-time voltage controller can be computed by using the w-plane to z-plane transform:

$$C_v(z) = \frac{7.0423 \cdot 10^{-3} z - 7.0416 \cdot 10^{-3}}{z - 1} \quad (60)$$

whose discrete-time differences equation is given by:

$$\overline{i_{Lpf}^*}(k) = \overline{i_{Lpf}^*}(k-1) + 7.0423 \cdot 10^{-3} e_v(k) - 7.0416 \cdot 10^{-3} e_v(k-1) \quad (61)$$

As can be observed from Fig. 12, the resulting phase margin of $T_v(w)$ is 90° and the crossover frequency is 12 Hz.

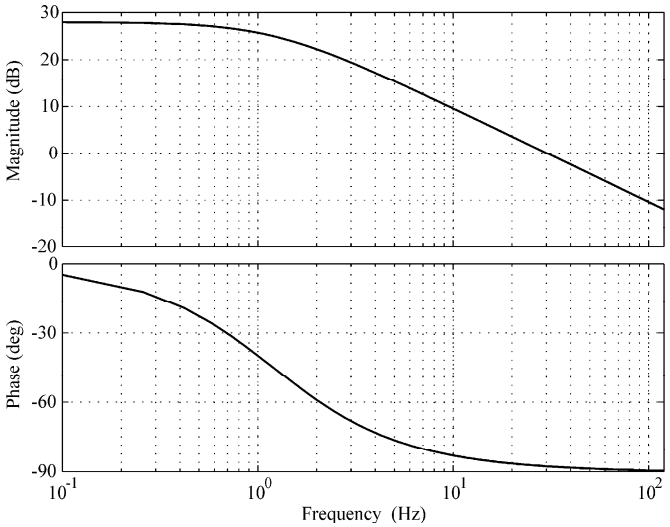


Fig. 11 Frequency response of $G_v(w)$.

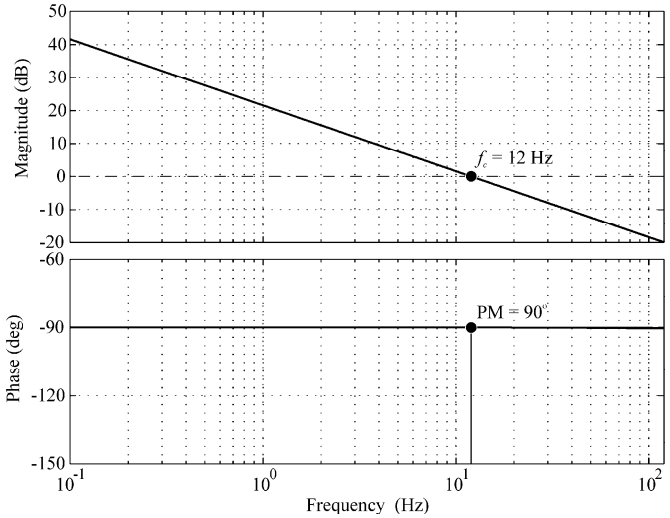


Fig. 12 Frequency response of the open-loop transfer function $T_v(w)$.

VI. EXPERIMENTAL RESULTS

A prototype of the closed-loop converter shown in Fig. 1 was built in our lab to verify the performance of the digital control system under distinct practical conditions. The digital controllers were implemented on DSP TMS320F2812 from Texas Instruments. The main parameters of the prototype and control system are presented in Table 1 and in Table 2, respectively.

Fig. 13 shows the input current, input and output voltage waveforms with a resistive load equal to 58.6 Ω, an output voltage equal to 400 V and nominal input voltage. At this operating point, the converter operates only in step-up mode, the total harmonic distortion (THD) of the input current

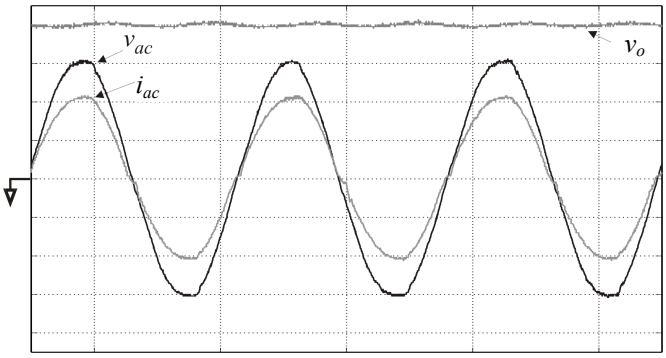


Fig. 13 Step-up mode: input current, input and output voltage waveforms (100 V/div, 10 A/div, 5 ms/div).

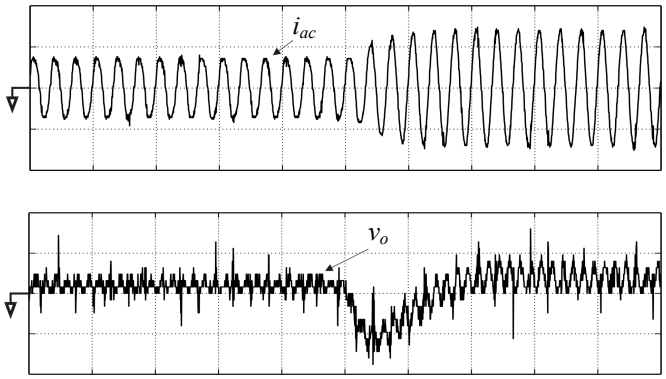


Fig. 14 Step-up mode: input current (top) and output voltage (bottom) under a sudden load change from 244 Ω to 122 Ω (10 A/div, 10 V/div, 50 ms/div).

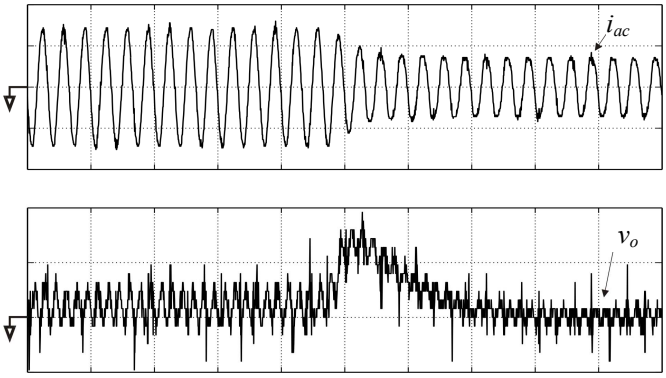


Fig. 15 Step-up mode: input current (top) and output voltage (bottom) under a sudden load change from 122 Ω to 244 Ω (10 A/div, 10 V/div, 50 ms/div).

waveform is 3.65% and the input power factor is 0.99.

Fig. 14 shows the input current and the output voltage during a sudden load change from 244 Ω to 122 Ω. The output voltage waveform was measured in ac mode to obtain a better visualization. On the other hand, Fig. 15 presents the same waveforms during a sudden load change from 122 Ω to 244 Ω. Both results illustrate the satisfactory transient performance of the closed-loop system.

VII. CONCLUSION

This paper presented a systematic procedure to design a digital control system for the Full-Bridge-Flyback isolated rectifier with power factor correction. The design of the controllers was based on frequency response techniques, using the small-signal models of the converter. The duty ratio-to-input current models for each operation mode were obtained from state-space averaging, whereas the input-current-to-output voltage model was derived from power balance analysis.

Experimental results show that the closed-loop system has a good steady-state and transient performances, even with sudden load changes.

REFERENCES

[1] P. Kong, S. Wang, F. C. Lee "Improving Balance Technique for High Frequency Common Mode Noise Reduction in Boost PFC Converters", IEEE PESC2008, pp. 2941–2947, jun. 2008.

[2] G. Chu, T. Siew-Chong, C. K. Tse, W. S. Chung, "General Control for Boost PFC Converter from a Sliding Mode Viewpoint", IEEE PESC2008, pp. 4452–4456, jun. 2008.

[3] International Electrotechnical Commission, *IEC 61000-3-2 - Electromagnetic compatibility (EMC) - Part 3-2 - Limits for harmonic current emissions (equipment input current up to and including 16 A per phase),* 2005.

[4] R. P. Torrico-Bascopé, D. S. Oliveira Jr., C. G. C. Branco, F. L. M. Antunes, "A High Frequency Transformer Isolation UPS System with 110V/220V Input Voltage", *Eletrônica de Potência*, vol. 11, no. 3 nov. 2006.

[5] L. Il-Oun, D. Y. Lee, B. H. Cho, "High performance boost PFC pre-regulator with improved zero-voltage-transition (ZVT) converter", IEEE PESC2002, vol. 3, pp. 1387–1391, jun. 2002.

[6] L. Woo-Jin, P. Ki-Bum, H. Tae-Won, M. Gun-Woo, "Output inductor less phase shift full bridge converter with current stress reduction technique for server power application". IEEE PESC2008, pp. 2517–2522, jun. 2008.

[7] G. V. T. Bascopé, "Conversor Flyback-Push-Pull alimentado em corrente com correção de fator de potência (in portuguese)", Master dissertation, Universidade Federal de Santa Catarina, jun. 1996.

[8] C. Jiann-Fuh, C. Ren-Yi, L. Tsorng-Juu, "Study and Implementation of a Single-Stage Current-Fed Boost PFC Converter With ZCS for High Voltage Applications", *IEEE Transactions on Power Electronics*, vol. 23, pp. 379–386, jan. 2008.

[9] P. Em-Sung, J. C. Sung, J. M. Lee, B. H Cho, "A soft-switching active clamp scheme for isolated full-bridge boost converter", APEC'04 IEEE, vol. 2, pp. 1067-1070, 2004.

[10] J. Duarte, M. Mezaroba, "Conversor Flyback Full-Bridge com entrada em corrente e correção do fator de potência (in portuguese)", CBA2008, 2008.

[11] R. W. Erickson, D. Maksimovic, *Fundamentals of power eletronics*, 2nd edition, University of Colorado; 2001.

[12] W. Tang, F. C. Lee, R. B. Ridley, "Small-signal modeling of average current-mode control"; IEEE APEC'92, pp. 747-755, 1992.

[13] S. Wall, R. Jackson, "Fast controller design for single-phase power-factor correction systems", *IEEE Transactions on Industrial Electronics*, vol. 44, no. 5, pp. 654-660, oct. 1997.

[14] *TMS320F2812 Data Manual*, Literature Number SPRS174L, dez. 2004.

[15] K. Ogata, *Discrete-Time Control Systems*, 2nd edition, Prentice Hall, New Jersey, 1994.