A ZVS PWM Three-Phase Inverter with Active Clamping Technique Using Only a Single Auxiliary Switch

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Abstract - This paper presents the analysis of a ZVS PWM Three-Phase Inverter with active voltage clamping technique using the reverse recovery energy of the diodes to improve the converter efficiency. The structure is particularly simple and robust. It is very attractive for Three Phase high power applications. Conduction and commutation losses are reduced due to implementation of a simple active snubber circuit that provides ZVS conditions for all switches, including the auxiliary one. Its main features are: Simple control strategy, robustness, lower weight and volume, lower harmonic distortion of the output current, and high efficiency. The operation principle for steady-state conditions, mathematical analysis and experimental results from a laboratory prototype are presented.

I. Introduction

With the appearance of the Bipolar Transistors in the 50s and posteriori the Mosfets in the 80s, PWM modulation techniques could be used together with the increase of the commutation frequency, with the aim to reduce the harmonic distortion in the output of the inverters. These measures give some benefits like the reduction of the volume and weight of the filters and magnetic elements; nevertheless they cause some difficulties due to the high commutation losses in the switches, which reduce the converter efficiency, and the electromagnetic interference appearing. This event occurs mainly in inverter topologies that use the bridge configuration; where the main switch conduction provoke the reverse recovery phenomenon of the anti-parallel diode of the complementary switch. A great number of works have been developed by power electronics scientific community, with the aim to diminish these problems. They can be divided in two groups: passive techniques [6, 7, 8, 9] and active techniques [1, 2,3 10, 11].

In the active techniques area, some researches were made recently using the reverse-recovery energy from the diodes to obtain soft commutation in the switches of the pre-regulated rectifiers with high power factor [4, 5].

In this paper a ZVS PWM Three-Phase Inverter with voltage clamping across the switches, using only a single auxiliary switch, is presented. The proposed structure uses the diode reverse recovery energy technique to obtain soft commutation in all switches.

This topology presents some advantages in comparison with the conventional soft commutation inverters studied in the literature, which we can print out:

- Soft commutation in all load range;
- Simple topology with a low number of components;
- Use a classical PWM modulation;
- Auxiliary switch works with constant duty cycle in all operation stages;
- Use of slow and low cost rectifiers diodes;
- Low clamping voltage across the capacitor;
- Low current stress through the main switches;
- Simple design procedure with low restrictions;
- High efficiency.

II. Proposed Circuit

The proposed circuit is shown in Fig. 1. It presents a Three-Phase inverter configuration, where **Q1, Q2, Q3, Q4, Q5** and **Q6** are the main switches, and **Qa** is the auxiliary switch. **C1, C2, C3, C4, C5** and **C6** are the commutation capacitors.

One controlled switch Qa, with anti-parallel diode Da, one small inductor Ls and one clamping capacitor Cs form the snubber circuit. The capacitor **Cs** is responsible by the storage of the diode reverse recovery energy and by the clamping of switches voltage. The inductor **Ls** is responsible by the control of the **di/dt** during the diode reverse recovery time. The auxiliary switch works with constant duty cycle in all operation stage. One of the most advantages of this converter consists in the use of only one auxiliary switch, which provides the clamping of the voltage and the ZVS conditions for all switches, including the auxiliary switch in the snubber circuit.

III. Operation Stages (for the first half cycle)

The inverter has symmetrical operation stages, so, will be presented the analysis to only one combination of the load currents. To simplify the studies, the following assumptions

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are made: the operation of the circuit is steady state; the semiconductors are considered ideal (excluding the reverse recovery of the diodes); the voltage across the capacitor **Cs**, and the current in the output inductors are considered constant during the switching period. The main waveforms are shown in **Fig. 2** and **Fig. 3** shows the main operation stages.

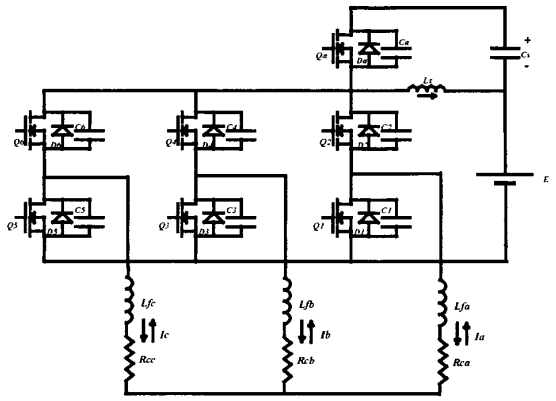

Fig. 1. Proposed Circuit.

First stage (t0-t1): At this stage, the current ***Ia*** flows through the circuit formed by inductor ***Ls***, source ***V1*** and diode ***D5***. The current ***Ib*** flows through the diode ***D4*** and current ***Ic*** flows through the diode ***D2***. At same time, the additional current ***iLs*** flows through **Qa, Ls e Cs**.

Second stage (t1-t2): This stage starts when the auxiliary switch **Qa** is blocked. The current ***iLs*** begins the charge of the capacitor **Ca** from **zero** to ***E+Vcs,*** and discharges **C1, C3** and **C6** from ***E+Vcs*** to ***zero***.

Third stage (t2-t3): At this stage the voltage across **C1, C3** and **C6** reaches ***zero,*** and are clamping by the anti-parallel diodes **D1, D3** and ***D6***. So, the switches **Q1, Q3** and **Q6** conduct with ZVS condition. At this moment, the bus voltage **E** is applied across the inductor **Ls** and the current i***Ls*** decrease linearly.

Fourth stage (t3-t4): It begins when the current ***iLs*** inverts its direction and flows through the switches **Q1, Q3** and **Q6**. The current ***iLs*** continues to decrease until inverting its direction of current of the diodes **D2, D4** and **D5**, starting its reverse recovery phase. The inductor **Ls** limits the ***diLs/dt***.

Fifth stage (t4-t5): This stage starts when the diodes **D2, D4** and **D5** finish its reverse recovery phase. The current ***iLs*** begins the charge of the capacitors **C2, C4** and **C5** from ***zero*** to ***E + Vcs*** and the discharge of **Ca** from ***E + Vcs*** to ***zero***.

Sixth stage (t5-t6): At this stage the voltage across the capacitor **Ca** reaches ***zero***, and it is clamped by the diode **Da.** Thus, the auxiliary switch **Qa** conducts with zero-voltage switching. The current ***iLs*** increases, due the application of the voltage **Vcs** across the inductor **Ls**.

Seventh stage (t6-t7): This stage begins when the current ***iCs*** changes its direction and flows through the switch ***Qa***. The current ***iLs*** continues to increase linearly.

Eighth stage (t7-t8): At this stage the switch **Q1** is blocked. The capacitor **C1** charges itself from ***zero*** to ***E + Vcs*** and the capacitor **C2** discharges itself from ***E + Vcs*** to ***zero***.

Ninth stage (t8-t9): It begins when the voltage across the capacitor **C2** reaches ***zero,*** and it is clamped by the diode **D2**. The current ***iLs*** continues increasing.

Tenth stage (t9-t10): At this stage the switch **Q3** is blocked. The capacitor **C3** charges itself from ***zero*** to ***E + Vcs*** and the capacitor **C4** discharges itself from ***E + Vcs*** to ***zero***.

Eleventh stage (t11-t12): It begins when the voltage across the capacitor **C4** reaches ***zero,*** and it is clamped by the diode **D4**. The current ***iLs*** continues increasing.

Twelfth stage (t12-t0): At this stage the switch **Q6** is blocked. The capacitor **C6** charges itself from ***zero*** to ***E + Vcs*** and the capacitor **C5** discharges itself from ***E + Vcs*** to ***zero***. This stage finishes when the voltage across the capacitor **C5** reaches ***zero,*** and it is clamped by the diode **D5,** restarting the first operation stage.

IV. Mathematical Analysis of the Soft-Switching Circuit

To guarantee ZVS conditions, it is necessary, in the second stage, that the stored energy in the inductor **Ls** be sufficient to discharge the capacitor **C1, C3** and **C6** and to charge **Ca**. Thus, by inspection of Fig. 3 (Interval t1-t2) the following condition can be formulated:

$$LsIf^2 \geq (Ca + C1 + C3 + C6)(V + Vg)^2 \tag{1}$$

Where ***If*** is the maximum current in **Cs,** and ***Vcs*** is maintained constant during a switching period. Assuming ***Vcs<<E*** we have:

$$If\min \geq E\sqrt{\frac{Ca + C1 + C3 + C6}{Ls}} \tag{2}$$

It is necessary to know the clamping voltage behavior for the design of the switches and capacitor **Cs**.

In the steady state conditions the clamping capacitor average current must be zero. Thus:

$$iCs_{av} = \frac{1}{Ts}\left[\int_0^{t7}\left(\frac{Vcs}{Ls}\cdot t - 3Ir\right)dt + \int_{t7}^{t9}\left(\frac{Vcs}{Ls}\cdot t - 3Ir - Ic\right)dt + \right.$$

$$\left.\int_{t9}^{t11}\left(\frac{Vcs}{Ls}\cdot t - 3Ir - Ic - Ib\right)dt \int_{t11}^{t1}\left(\frac{Vcs}{Ls}\cdot t - 3Ir - Ic - Ib - Ia\right)dt\right] \tag{3}$$

Where **Ts** is the switching period.

Solving the integral equation, and considering:

$$D1 = \frac{t7}{Ts};\quad D3 = \frac{t9}{Ts};\quad D6 = \frac{t11}{Ts};\quad t1 \approx Ts;,\quad iCs_{av} = 0 \tag{4}$$

We have:

$$Vcs = \frac{2Ls}{Ts}[3\cdot Ir + Ia(2 - D1 - D6) + Ib(D1 - D3)] \tag{5}$$

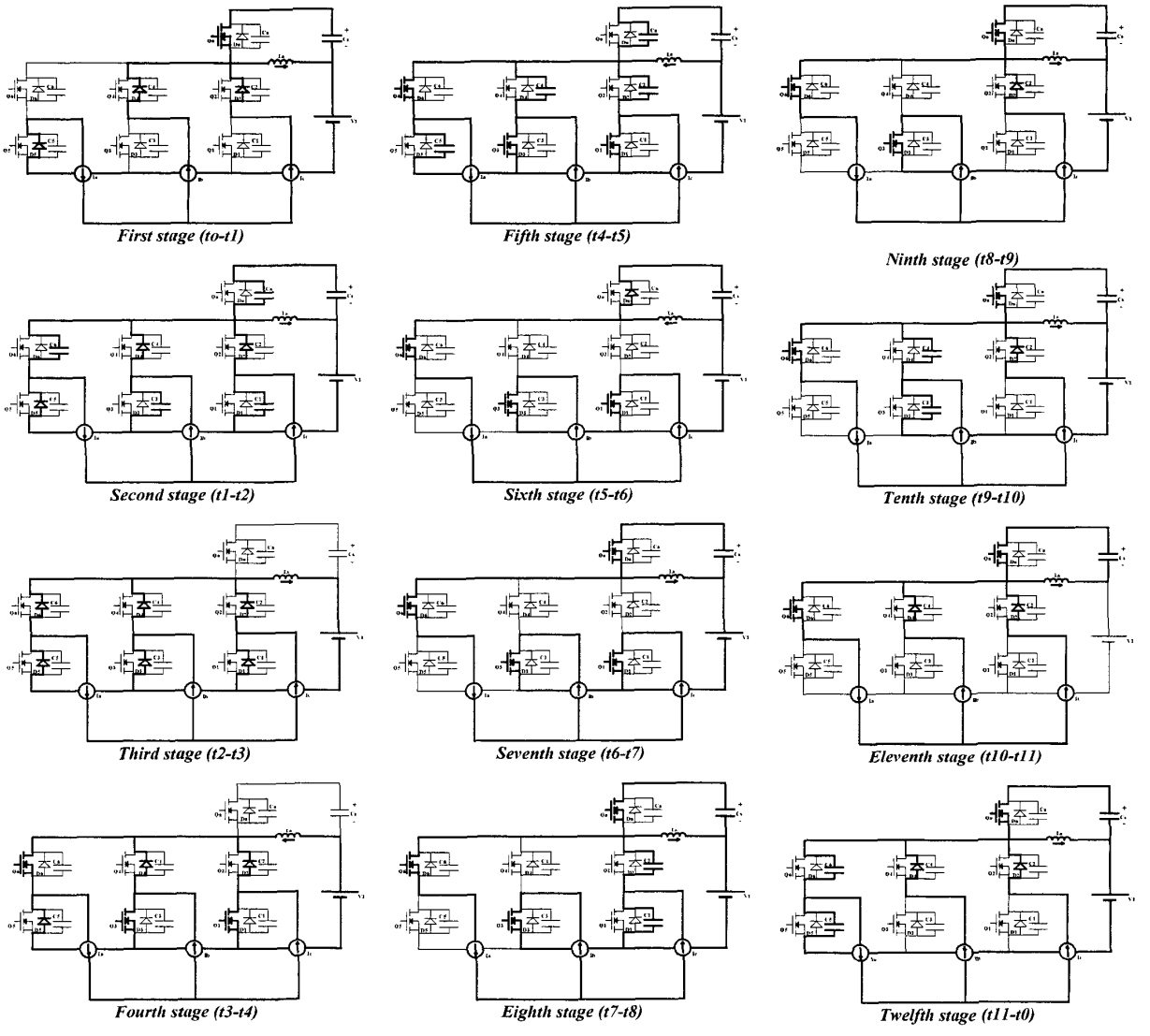

Fig. 2. Operation Stage

The output currents are given by:

$$Ia = \frac{E \cdot ma}{2 \cdot Zca} \cdot \operatorname{sen} \omega t \quad (6)$$

$$Ib = \frac{E \cdot ma}{2 \cdot Zcb} \cdot \operatorname{sen}\left(\omega t - \frac{2 \cdot \pi}{3}\right) \quad (7)$$

$$Ic = \frac{E \cdot ma}{2 \cdot Zcc} \cdot \operatorname{sen}\left(\omega t - \frac{4 \cdot \pi}{3}\right) \quad (8)$$

The load impedance are given by:

$$Zca = \sqrt{Rca^2 + (\omega \cdot Lca)^2} \quad (9)$$

$$Zcb = \sqrt{Rcb^2 + (\omega \cdot Lcb)^2} \quad (10)$$

$$Zcc = \sqrt{Rcc^2 + (\omega \cdot Lcc)^2} \quad (11)$$

Rca, Rcb e Rcc – Load resistances;

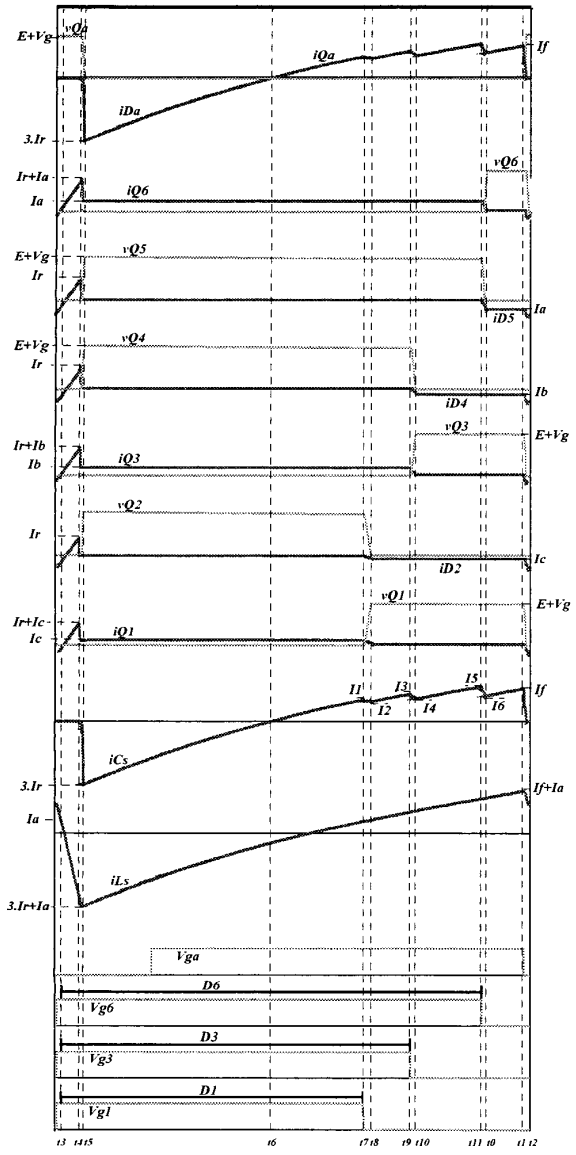

Fig. 3. Main waveforms

Lca, Lcb e Lcc – Load inductances

The duty cycle ***D*** can also be defined as:

$$D = ma \cdot sen\omega t \tag{12}$$

Where ***ma*** represents the modulation factor of amplitude.

From Eqs. 5 and 12 we obtain the expression of the ***Vcs*** voltage.

$$Vcs(t) = \frac{2 \cdot Ls}{Ts}\left[3 \cdot Ir + \frac{E \cdot ma}{Zca} \cdot \operatorname{sen}\omega t - \frac{E \cdot ma^2}{2 \cdot Zca} \cdot \operatorname{sen}^2 \omega t - \frac{E \cdot ma^2}{2 \cdot Zca} \cdot \operatorname{sen}\omega t \cdot \operatorname{sen}\left(\omega t - \frac{4 \cdot \pi}{3}\right) + \frac{E \cdot ma^2}{2 \cdot Zcb} \cdot \operatorname{sen}\omega t \cdot \operatorname{sen}\left(\omega t - \frac{2 \cdot \pi}{3}\right) - \frac{E \cdot ma^2}{2 \cdot Zcb} \cdot \operatorname{sen}^2\left(\omega t - \frac{2 \cdot \pi}{3}\right)\right] \tag{13}$$

Where ***Ir*** is the peak reverse recovery current of the anti-parallel diode, which can be given by:

$$Ir = \sqrt{\frac{4}{3} \cdot Qrr \cdot \frac{E}{Ls}} \tag{14}$$

Qrr – Reverse Recovery Charge

From the analysis of the current behavior in the capacitor **Cs**, the expression of the current ***If*** can be obtained:

$$If(t) = \frac{Vcs}{Ls} \cdot Ts - 2 \cdot Ia - 3 \cdot Ir \tag{15}$$

Combining Eq. 13 with Eq. 15 and making some simplifications we obtain the expression that represents the evolution of the current ***If***.

$$If(t) = 2 \cdot Ir + \frac{E \cdot ma}{Zca} \cdot \operatorname{sen}\omega t - \frac{E \cdot ma^2}{Zca} \cdot \operatorname{sen}^2 \omega t - \frac{E \cdot ma^2}{Zca} \cdot \operatorname{sen}\omega t \cdot \operatorname{sen}\left(\omega t - \frac{4 \cdot \pi}{3}\right) + \frac{E \cdot ma^2}{Zcb} \cdot \operatorname{sen}\omega t \cdot \operatorname{sen}\left(\omega t - \frac{2 \cdot \pi}{3}\right) - \frac{E \cdot ma^2}{Zcb} \cdot \operatorname{sen}^2\left(\omega t - \frac{2 \cdot \pi}{3}\right) \tag{16}$$

To guarantee ZVS condition in all load range the minimum value of the current ***If*** obtained from Eq. 16 must be bigger than the value obtained from Eq. 2.

V. Design Example

A. Input Data

E = 400V	Bus Voltage
Vout = 127 V	RMS Output Voltage
$Pout_{3\phi}$ = 12 kVA	Output Power
fs = 20KHz	Switching Frequency
f = 60Hz	Output Frequency
Lca = Lcb = Lcc = 575µH	Load Inductance
Rca = Rcb = Rcc = 4Ω	Load Resistance
ma=0,9	Modulation Factor

B. Calculation of the Auxiliary Inductor.

The auxiliary inductor is responsible for the di/dt limit during the turn off of the main diodes. The di/dt is directly related with the peak reverse recovery current ***Ir*** of the antiparallel diodes. A "snappy" di/dt produces a large amplitude voltage transient and contributes significantly to Electro-magnetic interference.

In the design procedure it is chosen a di/dt that is usually find in the diode data book. This is a simple way to obtain the diodes fundamental parameter for the design of the inverter. In such case the di/dt chosen for this example was 40A/us. Knowing that the current ramp rate is determined by the external circuit, thus:

$$Ls = \frac{E}{di/dt} = \frac{400V}{40\,A/\mu s} = 10\mu H \quad (17)$$

C. Load Impedance.

The load impedance is obtained from Eq. 18

$$Zout = \sqrt{4\Omega^2 + (2 \cdot \pi \cdot 60Hz \cdot 575mH)^2} \cong 4\Omega \quad (18)$$

D. Diode Choose.

For the performance of the inverter it is important to choose a slow diode. So, we opt to use the diode

SEMIKRON **SKKD 81/12**, which has the following characteristics:

Vrrm = 1.200V	Maximum Reverse Voltage
Ifav = 80A	Diode Average Current
Qrr = 120μC	Reverse Recovery Charge

E. Switching Period

$$Ts = \frac{1}{fs} = \frac{1}{20KHz} = 50\mu s \quad (19)$$

F. Reverse Recovery Current.

The reverse recovery current is given by the Eq. 20.

$$Ir = \sqrt{\frac{4}{3} \cdot 120\mu C \cdot \frac{400V}{10\mu H}} = 80A \quad (20)$$

G. Capacitor Clamping Voltage Behavior

Using a Eq. 13 the curves described in Fig. 4 are obtained.

For ma=0,9, the maximum clamping voltage is ***108V***.

We can observe that the voltage increment across the switches is too low.

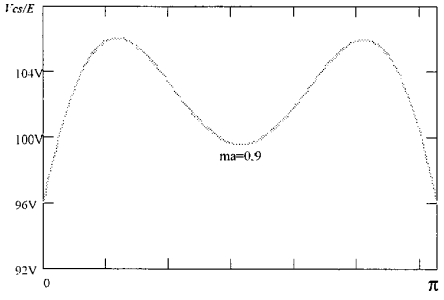

Fig 4. Capacitor Clamping Voltage Behavior

H. Current If Behavior.

The current ***If*** behavior, obtained from Eq. 2 and Eq.16, can be seen in Fig. 5.

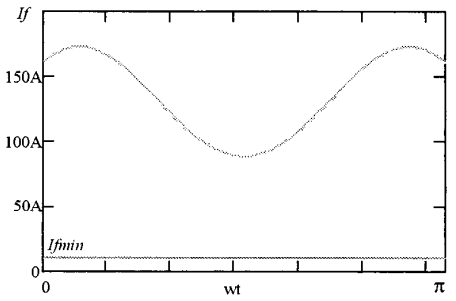

Fig. 5. Current ***If*** Behavior

VI. Experimental Results

An inverter prototype rated 12kVA operating with PWM commutation was built to evaluate the proposed circuit. The main specifications and components are given below:

A. Prototype Specifications

$Pout_{3\phi}$ = 12 kVA	(Output Power)
E = 400V	(Input Voltage)
Vout = 127V	(Rms Output Voltage)
f = 60Hz	(Output Frequency)
fs = 20 kHz	(Switching Frequency)
Switches	(IGBT GA250TS60U)
Diodes	(SKKD81/12)
Intrinsic Capacitance	1.5nF
Ls	(10uH each; Ferrite Core EE55/39; N=20 turns, 57 wires #22AWG)
Cs	(4 x 1000uF/350V; Electrolytic Capacitor)

B. Experimental Waveforms

In the figures presented below we can observe the experimental waveforms obtained from the laboratory prototype. **Figs. 6, 7** and **8** show the voltage and current in the switches. In **Fig. 9** it can be observed the current in the commutation auxiliary inductor for a switching period. The voltage across the clamping capacitor **Cs** is shown in **Fig. 10**. We can note a very low voltage across **Cs**. The output voltage and current are presented in **Fig. 11**. The efficiency of the converter at full load was about **96.5%.**

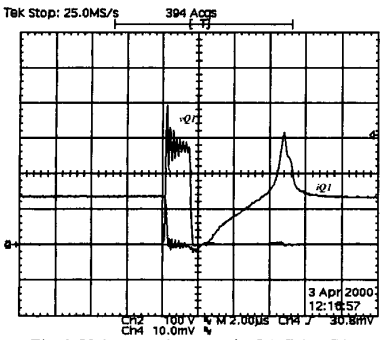

Fig 6. Voltage and current in Q1, D1 e C1

100V/div, 20A/div, 2us/div

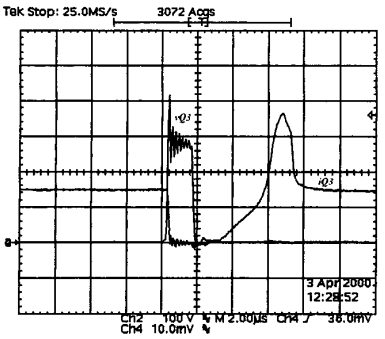

Fig 7. Voltage and current in Q3, D3 eC3

100V/div, 20A/div, 2us/div

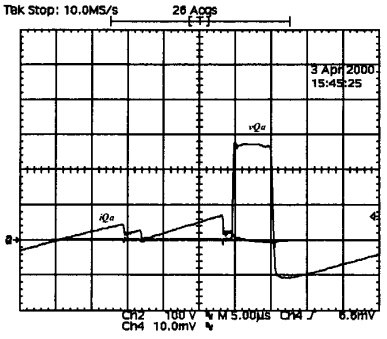

Fig 8. Voltage and current in Qa, Da e Ca

100V/div, 50A/div, 10us/div

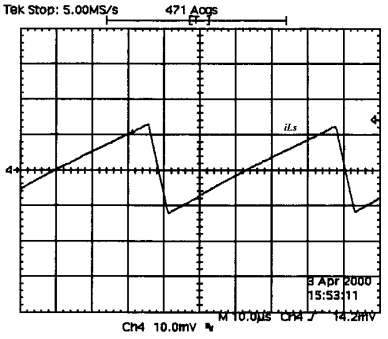

Fig 9. Current in Ls

50A/div, 10us/div

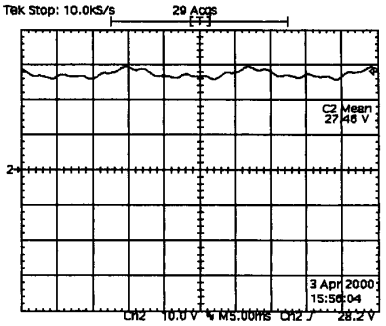

Fig 10. Voltage in Cs

10V/div, 5ms/div

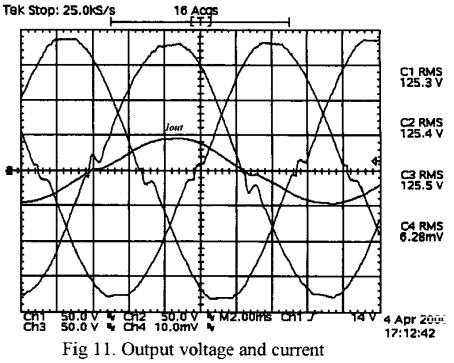

Fig 11. Output voltage and current

50V/div, 50A/div, 5ms/div

VII. CONCLUSIONS

A ZVS PWM Three-Phase Inverter with voltage clamping using a single auxiliary switch has been developed. The operation stages for steady-state condition, mathematical analysis, main waveforms and experimental results were presented. The experimental results show a low voltage in the clamping capacitor. Conduction and switching losses are reduced due to the implementation of the simple active snubber circuit, which provides ZVS conditions for all the switches, including the auxiliary one. The reduced number of components and the simplicity of the structure increase its efficiency and reliability, and make it suitable for practical applications. The proposed circuit presents soft commutation for all load range, confirming the theoretical studies.

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