A ZVS PWM Full-Bridge Inverter with Active Clamping Technique Using the Reverse Recovery Energy of the Diodes

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Abstract - **This paper presents a ZVS PWM Full Bridge Inverter with active voltage clamping technique that use the recovery energy of the diodes. The structure is particularly simple and robust because use only a single auxiliary switch. Switching losses are reduced due to implementation of the simple active snubber circuit that provides ZVS conditions for all switches, including the auxiliary one. It is very attractive for single-phase high power applications. Its main features are: Simple control strategy, robustness, lower weight and volume, lower harmonic distortion of the output current, and high efficiency. The principle of operation for steady-state conditions, mathematical analysis and experimental results from a laboratory prototype are presented.**

I. INTRODUCTION

With the appearance of the Bipolar Transistors in the 50s and posteriori the Mosfets in the 80s, PWM modulation techniques could be used together with the increase of the commutation frequency, with the aim to reduce the harmonic distortion in the output of the inverters. These measures give some benefits like the reduction of the volume and weight of the filters and magnetic elements; nevertheless they cause some difficulties due to the high commutation losses in the switches, that reduce the efficiency of the converter, and the electromagnetic interference appearing. This events occur mainly in inverter topologies that use the bridge configuration, where the main switch conduction provoke the reverse recovery phenomenon of the anti-parallel diode of the complementary switch.

A great number of works have been developed by power electronics scientific community, with the aim to diminish these problems. They can be divided in two groups: passive techniques [6, 7, 8, 9] and active techniques [1, 2, 3,10].

In the active technique area, some researches were made recently using the reverse-recovery energy from the diodes to obtain soft commutation in the switches of the pre-regulated rectifiers with high power factor [4, 5].

In this paper the analysis of a ZVS PWM full-bridge inverter with active clamping technique using the reverse recovery energy of the diodes to improve the efficiency of the converter, is presented.

This topology presents some advantages in comparison with the conventional soft commutation inverters studied in the literature, which we can print out:

- Soft commutation in all load range;
- Simple topology with a low number of components;
- Use a classical PWM modulation;
- Auxiliary switch works with constant duty cycle in all operation stages;
- Use of slow and low cost rectifiers diodes;
- Low clamping voltage across the capacitor;
- Low current stress through the main switches;
- Simple design procedure with low restrictions;
- High efficiency.

II. PROPOSED CIRCUIT

The proposed circuit is shown in Fig. 1. It presents a full bridge inverter configuration, where **Q1**, **Q2**, **Q3** and **Q4** are the main switches, and **Qa** is the auxiliary switch. **C1**, **C2**, **C3**, **C4** and **Ca** are the commutation capacitors.

The snubber circuit is formed by one controlled switch, **Qa**, with antiparallel diode **Da**, one small inductor **Ls** and one clamping capacitor **Cs**. The capacitor **Cs** is responsible by the storage of the diode reverse recovery energy and by the clamping of switches voltage. The inductor **Ls** is responsible by the control of the **di/dt** during the diode reverse recovery time. The auxiliary switch works with constant duty cycle in all operation stage. One of the most advantage of this converter consists in the use of only one auxiliary switch, which provides the clamping of the voltage and the ZVS conditions for all switches, including the auxiliary switch in the snubber circuit.

III. OPERATION STAGES (FOR THE FIRST HALF CYCLE)

The principle operation of both semicycle of the inverter load current is symmetrical. Thus, only for the first half cycle of the operation the circuit analysis will be made.

To simplify the analysis, the following assumptions are made: the operation of the circuit is steady state; the components are considered ideal; excluding the reverse recovery of the diodes **D1**, **D2**, **D3** and **D4**. The voltage across the capacitor **Cs**, and the current in the output inductor **Lc** are considered constant during the switching period. The parameter **E** represents the bus voltage, and **Vcs** is the voltage across the clamping capacitor **Cs**.

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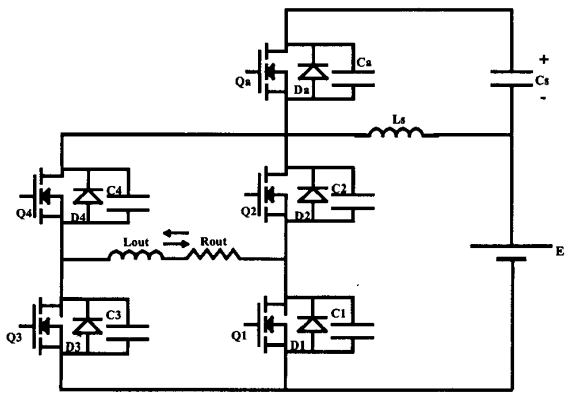


Fig. 1. Proposed Circuit.

In the following paragraphs the operation stage of the first positive half cycle of the output current is described in detail.

First stage (t0-t1): During this interval the output current ***Iout*** deliver energy to the source **E** via diodes **D1** and **D4**. At the same time, the additional current ***iLs*** flows around the mesh, formed by **Ls, Qa,** and **Cs.**

Second stage (t1-t2): This stage starts when the auxiliary switch **Qa** is blocked. The current ***iLs*** begins the charge of the capacitor **Ca** from **zero** to ***E+Vcs*** and discharges **C2** and **C3** from ***E+Vcs*** to ***zero***.

Third stage (t2-t3): At this stage the voltage across **C2** and **C3** reaches ***zero***, and it is clamping by the anti-parallel diodes **D2** and **D3.** So, the switches **Q2** and **Q3** conducts with ZVS condition. At this moment, the voltage is applied across the inductor **Ls** and the currents i***Ls*** decrease linearly

Fourth stage (t3-t4): It begins when the current ***iLs*** reaches *Iout* and flows through the switches **Q2** and **Q3**. The current ***iLs*** continues to decrease until inverting its direction of current of the diodes **D1** and **D4**, starting its reverse recovery phase. The inductor **Ls** limits the ***diLs/dt***. In the end this stage the current in **Ls** is equal to ***2Ir+Iout***.

Fifth stage (t4-t5): This stage starts when the diode **D1** and **D4** finishes its reverse recovery phase. The current ***iLs*** begins the charge of the capacitors **C1** and **C4** from ***zero*** to ***E + Vcs*** and the discharge of **Ca** from ***E + Vcs*** to ***zero***.

Sixth stage (t5-t6): At this stage the voltage across the capacitor **Ca** reaches ***zero***, and it is clamped by the diode **Da.** Thus, the auxiliary switch **Qa** conducts with zero-voltage switching. The current ***iLs*** increase, due the application of the voltage **Vcs** across the inductor **Ls**.This stage finishes when the current in **Cs** reaches ***zero***.

Seventh stage (t6-t7): This stage begins when the current ***iCs*** changes its direction and flows through the switch **Qa**. The current ***iLs*** continues to increase linearly.

Eighth stage (t7-t8): At this stage the switches **Q2** and **Q3** are blocked. The capacitors **C2** and **C3** charges itself from ***zero*** to ***E + Vcs*** and the capacitors **C1** and **C4** discharges itself from ***E + Vcs*** to ***zero***.

For the second half cycle the operation stage is analogous and can be described in an identical way.

The main waveforms are shown in Fig. 2, and Fig.3. shows the main operation stages.

IV. Mathematical Analysis of the Soft-Switching Circuit

To guarantee ZVS conditions, it is necessary, in the second stage, that the stored energy in the inductor **Ls** be sufficient to discharge the capacitors **C2** and **C3** and to charge **Ca**. Thus, by inspection of Fig. 3 (Interval t1-t2) the following condition can be formulated:

$$Lsif^2 \geq (Ca + C2 + C3)(E + Vcs)^2 \tag{1}$$

Where ***If*** is the maximum current in **Cs,** and ***Vcs*** is maintained constant during a switching period. Assuming ***Vcs<<E*** we have:

$$If\min \geq E\sqrt{\frac{C2 + C3 + Ca}{Ls}} \tag{2}$$

It is necessary to know the clamping voltage behavior for the design of the switches and capacitor **Cs.**

In the steady state conditions the clamping capacitor average current must be zero. Thus:

$$iCs_{mi} = \frac{1}{Ts}\left[\int_0^{t7}\left(\frac{Vcs}{Ls}\cdot t - 2Ir\right)dt + \int_{t7}^{t1}\left(\frac{Vcs}{Ls}\cdot t - 2Iout - 2Ir\right)dt\right] \tag{3}$$

Where **Ts** is the switching period.

Solving the integral equation, and considering:

$$D = \frac{t7}{Ts} \tag{4}$$

$$t1 \approx Ts \tag{5}$$

$$iCsav_{av} = 0 \tag{6}$$

We have:

$$Vcs = \frac{4\,Ls}{Ts}[Ir + Iout\ (1 - D)] \tag{7}$$

The output current is given by:

$$Iout = \frac{E \cdot ma}{Zout}\cdot \operatorname{sen}\omega t \tag{8}$$

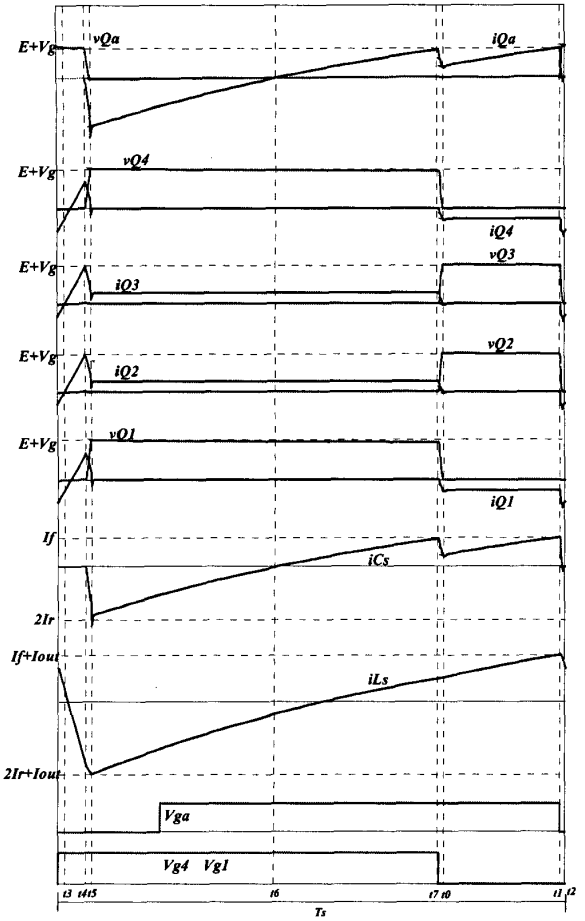


Fig. 2. Main Waveforms.

where ***Zout*** is the load impedance given by:

$$Zout = \sqrt{Rout^2 + (\omega \cdot Lout)^2} \tag{9}$$

Rout – Load resistance
Lc – Load inductance

The duty cycle ***D*** can also be defined as:

$$D = ma \cdot \sin\omega t \tag{10}$$

Where ***ma*** represent the modulation factor of amplitude.

Combining Eqs. 7, 8 and 10 we obtain the expression of the ***Vcs*** voltage.

$$Vcs(t) = \frac{4 \cdot Ls}{Ts}\left[Ir + \frac{E \cdot ma}{Zout} \cdot \sin\omega t \cdot (1 - ma \cdot \sin\omega t)\right] \tag{11}$$

Where ***Ir*** is the peak reverse recovery current of the anti-parallel diode, which can be given by:

$$Ir = \sqrt{\frac{4}{3} \cdot Qrr \cdot \frac{E}{Ls}} \tag{12}$$

Qrr – Reverse Recovery Charge

From the analysis of the current behavior in the capacitor **Cs** , the expression of the current ***If*** can be obtained :

$$If(t) = \frac{Vcs}{Ls} \cdot Ts - 2 \cdot Iout - 2 \cdot Ir \tag{13}$$

Combining Eq. 11 with Eq. 13 and making some simplifications we obtain the expression that represents the evolution of the current ***If***.

$$If(t) = 2 \cdot Ir + \frac{2 \cdot E \cdot ma}{Zout} \cdot \sin\omega t - \frac{4 \cdot E \cdot ma^2}{Zout} \cdot \sin^2\omega t \tag{14}$$

To guarantee ZVS condition in all load range the minimum value of the current ***If*** obtained from Eq. 14 must be bigger than the value obtained from Eq. 2.

V. Design Example

A. Input Data.

E = 200V	Bus Voltage;
Vout = 127 V	RMS Output Voltage;
Pout = 6 KVA	Output Power;
fs = 20KHz	Switching Frequency;
f = 60Hz	Output Frequency
Lout = 1 mH	Load Inductance;
Rout = 2,7Ω	Load Resistance;
ma=0,9	Modulation Factor.

B. Calculation of the Auxiliary Inductor.

The auxiliary inductor is responsible for the di/dt limit during the turn off of the main diodes. The di/dt is directly related
with the peak reverse recovery current ***Ir*** of the antiparallel diodes. A "snappy" di/dt produces a large amplitude voltage transient and contributes significantly to Electro-magnetic interference.

In the design procedure it is chosen a di/dt that is usually find in the diode data book. This is a simple way to obtain the diodes fundamental parameter for the design of the inverter. In such case the di/dt chosen for this example was 40A/us. Knowing that the current ramp rate is determined by the external circuit, thus:

$$Ls = \frac{E}{\frac{di}{dt}} = \frac{200V}{40\,A/\mu s} = 5\mu H \tag{15}$$

C. Load Impedance.

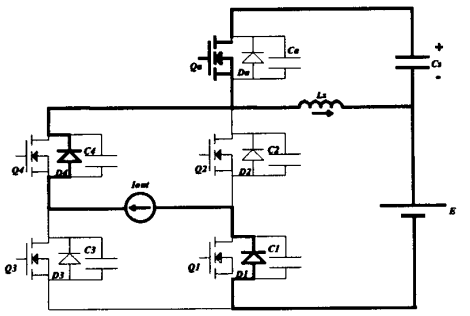
The load impedance is obtained from Eq. 16

$$Zout = \sqrt{2{,}7\Omega^2 + (2 \cdot \pi \cdot 60Hz \cdot 1mH)^2} \cong 2{,}7\Omega \tag{16}$$

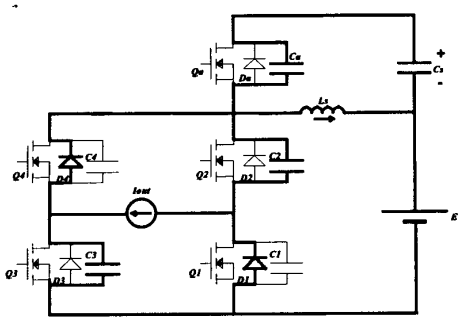
D. Diode Choose.

For the performance of the inverter it is important to choose a slow diode. So, we opt to use the diode SEMIKRON **SKKD 81/12**, which has the following characteristics:

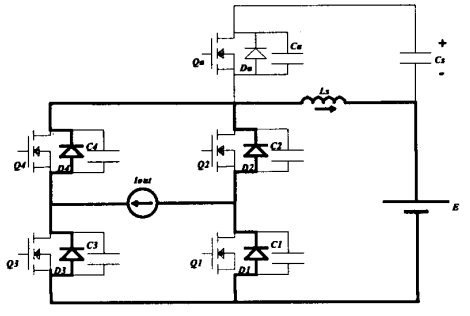
Vrrm = 1.200V	Maximum Reverse Voltage.
Ifav = 80A	Diode Average Current.
Qrr = 120μC	Reverse Recovery Charge.



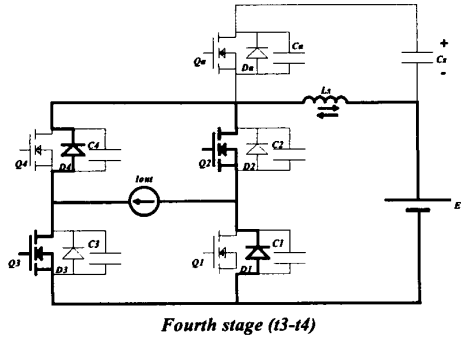
First stage (to-t1)



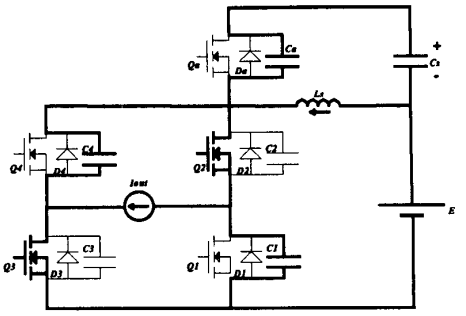
Second stage (t1-t2)



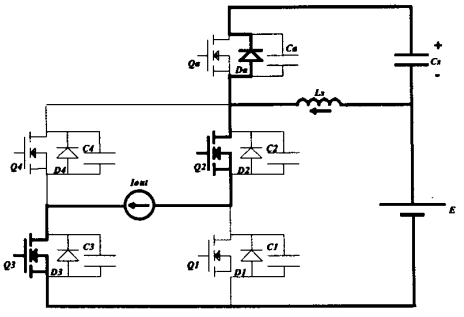
Third stage (t2-t3)



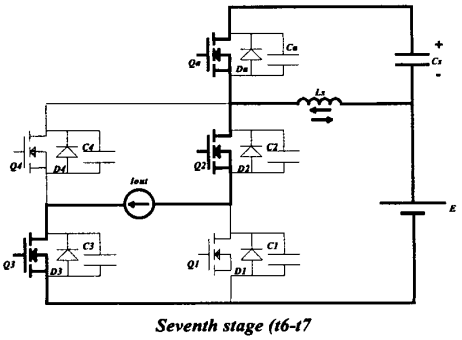
Fourth stage (t3-t4)



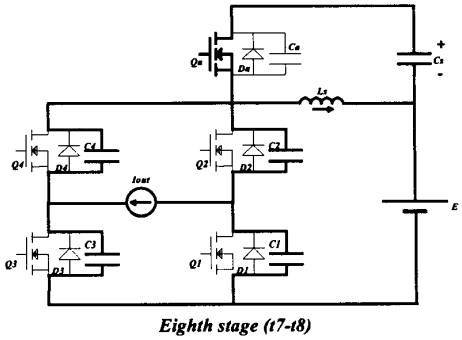
Fifth stage (t4-t5



Sixth stage (t5-t6)



Seventh stage (t6-t7



Eighth stage (t7-t8)

Fig. 3. Operation Stage

E. Switching Period.

$$Ts = \frac{1}{fs} = \frac{1}{20kHz} = 50\mu s \qquad (17)$$

F. Reverse Recovery Current.

The reverse recovery current is given by the Eq. 12.

$$Ir = \sqrt{\frac{4}{3} \cdot 60\mu C \cdot \frac{400V}{10\mu H}} = 56A \qquad (18)$$

G. Capacitor Clamping Voltage Behavior.

Using a Eq. 11 the curves described in Fig. 4 are obtained.

For ma=0,9, the maximum clamping voltage is ***42V***.

We can observe that the voltage increment across the switches is too low.

H. Current If Behavior.

The current ***If*** behavior, obtained from Eq.12 and Eq.14, can be seen in Fig. 5.

It is observed that the current ***If*** has a minimum point that is located in $\pi/2$, and the intensity of the current diminishes with the increase of the load. To guarantee ZVC condition in all range load, the minimum value of the current ***If***, obtained from Eq. 14, must be bigger than the value of the traced straight line from Eq. 12.

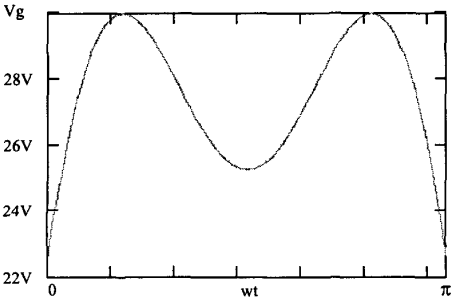


Fig 4. Capacitor Clamping Voltage Behavior

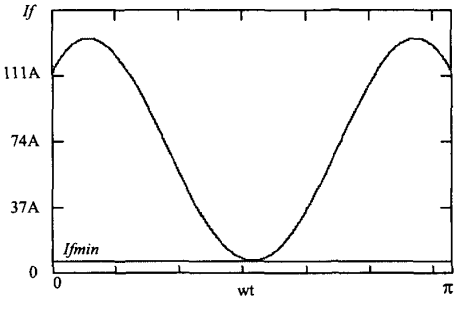


Fig. 5. Current ***If*** Behavior

VI. Experimental Results

An inverter prototype rated 6kW operating with PWM commutation was built to evaluate the proposed circuit. The main specifications and components are given below:

A. Prototype Specifications

Pout =	6000 W (Output Power)
E = 200V	(Input Voltage)
Vout = 127V	(Rms Output Voltage)
f = 60Hz	(Output Frequency)
fs = 20 kHz	(Switching Frequency)
Q1, Q2, Q3, Q4, Qa	(IGBT GA250TS60U)
D1, D2, D3, D4, Da	(SKKD81/12)
C1, C2, C3, C4, Ca	(Intrinsic Capacitance ≈1.5nF)
Ls	(Ferrite Core EE55/39)
Cs	(4 x 1000uF/350V)

B. Experimental Waveforms

In the figures presented below we can observe the experimental waveforms obtained from the laboratory prototype. Figs.6, and 7 show the voltage and current in the switches.

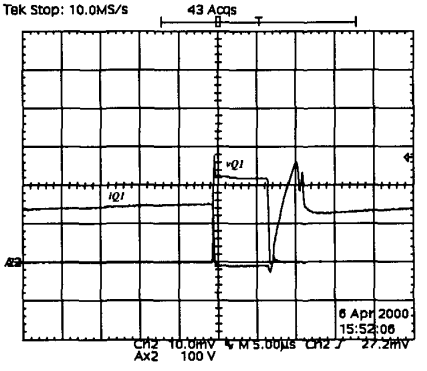


Fig. 6. Voltage and current in Q1, D1 e C1
100V/div, 20A/div, 5us/div

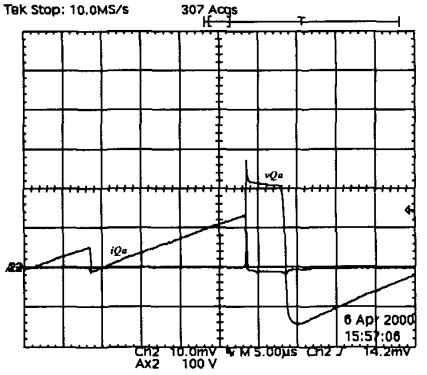


Fig. 7. Voltage and current in Qa, Da e Ca
100V/div, 50A/div, 5us/div

In Fig. 8 it can be observed the current in the commutation auxiliary inductor for a switching period.

The voltage across the clamping capacitor **Cs** is shown in Fig.9. We can note a very low voltage across **Cs**.

The output voltage and current are presented in Fig.10.

Fig. 11 show the efficiency as function of the load range.

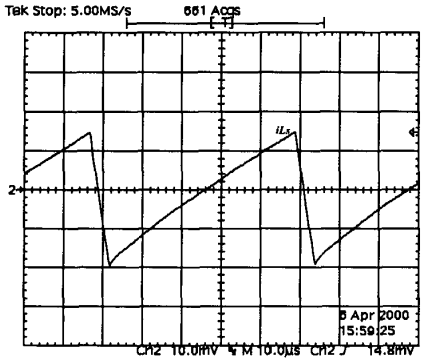


Fig. 8. Current in Ls
50A/div, 10us/div

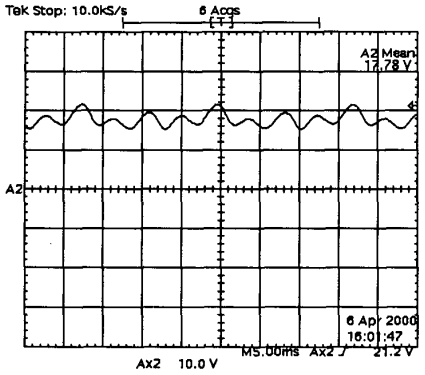


Fig. 9. Voltage in Cs
10V/div, 5ms/div

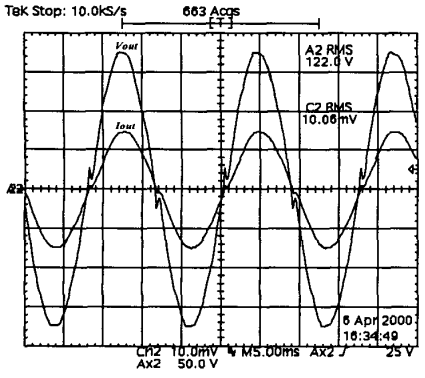


Fig. 10. Output voltage and current
50V/div, 50A/div, 5ms/div

VII. CONCLUSIONS

This paper shows a ZVS PWM full bridge inverter with active voltage clamping using the reverse recovery energy of the diodes. The operation stages for steady-state condition, mathematical analysis, main waveforms and experimental results were presented. The experimental results show a low voltage in the clamping capacitor. Switching losses are reduced due to the implementation of the simple active snubber circuit, that provides ZVS conditions for all the switches, including the auxiliary one. The reduced number of components and the simplicity of the structure increase its efficiency and reliability, and make it suitable for practical applications. The proposed circuit presents soft commutation for all load range, confirming the theoretical studies.

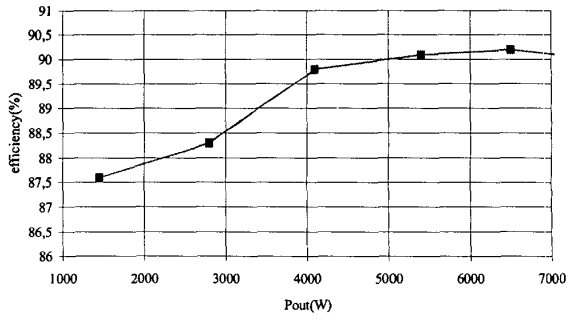


Fig. 11. Efficiency over the output range.

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