A NEW HIGH GAIN NON-ISOLATED DC-DC BOOST CONVERTER FOR PHOTOVOLTAIC APPLICATION

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***Abstract* – This paper introduces a new topology of the high gain non-isolated DC-DC boost converter with central point on its output. The proposed converter is derived from the quadratic single switch boost converter and the three level boost converter. The static gain of this converter is bigger than the one from the conventional boost converter and the maximum voltage on both switches is half of the output voltage. Qualitative and quantitative analysis of the operation stages, the main waveforms and the experimental results of a 520 W prototype are presented. The converter is aimed for modular photovoltaic application.**

***Keywords* - High gain DC-DC boost converter, quadratic boost converter, photovoltaic.**

I. INTRODUCTION

Photovoltaic (PV) power-generation systems are becoming increasingly important and prevalent in distribution generation systems. Unfortunately, the power capacity range of a single PV module is usually about 100 W to 300 W, and the maximum power point (MPP) voltage range is from 15 V to 40 V. These values are low when comparing with the required input voltage of inverters; making it difficult to reach high efficiency [1, 2].

In this case, the difference between the low voltage of PV modules and the required input voltage of inverters can be compensated by the connection of various PV modules in series. However, the generated output power of the PV arrays is decreased greatly due to module mismatch or partial shading, resulting in difficulties to reach the MPP for every PV panel or for whole and then reducing system efficiency.

Thus, the modular power conversion without galvanic isolation may be promising because it is less perturbed and it would allow an effective use of the energy available in the PV arrays, but its output voltage is low. Therefore, in this context, it is necessary to utilize a step-up DC-DC converter as intermediate stage between the PV array and the inverter.

Besides the isolated converters with transformer, the conventional boost converter is generally used in this application. But, its voltage gain is limited due to the losses associated with inductor, filter capacitor, rectifier diodes and the main power switch when operating with extreme duty cycle [3, 4].

To extend the range of voltage conversion [5, 6] proposes the use of the cascade boost converters, because its voltage gain is higher with quadratic characteristic as a function of duty cycle. However, its structure becomes bulky and the voltage stress across the switch is high. Using the similar technique, in [7, 8] the high gain converters with coupled inductors are introduced. By using the coupled inductor, it is possible to obtain high static gain by a properly choosing the windings ratio [12]. The switch voltage stress is suppressed and reverse recovery of the output diode is alleviated. But, the voltage across the output diode remains high and the resonance between the leakage inductance and parasitic capacitor of the output diode cause electromagnetic interference problem and increases losses. Furthermore, the input current ripple is high due to the discontinuity of the current.

By applying the three-level switching cell to the single switch boost converter [9, 10] proposed a quadratic converter. In this converter the blocking voltage of the switches is a fraction of the output voltage. It this capable of equally sharing the switches' voltages if the voltage gain is smaller than 4.

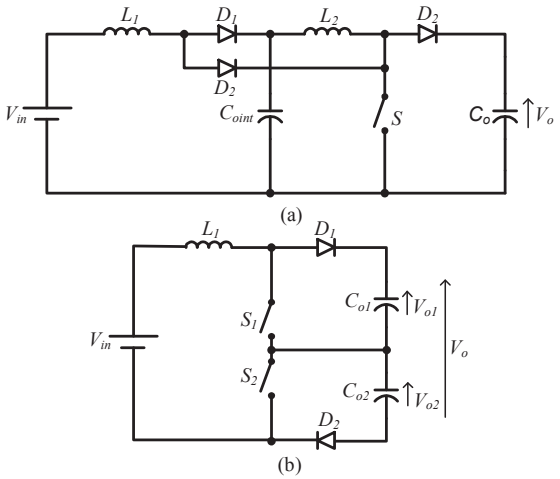

Fig. 1 Single switch quadratic boost converter (a) and three level boost converter (b)

This paper proposes a new topology of the high gain non-isolated DC-DC boost converter. The proposed converter is a topology obtained from the single switch quadratic boost converter Figure 1 (a) and the three-level boost converter Figure 1(b), presented in [6, 11], respectively. Figure 2 shows the topology of the proposed converter. This converter has quadratic static gain as a function of duty cycle, and the maximum voltage on both switches is half of the output voltage. Moreover, the output voltage is balanced, to avoid destruction of the switches and to allow the connection of inverters with capacitive voltage divider such as NPC, half bridge and so on. In contrast, the current conducted by the switches is high; therefore, it is the sum of the current of both inductors. Furthermore, in terms of control, this topology presents a high order transfer function that increases its complexity, and also requires an additional loop to balance the voltage of both filter capacitors [13].

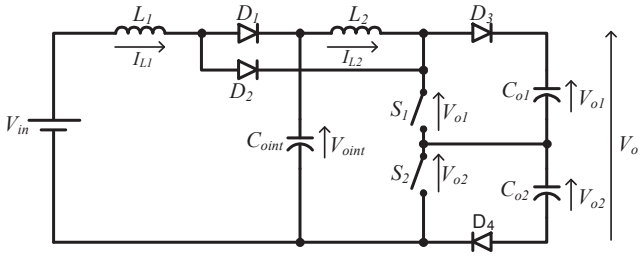

Fig. 2 Proposed topology

II. PRINCIPLE OF OPERATION

The modulation strategy adopted for the proposed converter is a phase shift PWM modulation. This strategy of modulation results in two pulses of command delayed by 180º as shown in Figure 4 and 6.

To explain the principle of operation and analyze theoretically the proposed topology, the continuity of the current in both inductors is considered. In this paper only the CCM operation in both inductors will be presented. The complete analyzes with different modes of operation already derived, but shall be dealt with detail in other paper. Moreover, the converter is investigated for two regions defined by the values of the duty cycle (D < 0.5 and D > 0.5).

A. CCM operation for D < 0.5(Rev1_3)

The operation stages in CCM for D < 0.5 are described below. The topological states and the main waveforms of the four stages of operation are illustrated in Figure 3 and Figure 4, respectively.

- **Stage 1 ($t_0 - t_1$)** – Figure 3(a): S_1 and S_2 are blocked and the current of both inductors decreases linearly. The energy is being delivered from the power supply to the load.
- **Stage 2 ($t_1 - t_2$)** – Figure 3 (b): It starts when S_2 is turned on, and the energy is accumulated in the inductors L_1 and L_2.
- **Stage 3 ($t_2 - t_3$)** – Figure 3 (a): This stage of operation starts when S_2 is commanded to turn off. The topological state and the principle of operation of this stage are equal to the first stage of operation.
- **Stage 4 ($t_3 - t_4$)** – Figure 3 (c): In this stage of operation, S_1 is commanded to turn on and the energy is being transferred from the input power source to the load.

By inspection the main waveforms of the operation stages shown in Figure 4, it is possible to determine the time intervals of each operation stage. The relationship between the time intervals of each stage of operation as a function of the duty cycle are given by (1) and (2).

$$\Delta t_1 = \Delta t_4 = \frac{T.(1-2.D)}{2} \quad (1)$$

$$\Delta t_2 = \Delta t_5 = D.T \quad (2)$$

Where:

Δ_{t1} to Δ_{t5} – Time intervals of the four stage of operation
D - Duty cycle
T - Switching period

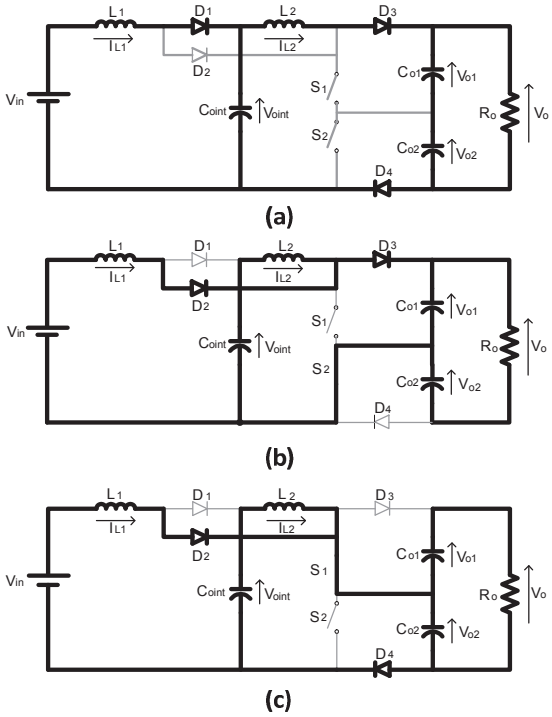

Fig. 3 Topological states of the proposed converter in CCM for D < 0,5

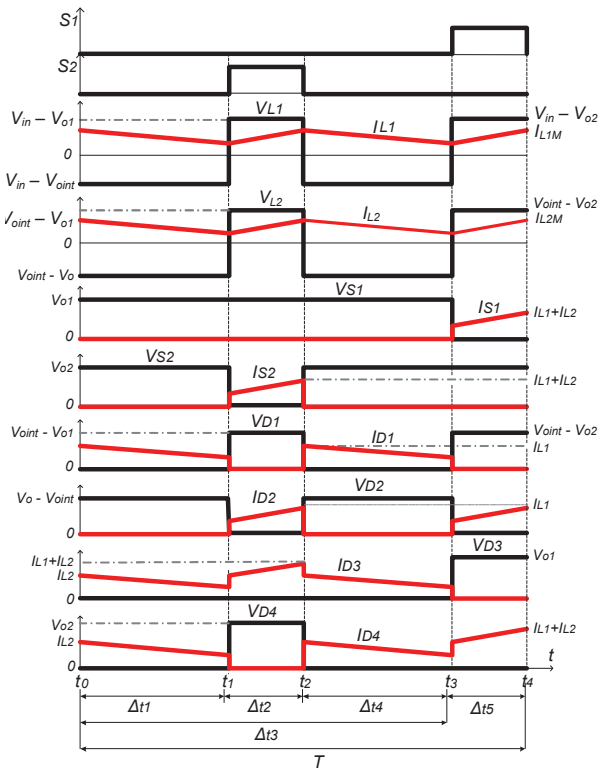

Fig. 4 Main waveforms of the operation stages in CCM for D < 0.5

B. CCM operation for D > 0.5

The four operation stages of the converter in CCM for D > 0.5 are presented below. The topological states and the main waveforms of the operation stages are illustrated in Figure 5 and Figure 6, respectively.

- **Stage 1 ($t_0 - t_1$)** – Figure 5(a): S_1 and S_2 are conducting simultaneously, starting the accumulation of energy in

the inductors L_1 and L_2. The capacitors C_{o1} and C_{o2} deliver energy to the load.

- **Stage 2 ($t_1 - t_2$)** – Figure 5 (b): It starts when S_2 is turned off. The energy is being transferred from input power source to the load. The voltage across S_2 is equal to $V_o/2$.
- **Stage 3 ($t_2 - t_3$)** – Figure 5 (a): In this stage the S_2 is commanded to turn on again. The topological state and the principle of operation of this stage are equal to the first stage of operation.
- **Stage 4 ($t_3 - t_4$)** – Figure 5 (c): This stage starts when S_1 is turned off and the energy is being delivered to the load. The voltage across S_1 is equal to $V_o/2$.

According to the main waveforms illustrated in Figure 6, the relationship between time intervals of each stage of operation as a function of the duty cycle can be defined in (3) and (4).

$$\Delta t_1 = \Delta t_4 = \frac{T.(2.D-1)}{2} \quad (3)$$

$$\Delta t_2 = \Delta t_5 = T.(1-D) \quad (4)$$

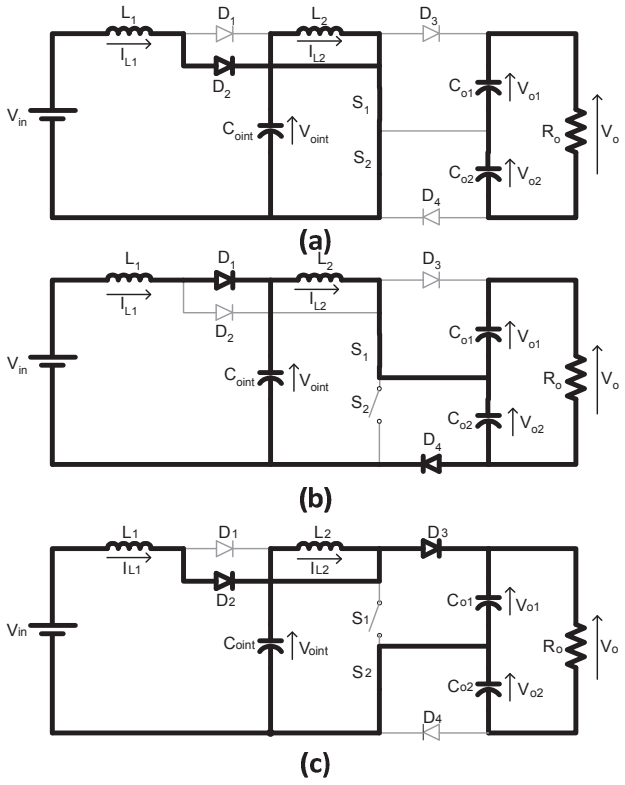

Fig. 5 Topological states of the proposed converter in CCM for D > 0.5

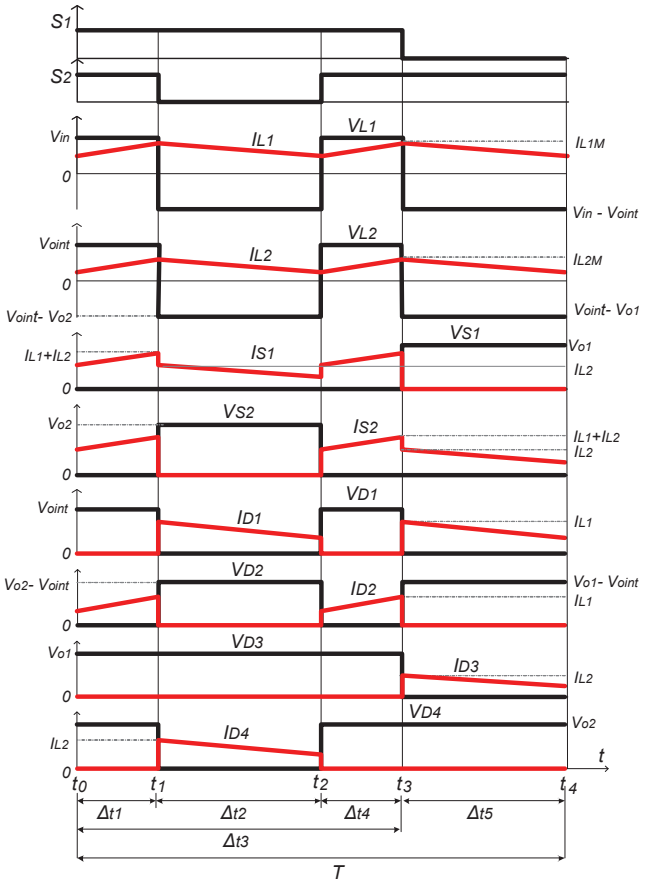

Fig. 6 Main waveforms of the operation stages in CCM for D > 0.5

III. STATIC ANALYSIS

To analyze the steady state characteristics of the proposed converter in CCM, it is assumed that all power devices are ideal and all capacitors are extremely large to ensure the constant output voltage.

The ideal static gain of this proposed converter is obtained by calculating the average voltage of the inductors L1 and L2. To calculate the static gain, each step-up stage can be analyzed separately, as follows. In steady state the average voltage across L1 is equal to zero as shown in (5). Vin is the input voltage and Voint is the intermediary DC link voltage. The static gain between the intermediary DC link and the input voltage is determined by (6). Considering the same procedure, the static gain for the second step-up stage can be calculated as given by (7) and (8), where Vo is the output voltage of converter.

By multiplying (6) by (8), the total static gain for D < 0.5 can be obtained as shown in (9).

$$2.\Delta t_1.(V_{in} - V_{oint}) + \Delta t_2.(V_{in} - V_o) = 0 \quad (5)$$

$$\frac{V_{oint}}{V_{in}} = \frac{1-D}{2.D^2 - 2.D + 1} \quad (6)$$

$$2.\Delta t_1.(V_{oint} - V_o) + \Delta t_2.(V_{oint} - V_o) = 0 \quad (7)$$

$$\frac{V_o}{V_{oint}} = \frac{1}{1-D} \quad (8)$$

$$G_{CCM(D<0,5)} = \frac{V_{oint}}{V_{in}}.\frac{V_o}{V_{oint}} = \frac{1}{2.D^2 - 2.D + 1} \quad (9)$$

The static gain of the converter in CCM for D > 0.5 can also be obtained by analyzing individually each stage of

conversion. Following the same procedure as in the previous case, partial static gains of the first and second stage of the converter are given by (10) and (11). By multiplying (10) by (11), it is possible to obtain the total static as shown in (12).

$$\frac{V_{oint}}{V_{in}} = \frac{1}{2(1-D)} \quad (10)$$

$$\frac{V_o}{V_{oint}} = \frac{1}{(1-D)} \quad (11)$$

$$G_{CCM(D>0,5)} = \frac{1}{2.(1-D)^2} \quad (12)$$

It is interesting to notice in (7) and (12) that the total static gain of the proposed converter for both regions of operation presents a quadratic characteristic. Moreover, the total static gain for D > 0.5 is half of the total static gain of the other quadratic converters presented previously in the introduction. Figure 7 shows a comparison of static gains between the proposed converter, the single switch quadratic boost converter and the conventional boost converter, all operating in CCM. The proposed converter presents static gain smaller than single switch quadratic boost converters. However, for the same static gain, the proposed converter can be better controlled than cascade boost converter, because the increment of the static gain is smoother. The static gain of proposed topology is always greater than the static gain of the conventional boost that allow to obtain a higher output voltages by using the smaller duty cycles, which results in better utilization of the switches.

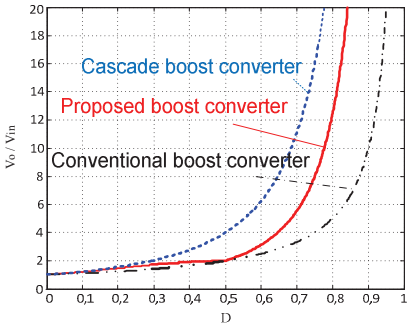

Fig. 7 Comparison of static gains between the proposed converter, the single switch quadratic boost converter and conventional boost converter

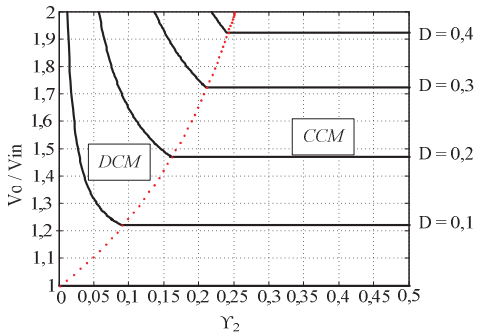

Fig. 8 External characteristics of proposed converter for $D < 0.5$

From the evaluation in discontinuous conduction mode (DCM) of proposed converter is yielded the external characteristic graph, and it is presented in Figure 8 and 9, respectively. The continuous line depicts the converter's output characteristic and the dashed line shows the boundary between mode of operation. The current parameterized is represented by Υ2. The equations are not shown due to digest size limitation.

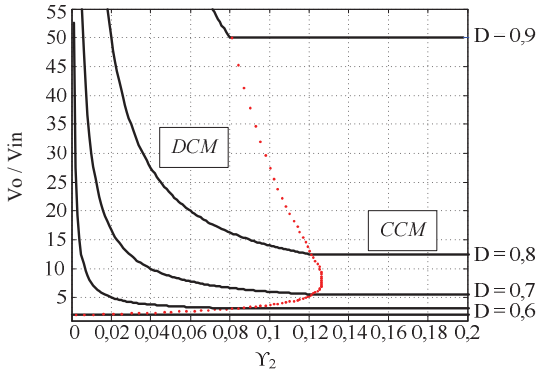

Fig. 9 External characteristics of proposed converter for $D > 0.5$

For a given value of the current ripple (ΔI_L), the duty cycle (D) and the switching frequency (f), it is possible to calculate the inductances of L_1 and L_2, which are given by (13) to (16).

$$L_{1(D<0,5)} = \frac{V_o.[4.D^3 - 4.D^2 + D]}{2.\Delta I_{L1}.f} \quad (13)$$

$$L_{2(D<0,5)} = \frac{V_o.[D.(1-2.D)]}{2.\Delta I_{L2}.f} \quad (14)$$

$$L_{1(D>0,5)} = \frac{V_o.[(1-D)^2.(2.D-1)]}{\Delta I_{L1}.f} \quad (15)$$

$$L_{2(D>0,5)} = \frac{V_o.[(1-D).(2.D-1)]}{2.\Delta I_{L2}.f} \quad (16)$$

The normalized current ripple ($\overline{\Delta I_L}$) of L_1 and L_2 for both regions of operation is represented by (17), (18), (19) and (20). The Figures 10 show the normalized current ripple of L_1 and L_2 as a function of duty cycle.

Analysis for D < 0.5

$$\Delta I_{L1}.\frac{L_1.f}{R_0} = \frac{(4.D^3 - 4.D^2 + D).(2.D^2 - 2.D + 1)}{2} \quad (17)$$

$$\Delta I_{L2}.\frac{L_2.f}{R_0} = \frac{D.(1-2.D)}{2} \quad (18)$$

Analysis for D > 0.5

$$\Delta I_{L1}.\frac{L_1.f}{R_0} = 2.(1-D)^4.(2.D-1) \quad (19)$$

$$\Delta I_{L2}.\frac{L_2.f}{R_0} = \frac{(1-D).(2.D-1)}{2} \quad (20)$$

The capacitances of the capacitors Coint, Co1 and Co2 can be calculated with a determined voltage ripple (ΔVC), as shown in (21) and (22).

$$\Delta V_{Coint} = \frac{2.I_o.(V_{oint} - V_{in})}{C_{oint}.f.V_{in}} \quad (21)$$

$$\Delta V_{Co1} = \Delta V_{Co2} = \frac{I_o.(2.V_{Co1} - V_{oint})}{2.C_{o1}.f.V_{Co1}} \quad (22)$$

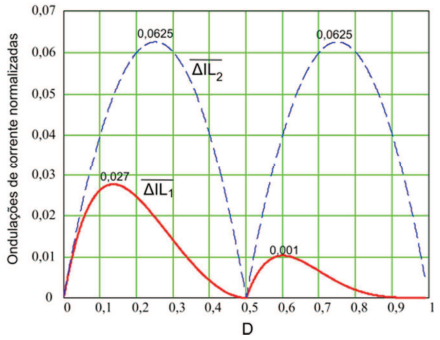

Fig. 10 Normalized current ripple of the inductor L_1 and L_2

IV. EXPERIMENTAL RESULTS

In order to validate the operation principle and to verify the performance of the proposed converter, a prototype of 520W was constructed in laboratory using the parameters shown in Table I. The power and input voltage are equivalent to the series and parallel combination of 4 PV modules of 130W and 17V. The converter has been modeled and controlled by three loops. A current loop controlled L_1 current and two voltage loops, one for the total voltage and another to keep the capacitors balancing. The control analysis will not be presented here due to its size but will be the goal of another paper.

The values of the inductors and capacitors are calculated using the expressions (15), (16), (21) and (22) considering that D=0.78, $\Delta I_{L1(max)}=\Delta I_{L2(max)}=20\%$ and $\Delta V_{oint}=\Delta V_o=1\%$.

TABLE 1
Parameters of proposed converter

Parameters	Values
Vin	34 V
Vo	380 V
Po	520 W
f	50 kHz
L1	60µH
L2	169µH
Coint	940µF/250V
Co1 e Co2	330µF/450V
D1, D2, D3 e D4	HFA15PB60
S1 e S2	IXFR90N30

Experimental results are being presented by Figure 11. Figure 11 (a) shows the waveforms of the input voltage and input current. Note that the input voltage is around 34V. The average input current is approximately 15A and the current ripple is 9%.

In Figure 11 (b) are shown the waveforms of intermediary DC link voltage and intermediary current. Observe that the intermediary DC link voltage is approximately 80V, while the average current of L_2 is 6.5A. The intermediary current ripple is 12%.

Figure 11 (c) shows the voltage across the switches S_1 and S_2. Note that the voltage of each switch is half of the output voltage, which is approximately equal to 190V. However, in Figure 11 (d) are presented the waveforms of the voltage across the diodes D_3 and D_4. Since the maximum reverse voltage of each diode is equal to half of the output voltage.

In Figure 11 (e) are illustrated the voltage of C_{o1} and C_{o2}. The voltage across each capacitor is also equal to half of output voltage. Figure 11 (f) shows the output voltage and the output current of the converter. The output voltage rated is approximately 380V and the output current is approximately 1,3A.

Figure 13 shows the commutation waveforms of the switch S_1. It is possible to observe the influence of the diode reverse recovery to the current of the switch. In Figure 12 is shown the efficiency of the proposed converter as a function of the output power. The proposed converter has achieved its highest efficiency in 350W output power level, while for the output rated power its efficiency is 89%. This efficiency could be increased using a commutation auxiliary circuit. However, in this work it was not used any kind of commutation auxiliary circuit.

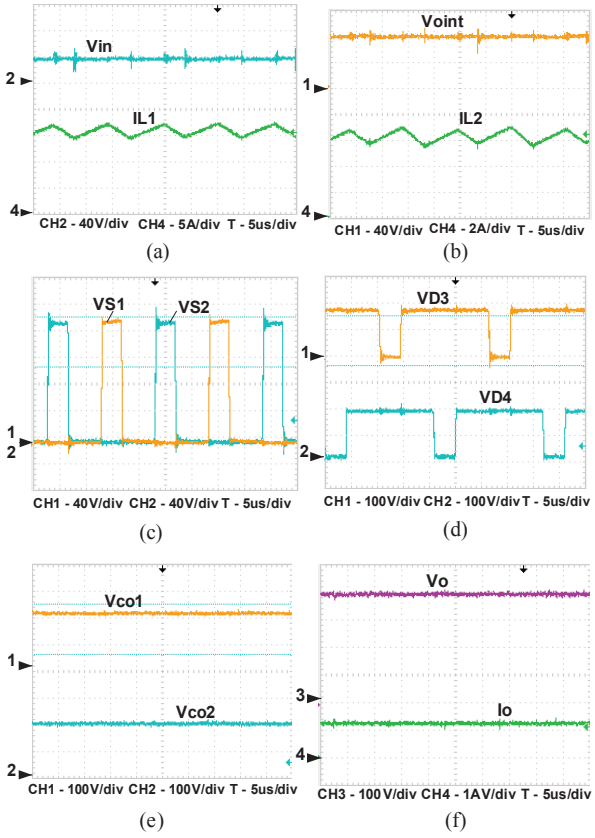

Fig. 11 Experimental result waveforms

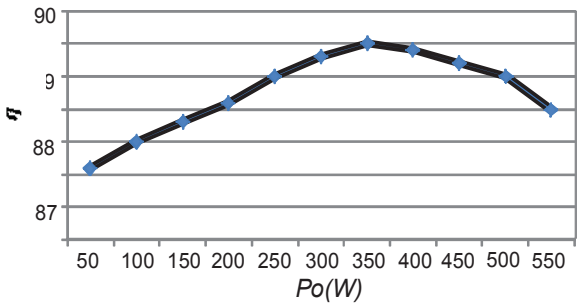

Fig. 12 Measured efficiency of the proposed converter

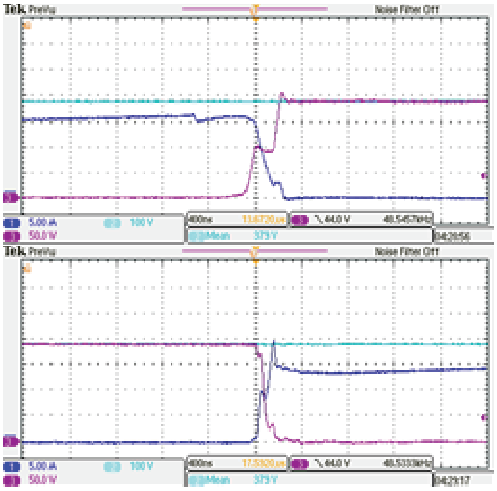

Fig. 13 Commutation waveforms of the switch S_1

V. CONCLUSIONS

From the theoretical analysis and experimental study in the laboratory we can draw the following conclusions:

An alternative topology is presented to obtain a high step-up voltage gain for non-isolated DC-DC converter which is a derivative of the single switch quadratic boost and three level boost converters.

The main advantage of the proposed converter is that the voltage stresses across the switches is limited to the half of the output voltage. Moreover, the voltage on capacitors C_{o1} and C_{o2}, being actively balanced, allows the connection of inverters with capacitive divider, which by itself reduces common mode current circulation through the grid.

Despite the efficiency results were not great; one must consider that the switching frequency could be reduced and the converter specifications were for low input voltage and consequently high current, therefore they are better applicable in low power, which usually results in lower efficiency converters. The most of quadratic converters have a low efficiency, because of the cascading. In this case, the converter has two stages. Besides that, in a PV system, the whole efficiency should be computed since when a modular system is considered, some gain on the MPPT efficiency might be achieved.

The presented converter can be interesting for applications where a high voltage ratio and high output power are necessary, what may be the case of clean energy source applications, but only when transformer isolation is not required.

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