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Single-Phase Non-Isolated Interleaved DCM Boost Rectifier With High Power Factor and ZVS Based on TAIPEI Rectifier

Rodrigo Heinrich[1] | Yales Romulo de Novaes[1] | Sergio Vidal Garcia Oliveira[1,2]

[1]Electrical Engineering Department, Universidade do Estado de Santa Catarina (UDESC), Santa Catarina, Brazil | [2]Electrical Engineering Department, Universidade Regional de Blumenau (FURB), Santa Catarina, Brazil

Correspondence: Rodrigo Heinrich (rodrigo.heinrich@edu.udesc.br)

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ABSTRACT

This paper proposes modifying the Taipei rectifier into a single-phase version and analysing its advantages as a single-stage rectifier for single-phase high-power electro-domestic applications. The rectifier utilizes two boost cells operating in discontinuous-conduction mode, separated by a virtual neutral. Frequency modulation is applied to switch-on the transistors with zero-voltage-switching and maintain a balanced voltage at the output capacitors. The virtual neutral, along with a coupled inductor, allows the use of low-rating electrolytic capacitors at the DC bus and increases common-mode noise immunity. The interleaved cells ensure a continuous input current and work as voltage followers without requiring a current control loop. There are no reverse recovery losses, and the body diode of the adjacent cell's switch is utilized as a boost diode, thereby sparing two components and enabling synchronous rectification. The topology operation stages and their features are studied and compared with similar power-factor-correction single-phase rectifiers. Additionally, the equations required to design the power components are introduced and validated in a 3 kW prototype, with a minimum switching frequency of 50 kHz, input and output voltages of 220 and 385 V, respectively. At rated conditions, the topology complies with IEC 61000-3-2, achieving a total efficiency of 92.52%.

1 | Introduction

Most of the rectifiers are designed to comply with power quality standards like IEC 61000-3-2/4 or IEEE 519-2022 that limit the device harmonic distortion to improve power-factor-correction (PFC), so to obtain better results manufacturers constantly seek for new technologies, optimized methodologies, or enhanced topologies.

Among the three-phase power converter rectifiers, a new topology, named the TAIPEI rectifier, is introduced in [1], which operates in discontinuous-conduction mode (DCM) and is based on a Boost converter. It achieves a total harmonic distortion (THD) below 5% and efficiency up to 97% in a 2.8 kW prototype operating at 20 kHz with 380 V_{RMS} line-to-line voltage. Figure 1 illustrates the rectifier composed of only two transistors that switch on with zero-voltage-switching (ZVS), thereby reducing the switching loss that is more detrimental in DCM converters. The input current is continuous due to the ripple cancellation of the three interleaved inductors, so the input electromagnetic interference (EMI) filter is not as bulky as other DCM converters. The inductor current follows the sinusoidal input voltage, then only the output voltage is controlled, the switches are commanded with frequency modulation (FM), keeping a fixed duty cycle of 50% to ensure switch-on with ZVS. Typically, three-phase rectifiers with a few switches are not efficient because they cannot independently shape each phase current into a sinusoidal waveform, so topologies with multiple switches or complex controllers are adopted [2–5]. Hence, the results obtained with the TAIPEI rectifier are impressive, making it an attractive option for PFC applications due to its simple topology and control circuit [6–10].

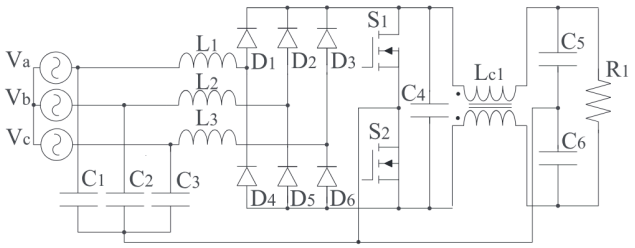

FIGURE 1 | Topology of three-phase TAIPEI rectifier applied to power factor correction.

Although the TAIPEI rectifier was first designed for three-phase systems, it is also interesting for single-phase applications. In [11, 12], the authors modify the Taipei rectifier into a single-phase topology to employ in aviation applications. In these systems, where the line frequency is up to 800 Hz, DCM converters are an attractive alternative to maintain sinusoidal input current shaping without a current controller, which would require a minimum bandwidth of around 50 kHz. The tests made with a 320 W prototype achieve 3.3% THD and comply with the DO-160 standard, and an efficiency of 95.2% at rated conditions with input voltage of 115 V.

In the scope of electrodomestic single-phase power supplies, where the line frequency is much lower, varying between 50 and 60 Hz the boost converter [13] operating in continuous conduction mode (CCM) is the most conventional solution in low-power applications until a few kilowatts [14], achieving low THD and practically unitary power factor using few components. However, conduction and diode reverse recovery losses are high [15], accounting for most of the rectifier's total losses. The control circuit is complex, comprising a slow loop to regulate the output voltage and an additional, faster loop to control the inductor current, thereby emulating a resistive load with a sinusoidal shape at the input to achieve a high power factor.

The continuous enhancements in semiconductor technology [16–21] enable manufacturers to handle better problems such as switching loss and current spikes, making the DCM boost converter (BDCM) competitive in the industry [22]. The control circuit is simpler than that of CCM converters [23], typically requiring only one slow loop to control the output voltage [24], as the discontinuous inductor current already has a sinusoidal shape. Converters operating in DCM use smaller inductors, resulting in an overall reduction in size and weight of the converter [25]. The disadvantage is the high and discontinuous input current ripple that requires a bulky input filter to eliminate high-frequency harmonics.

One way to overcome the problem of current efforts in DCM converters and improve input current distortion is by replicating the converter in smaller cells that operate in interleaved mode along a switching cycle, as exemplified in [26–34]. According to [35], an interleaved DCM boost (BIDCM) rectifier with variable frequency modulation achieves similar efficiency to a conventional ZVS boost rectifier. Interleaved boost topologies with DCM cells have continuous input current because part of the inductor current ripple from one cell is cancelled by the others [36]; according to [37], the input current ripple is reduced by 14.7% in a boost DCM with two cells operating with duty cycle modulation and 29.2% when operating with frequency modulation, by employing three cells these values are even more reduced to 8.5% and 11%, respectively.

In [38], a new DCM interleaved boost topology with two cells is introduced, named the Nabae rectifier. It utilizes a capacitor divider on the alternating current (AC) side to create a virtual neutral, which divides both cells and enhances the common mode noise immunity. The switches are controlled by frequency modulation because it is necessary to have a fixed duty cycle of 50% to switch-on with ZVS. The input current is continuous, and the ripple has double the switching frequency. The converter has two fewer diodes because the MOSFET body diode of the adjacent cell works as the boost diode. The paper made experiments with a 75 W prototype operating at 10 kHz with an input voltage of 100 V and output voltage of 200 V without using an input EMI filter and achieved a THD of 6.03%.

In [39], the Nabae rectifier is modified by relocating the input capacitor divider to the direct current (DC) side, allowing the use of electrolytic capacitors. This is an interesting solution for high-power applications where the use of film capacitors would be more costly. However, it is also necessary to add two diodes to ensure unidirectional current flow to the load, increasing conduction losses. An 85 W prototype with an input voltage of 200 V and switching frequency of 52 kHz is built; it complies with IEC61000-3-2 with a THD of 9.2%, power factor of 0.994 and efficiency of 83%, where the diode conduction losses are the primary source of losses.

In [40] another variation of the Nabae rectifier is studied to use lower-voltage rating components, named as three level interleaved boost DCM (TLI DCM). The virtual neutral is extended, splitting the DC bus output into a capacitor divider, and two fast diodes are added between them and the switches. These modifications result in the reduction of the voltage effort at the semiconductors and output capacitors to half of the DC bus. It uses asymmetric pulse width modulation (PWM) to control the switches and balance the output capacitor voltage, so there is no ZVS to reduce losses. The proposed converter achieves a power factor of 0.99 and a THD of 10%, with an efficiency of about 90%.

This paper is an extension of [11, 12]. A high-power single-phase version of the TAIPEI rectifier is studied for electrodomestic applications with a line frequency of 50–60 Hz, in accordance with IEC 61000-3-2 class A, CISPR 14, and IEC 60950-1 Class I. The rectifier is compared to other single-phase topologies to analyse its advantages and disadvantages. More details are given about the component design and selection to optimize operational results. The electromagnetic interference is analysed and compared to CISPR 14. A simpler hysteresis control is used, maintaining a fast dynamic response without increasing controller costs. The SPT optimizes the volume and price of the passive components of the output stage by implementing a three-level DC bus with a virtual neutral that employs low-rating electrolytic capacitors, also, a coupled inductor improves common mode noise from load, reduces current ripple at the bus capacitors, and reduces noise from the high dV/dT caused by the boost cells' interleaving process.

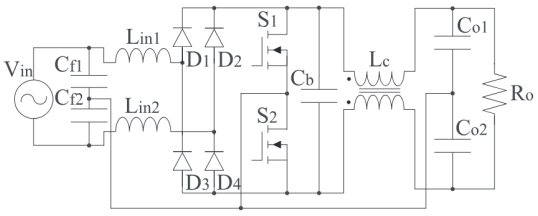

FIGURE 2 | Proposed single-phase TAIPEI rectifier for power factor correction.

The modification of the three-phase TAIPEI rectifier into a single-phase version uses two interleaved boost converter cells, similar to the Nabae rectifier and its variations. The main advantages of this rectifier are: switch-on with ZVS in both switches, requires small output electrolytic capacitors, has high common-mode noise immunity, has a simple control circuit, continuous input current and uses the body-diode from the switch of the adjacent cell as a boost diode.

Section 2 explains the proposed topology and its features, comparing the advantages and disadvantages to other DCM similar topologies. Section 3 presents the theoretical analysis, including design equations and component selection. The simulations and experimental results with a 3 kW prototype are presented in Section 4, followed by discussion and conclusions in Section 5.

2 | Description of the Single-Phase TAIPEI Rectifier

Figure 2 shows TAIPEI rectifier modified to operate as a single-phase topology. It is formed by two boost cells separated by a midpoint connected between C_{f1} and C_{f2}, S_1 and S_2, C_{o1} and C_{o2}. The midpoint works as a virtual neutral with zero potential, increasing the symmetry of the circuit to ground and improving common-mode noise immunity. The cells are decoupled due to the virtual neutral, so the boost inductors L_{in1} and L_{in2} are magnetized individually by half of the input voltage imposed by the input capacitor C_{f1} or C_{f2}.

There is no specific component used as boost diodes; instead, it uses the switch's body diode of the adjacent cell to transfer the energy from the boost inductor to the output, sparing two fast diodes.

The switches S_1 and S_2 operate in a complementary way, so while one cell is magnetizing the boost inductor, the other is transferring the energy accumulated in its boost inductor to the output.

The capacitor C_b and the coupled inductor L_c form a high-frequency current source, where at each switching frequency semi-cycle the energy stored in L_{in1} and L_{in2} are transferred to one of the output capacitors C_{o1} and C_{o2}, respectively.

To keep the voltage balanced in C_{o1} and C_{o2} besides maintaining ZVS, S_1 and S_2 operate with a fixed duty cycle of 50% and the power flow is controlled by varying the modulation frequency.

The boost inductor current of each cell adds up in the converter's input power mains. Due to both cells operating in opposed stages, part of the discontinuous current is cancelled, resulting in a continuous input current with a ripple of twice the switching frequency.

2.1 | Analysis of Operation

The rectifier has eight operational stages in one switching cycle, where two of them are due ZVS in S_1 and S_2. To facilitate the analysis, some considerations are taken:

- The rectifier is operating in steady state with fixed frequency switching and duty cycle of 50% in S_1 and S_2;
- The switching frequency is fast enough that the input voltage remains constant during this period;
- The network input voltage is in the positive semi-cycle ($V_{in} > 0$);
- All components are considered ideal, so series resistances and inductances, forward voltages and parasitic elements are not included;
- The capacitors C_{f1} and C_{f2} have the same capacitance values, and are large enough that the voltage remains constant during one switching cycle;
- Switches S_1 and S_2 are represented by an ideal switch with an anti-parallel diode and a parallel capacitor, which simulate respectively the MOSFET's body diode and the output capacitance (C_{oss}).

Figure 3 presents the eight operational stages, with the current loop of each component drawn instead of the equivalent current, to clearly distinguish the operational stage of each cell. Figure 4 presents the resulting waveforms considering one switching cycle. Next to each figure with a smaller scale, the waveforms are replotted for one cycle of the low-frequency network.

1. Stage one: S_1 is switch-on, but the current flows through D_{S1} because the current in L_{in2} is higher than L_{in1}. C_{f1} imposes half of input voltage (V_{in}) in L_{in1} which starts to store energy. L_{in2} charges C_b which transfer energy to the output capacitor C_{o2}.
2. Stage two: L_{in1} has more storied energy than L_{in2} and the current start to flow through S_1. The other components keep working according to the first stage.
3. Stage three: There is no more energy stored in L_{in2} and its current is null while the other components keep the same operation as the previous stages.
4. Stage four: S_1 is turned off and S_2 is turned on. Part of the current flows through C_{s1} and C_{s2}, charging the first with the output bus voltage V_o and discharging the second at the same rate.
5. Stage five: The switching process ends and L_{in1} start to demagnetize through D_{s2} to charge C_b while L_{in2} start to storage energy. The current flows through D_{s2} because the energy in L_{in1} is higher than L_{in2}. With the shift of the

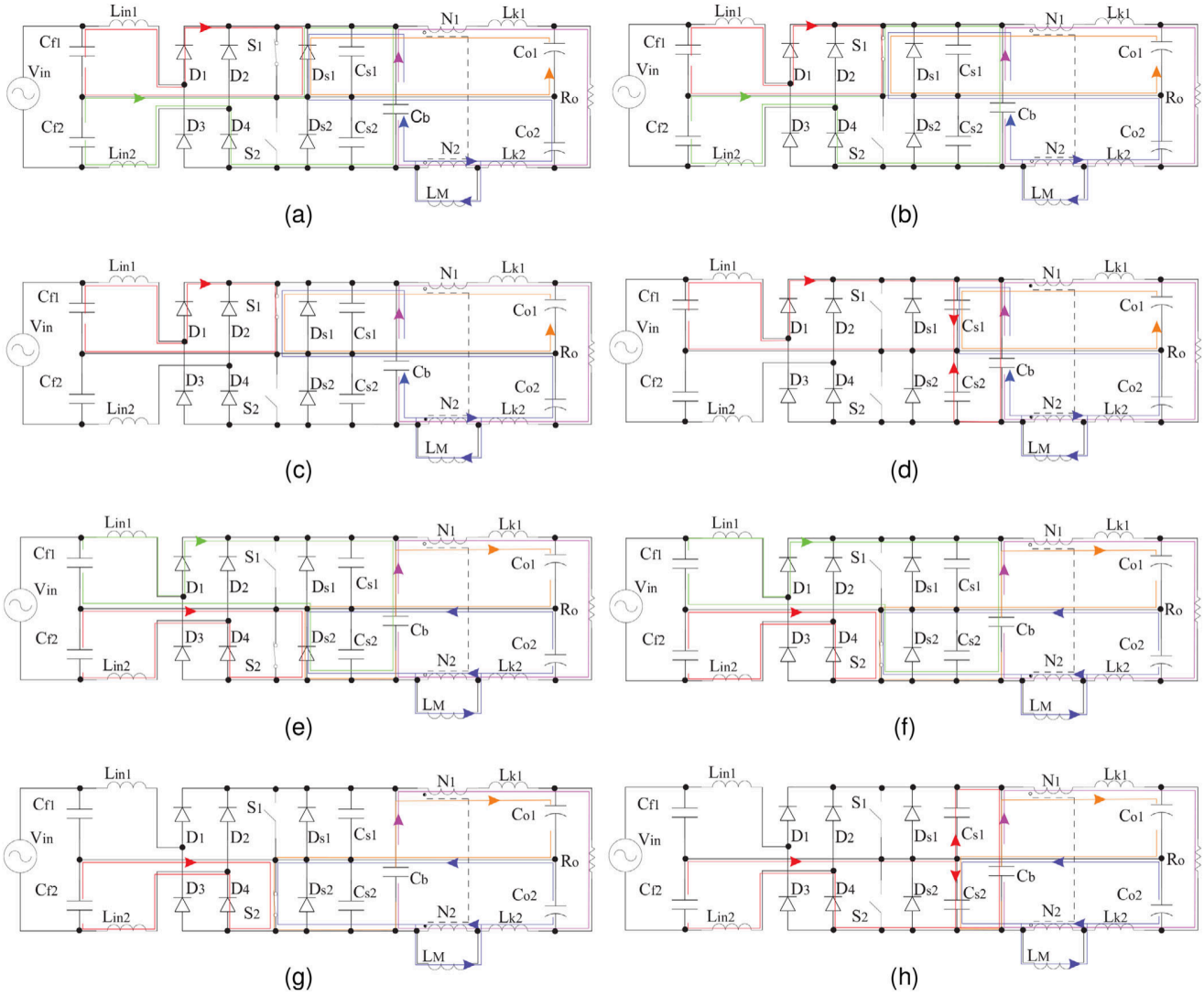

FIGURE 3 | Operational stages of SPT rectifier at one switching cycle for $V_{in} > 0$. (a) $[T_1 - T_2]$. (b) $[T_2 - T_3]$. (c) $[T_3 - T_4]$. (d) $[T_4 - T_5]$. (e) $[T_5 - T_6]$. (f) $[T_6 - T_7]$. (g) $[T_7 - T_8]$. (h) $[T_8 - T_1]$.

demagnetizing cell, the displacement current in C_b reverses, transferring the energy to C_{o1}. During this stage, C_{f2} imposes half of the input voltage to magnetize L_{in2}.

6. Stage six: L_{in2} has more storied energy than L_{in1} and the current start to flow through S_2. The other components keep working according to the fifth stage.
7. Stage seven: There is no more energy stored in L_{in1} and its current is null while the other components keep the same operation as the previous stages.
8. Stage eight: S_2 is turned off and S_1 is turned on. Part of the current flows through C_{s1} and C_{s2}, charging the second with the output bus voltage V_o and discharging the first at the same rate.

2.2 | Topological Comparison of SPT

Table 1 summarizes the main features of the SPT converter in comparison to similar single-phase topologies. Due to the discontinuous current at the boost cells, diodes have zero-current-switching (ZCS).

All topologies only require controlling the output voltage, and the controller complexity depends mainly on the modulation type. FM is simpler due to its use of hysteresis control, but it has limitations on load variation. In contrast, PWM uses complex circuits but can be easily tuned to operate with light loads.

The topology from [40] is interesting when it aims to reduce cost with semiconductors while still achieving low common-mode noise, thanks to the use of low-voltage rating components.

For applications where AC film capacitors are not desired, [39] is a good option if maintaining a good trade-off in the diodes' conduction losses.

The SPT requires low current ripple (LCR) and voltage rating electrolytic capacitors, so the DC bus cost is improved.

TABLE 1 | Main differences between SPT and similar topologies.

		DCM interleaved boost PFC [35]	Nabae rectifier [38]	Nabae modified w/ elect. cap. [39]	Three-level DCM boost [40]	Single-phase TAIPEI rectifier
Transistors comm.		Lossy switching	ZVS	ZVS	Lossy switching	ZVS
Diodes comm.		ZCS	ZCS	ZCS	ZCS	ZCS
Modulation		PWM	FM	FM	PWM asymmetric	FM
Control		PI voltage loop	Hysteresis	Hysteresis	PI voltage loop	Hysteresis
D_x:	Type	Slow / Ultrafast	Ultrafast	Ultrafast / Ultrafast	Ultrafast / Ultrafast	Ultrafast
	Quantity	4 / 2	4	4 / 2	4 / 2	4
	Voltage	V_{in} / V_o	V_{in}	V_{in} / $(V_{in}/2) - V_o$	V_{in} / $V_o/2$	V_{in}
S_x:	Voltage	V_o	V_o	V_o	$V_o/2$	V_o
	Quantity	2	2	2	2	2
L_x:	Type	DCM boost	DCM boost	DCM boost	DCM boost	DCM / CM filter
	Quantity	2	2	2	2	2 / 1
C_x:	Type	Electrolytic	AC film / Elect.	Elect. / Elect.	Elect. / AC film	Elect. / AC film / DC film
	Local	Boost cells	Boost / DC bus	DC bus / Boost	Split DC / Boost	Split DC / Boost / Filter
	Ripple	HCR	HCR / HCR	HCR / HCR	HCR / HCR	LCR / HCR / HCR
	Quantity	1	2 / 1	1 / 2	2 / 2	2 / 2 / 1
	Voltage	V_o	$V_{in}/2$ / V_o	V_o / $V_o/2$	$V_o/2$ / $V_{in}/2$	$V_o/2$ / $V_{in}/2$ / V_o

TABLE 2 | Powersim simulation parameters.

Parameter	Symbol	Value
Output power	P_o	1000 W
Output voltage	V_o	600 V
Input voltage	V_{in}	220 V
Switching frequency	f_s	50 kHz
Network frequency	f_r	60 Hz
Maximum voltage ripple at V_o	ΔV_o	10%
Cut-frequency input filter	—	5 kHz

The rectifier from [38] features a simpler topology, utilizing a neutral point to mitigate common-mode noise, but it requires a bulky DC bus capacitor due to the high current ripple (HCR).

To evaluate the topologies quantitatively, they are simulated in the software Powersim according to the features exhibited in Table 2. The simulation results are used to calculate figures of merit for processed power in semiconductors and for energy in passive components, both linked to efficiency and cost.

1. Transistors: Uses (1), where I_{RMS} is the transistor's effective current considering the body-diode. This variable is linked to conduction losses, heatsink size, and component price. V_{max} is the maximum blocking voltage, linked to switching losses and price.

$$P_{FMS} = I_{RMS} V_{max} \tag{1}$$

2. Diodes: Uses (2), where I_f is the diode's forward current, related to conduction losses, heat sink size and component price. V_{RRM} is the maximum repetitive reverse voltage required, linked to switching loss and price.

$$P_{FMD} = I_f V_{RRM} \tag{2}$$

3. Inductors: Uses (3), where L_x is the component's inductance, linked to volume, number of turns, and component price. I_{RMS} is the effective current, linked to winding losses, temperature rise, volume, and price (copper volume). I_{pk} is the peak current, related to the number of turns, and core losses (ΔB_{sat}).

$$E_{FMI} = \frac{1}{2} L_x I_{RMS} I_{pk} \tag{3}$$

4. Capacitors: Uses (4), where C_x is the component's capacitance and Δ_V is the voltage ripple, both linked to volume, component price, and losses (dissipation factor).

$$E_{FMC} = \frac{1}{2} C_x \Delta_V^2 \tag{4}$$

Figure 5a presents the normalized processed power for all semiconductors in each topology. The topologies from Nabae, Nabae modified and SPT have higher processed power. The transistors dissipate most of the processed power because they switch at V_{out} and have the current from the boost diode incorporated in the intrinsic antiparallel diode, increasing I_{RMS}. TLI DCM presents lower processed power because the semiconductors switch at

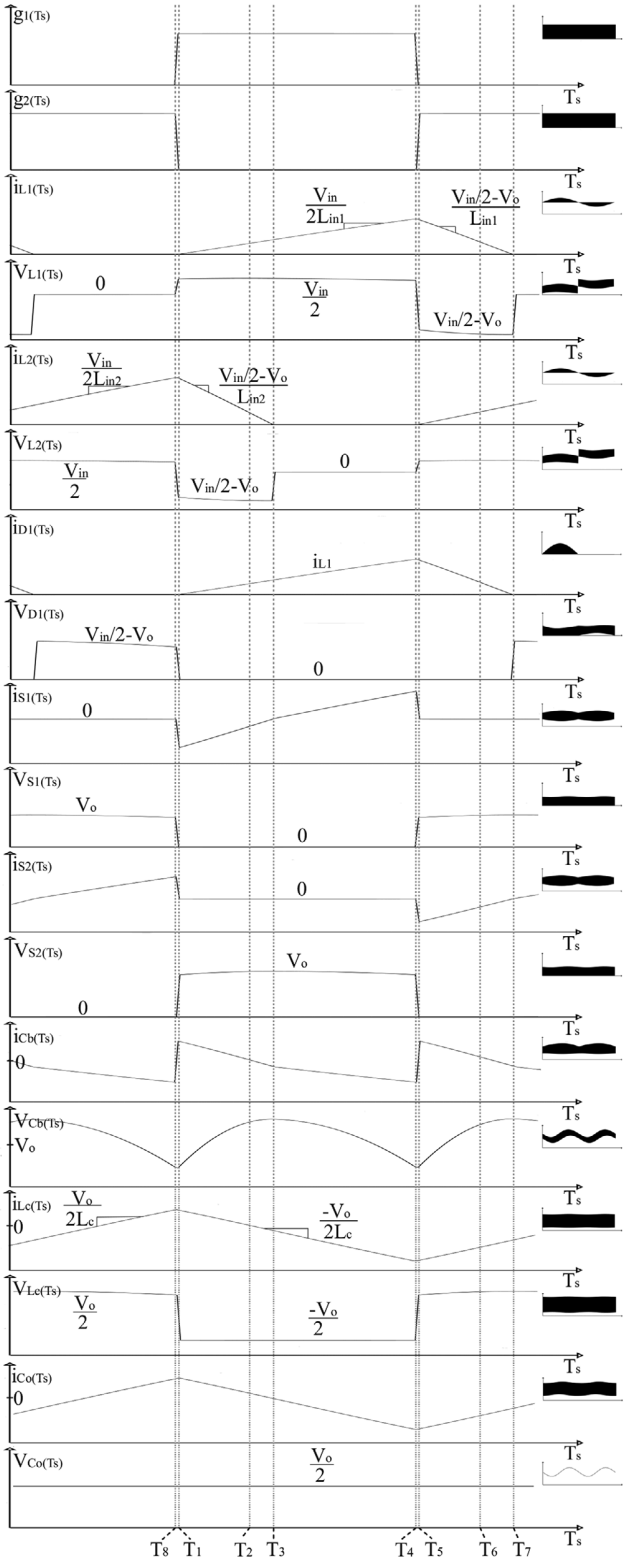

FIGURE 4 | Main waveforms of SPT rectifier at one switching cycle for $V_{in} > 0$ and $\mu_o < 0.4$. The gates g_1 and g_2 are plotted as a reference for each operational stage. Next to each high-frequency waveform is plotted on a smaller scale the same signal extrapolated for one low-frequency network cycle.

$V_{out}/2$. Although BDCM and BIDCM yield equivalent results for this figure of merit, it is worth noting that in BIDCM, the current through the boost diodes and transistors is half that in BDCM.

Figure 5b presents the normalized energy accumulated in the passive components, accounting for the input EMI filter. The total energy from magnetic components is lower in the topologies with virtual neutral than in the classical BDCM and BIDCM. TLI DCM and SPT have lower total energy consumption in passive components, making them more economical since passive components are more expensive than semiconductors. TLI DCM is more promising than SPT for reducing semiconductor costs, even with two additional diodes, since it uses transistors and boost diodes switched with $V_{out}/2$. Even though both have similar total energy in the passive components, the SPT permits better optimization of the output capacitors due to the presence of the common-mode inductor installed between the boost cells and the three-level output capacitors. Figure 5c presents the normalized current per output capacitor for each topology, highlighting the advantage of SPT.

The graphics from Figure 5 highlight one advantage of SPT: the lower energy accumulated in the passive components, which allows better optimization of these components compared to other DCM topologies. However, it also highlights a disadvantage: the high processing power in semiconductors, especially transistors. Based on that, the topology is more interesting for high-frequency applications, reducing magnetic components even further and taking advantage of ZVS in transistors to minimize switching losses at the component with the higher processed power. For higher output power, this analysis remains valid, since only the energy per component increases, while the dynamics of the topologies remain the same. In the next section, each component of the SPT is analysed to optimize costs while maintaining a unitary power factor, an acceptable efficiency, and input THD that comply with IEC 61000-3-2 class A.

3 | Qualitative Analyses and Design Equations

In this section, a qualitative analysis is performed for each component to design the single-phase TAIPEI rectifier (SPT), presenting the main equations and methodologies to enhance the converter.

3.1 | Boost Inductor L_{in1} and L_{in2}

The boost inductor operates in DCM, reaching peak current at half the switching cycle. According to (5), the magnetizing current slope is proportional to the voltage applied by C_f, corresponding to half of the input voltage.

$$I_{Lin,pk} = \frac{V_{cf,pk}\sin(\omega_r t)}{L_{in}} \cdot \frac{T_s}{2} \tag{5}$$

As indicated in (6), the demagnetizing time depends on the switching period and the gain α, which is the ratio between the

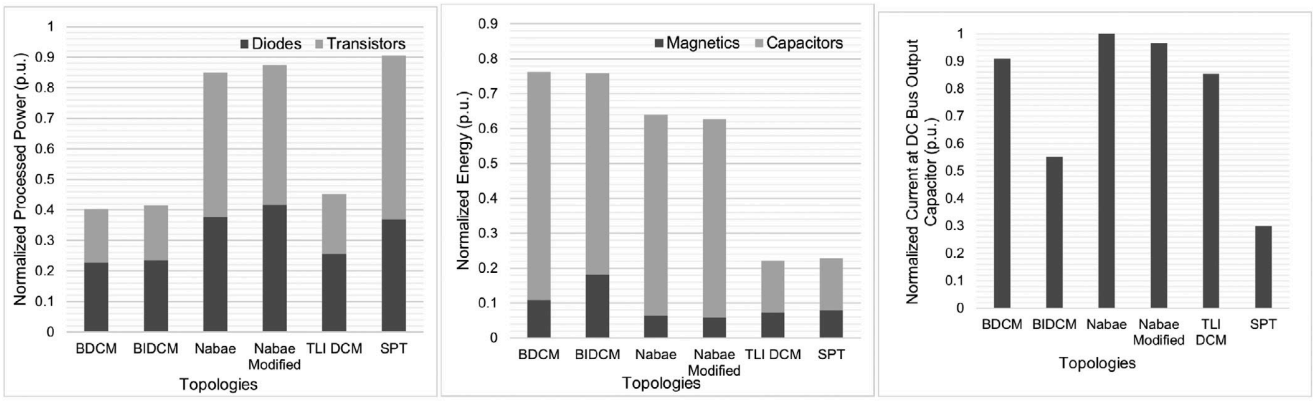

FIGURE 5 | (a) Graphic of normalized processed power in the semiconductors for each DCM converter. (b) Graphic of normalized energy in the passive components for each DCM converter. (c) Graphic of normalized current at the DC bus capacitors.

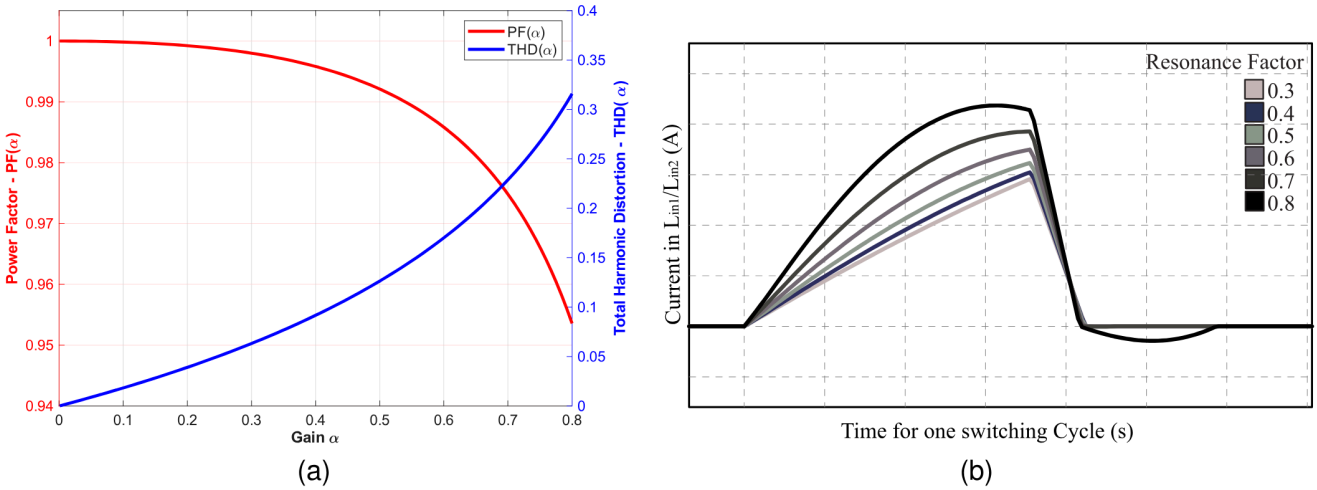

FIGURE 6 | (a) Graphic comparing the impact of α in the input current THD and PF. The increase in output voltage in proportion to the input voltage causes a reduction in the input current ripple, improving THD and PF. (b) Current in L_{in} for different values of μ_o. As the resonance factor increases, the input filter formed by L_{in} and C_f becomes under-damped, and the current assumes a sinusoidal waveform.

peak voltage at C_f and output voltage of the boost cell.

$$t_d = \frac{\alpha \sin(\omega_r t)}{1 - \alpha \sin(\omega_r t)} \cdot \frac{T_s}{2} \tag{6}$$

As reported in [1, 37], higher voltage gains of the boost cells reduce the demagnetization time and the input current distortion, improving the power factor. This occurs because the sinusoidal term from (6) is also attached to the input current, adding a distortion that is reduced when α is small enough to make the denominator practically unitary. Figure 6a presents the impact of the demagnetizing current at the input THD for different values of α. Even when ignoring the high-frequency switching ripple, there is still a minimum level of low-frequency distortion due to each cell's demagnetizing current. The interleaved technique is only useful for cancelling even harmonics and part of the switching-frequency harmonics with their sidebands, while the demagnetization time creates low-frequency odd harmonics that are reflected into the rectifier input current, reducing the equivalent THD.

The minimum inductance to maintain the cell in DCM calculated by (7) is the same as for the conventional boost rectifier. It is optimized in applications that require a larger load and are feasible to use higher switching frequency, reducing the component into smaller coils, optimizing the material's volume and weight in the topology.

$$L_{in} = \frac{\alpha R_o \left(-\frac{\pi}{\alpha} + \frac{2}{\alpha\sqrt{1-\alpha^2}} \cdot \left(\frac{\pi}{2} + \arctan\left(\frac{\alpha}{\sqrt{1-\alpha^2}} \right) \right) - 2 \right)}{4\pi f_s} \tag{7}$$

The gain equation is obtained by correlating the output current I_o with the sum of the demagnetizing currents from L_{in1} and L_{in2}, where its average value is the same as the output current. The SPT's gain is the same from a boost converter operating in DCM, calculated by (9) where Ψ_1 is given by (8).

$$\Psi_1 = -2 - \frac{\pi}{\alpha} + \frac{2}{\alpha\sqrt{1-\alpha^2}} \cdot \left[\frac{\pi}{2} + \arctan\left(\frac{\alpha}{\sqrt{1-\alpha^2}}\right)\right] \quad (8)$$

$$\frac{V_o}{V_{in}} = \frac{\sqrt{2}R_o}{8\pi L_{in} f_s} \cdot \Psi_1 \quad (9)$$

As shown in Figure 4 and Equation (5), the inductor current has a triangular shape for each switching cycle, with the peak value changing according to the sinusoidal voltage input. Consequently, the core's flux has a major hysteresis loop that ends at the network line period, with a 2π periodic cycle; and each switching cycle represents an inner minor hysteresis loop that repeats until it closes the major hysteresis loop. To calculate core losses in flux waveform with minor loops, the improved modified generalized Steinmetz (iGSE) equation from [41] must be used, once the losses depend on the time history of the flux waveform as well as on its instantaneous value and derivative. The total core losses correspond to the sum of losses caused by the minor and major loops, calculated with (10) using the Steinmetz coefficients and (11).

$$\overline{P_v} = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \quad (10)$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \quad (11)$$

The magnetic core of L_{in1} and L_{in2} should be of ferrite material with an air gap, since the current ripple is high and core losses are worse than converters with continuous current. Ferrite materials exhibit lower core losses than powder cores with distributed gaps. Additionally, the low permeability from the air gap dominates the equivalent core permeability, and the inductance remains relatively unchanged with variations in current ripple or temperature.

When designing the winding, it is important to consider AC resistance losses caused by frequency modulation, which may lead the rectifier to operate at a high frequency as specified by the design. The harmonics and multiples of the switching frequency further increase the skin and proximity effects. Therefore, the authors recommend selecting a winding cross-section at least twice that determined by the skin effect from (12), using the rated switching frequency as a reference.

$$\delta(f) = \sqrt{\frac{\rho_T}{\pi f_s \mu_o}} \quad (12)$$

Equations (13)–(17) from [42] calculate R_{AC} as a fraction $F_R(f)$ of R_{DC} and take into consideration the skin effect in the first term and the proximity effect in the second term. N_l is the non-integer number of layers, k is the number of parallel strands per winding, d_e is the equivalent diameter of the set of k parallel strands, d_i is the diameter of the bare conductor wire and η_w is the porosity factor.

The total winding losses are calculated by the sum of the losses caused by each harmonic and its equivalent R_{AC}, summed to the losses from R_{DC}.

$$R_{AC}(f) = R_{DC} F_R(f) \quad (13)$$

$$F_R(f) = A_f\left[\frac{\sinh(2A_f)+\sin(2A_f)}{\cosh(2A_f)-\cos(2A_f)} + \frac{2(N_l^2 k-1)}{3}\frac{\sinh(A_f)-\sin(A_f)}{\cosh(A_f)+\cos(A_f)}\right] \quad (14)$$

$$A_f = A(f) = \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \frac{d_e}{\delta(f)\sqrt{k}}\sqrt{\eta} \quad (15)$$

$$d_e = d_i\sqrt{k} \quad (16)$$

$$\eta_w = 0,9\frac{d_e}{d_i} \quad (17)$$

3.2 | Input Capacitors C_{f1} and C_{f2}

These AC capacitors form a voltage divider splitting both boost cells between the virtual neutral with half of the input voltage each. L_{in1} and L_{in2} along with C_{f1} and C_{f2} form LC filters where the ratio between the switching frequency (ω_s) and the filter natural frequency (ω_{o1}) defines the quality factor μ_o in (18) and nominated as resonance factor.

$$\mu_o = \frac{\omega_{o1}}{\omega_s} = \frac{\frac{1}{\sqrt{L_{in}C_f}}}{2\pi f_s} = \frac{1}{2\pi f_s\sqrt{L_{in}C_f}} \quad (18)$$

In Figure 6b, the boost inductor current waveform for different values of μ_o is plotted. As the resonance factor increases and approaches the filter's natural frequency, the waveform becomes more sinusoidal due to the effects of resonance. The authors recommend designing L_{in} and C_f to result in $\mu_o < 0.4$ to ensure an over-damped filter and reduce the current efforts.

The minimum value of C_{f1} and C_{f2} are calculated using (19) by selecting a value for μ_o.

$$C_{f1,min} = C_{f2,min} = \frac{1}{4\pi^2 f_s^2 \mu_o^2 L_{in}} \quad (19)$$

By choosing values of μ_o higher than 0.4, the distortion in the inductor current is reflected in the input harmonics, increasing the THD. This is because the resonance becomes more intense, reflected in the C_{f1} and C_{f2} voltages due to the addition of a high-frequency ripple oscillating at the switching frequency. The high-frequency ripple can be calculated by (20).

$$V_{cf\_res} \approx \left|\frac{I_{L\_fund}}{C_f \cdot \omega_s \cdot (\mu_o^2 - 1)}\right| \quad (20)$$

The peak amplitude of each harmonic considering the effect of α and μ_o can be approximated by the series Taylor expansion of (21) where the instantaneous averaged current is calculated by (22) where $\Delta\alpha = V_{cf\_res}/V_o$.

$$b_n = \frac{1}{\pi}\int_0^{2\pi} i_{in}(\omega t)\sin(n\omega t)\, d(\omega t) \quad (21)$$

$$i_{in}(\omega t) = \frac{V_o \sin(\omega t)}{8 f_s L_{in}}\left[\frac{\alpha_0}{1-\alpha_0|\sin(\omega t)|} + \frac{0.5\cdot|\sin(\omega t)|\cdot\Delta\alpha^2}{(1-\alpha_0|\sin(\omega t)|)^3}\right] \quad (22)$$

Table 3 shows the importance of μ_o in the design by presenting the resonance impact for various μ_o values in a 1 kW SPT with a 20

TABLE 3 | Impact of μ_o in the low frequency harmonics using Equations (22) and (21). The design considers an SPT of 1 kW, with switching frequency of 20 kHz, $\alpha = 0.43$, and $L_{in} = 60.43$ µH.

Harmonic	$\alpha = 0.43$	$\mu_o = 0.2$	$\mu_o = 0.3$	$\mu_o = 0.4$	$\mu_o = 0.5$	$\mu_o = 0.6$
1st	12.86	12.87	12.96	13.24	14.00	16.15
3rd	1.31	1.32	1.35	1.46	1.76	2.60
5th	0.02	0.02	0.02	0.04	0.04	0.15
7th	0.03	0.03	0.03	0.03	0.04	0.05

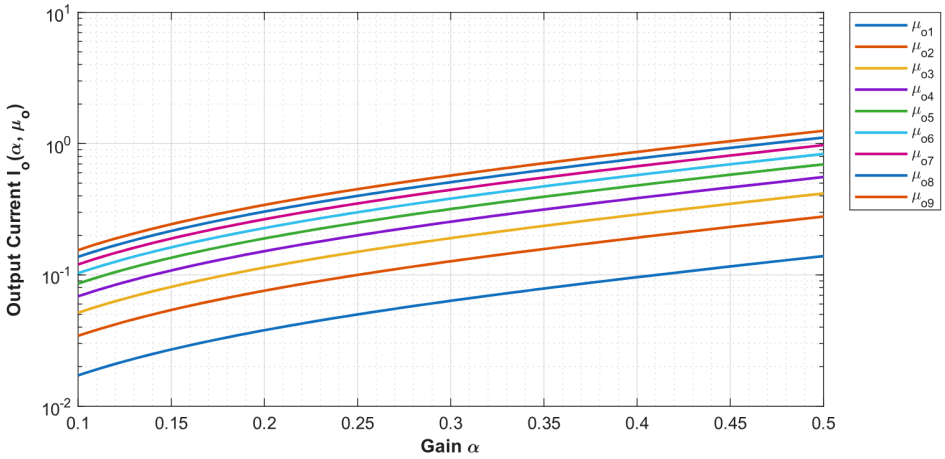

FIGURE 7 | Graphic of normalized output current (I_o) in function of the gain α for multiple values of μ_o. Lower values of α result in a reduction of I_o due to the decrease of t_d from L_{in}. I_o is also affected by the resonance factor, which increases the RMS value of L_{in} during the stages $[T_1 - T_3]$ and $[T_5 - T_7]$.

kHz switching frequency, $\alpha = 0.43$ and $L_{in} = 60.43$ µH. The first column lists the theoretical peak of each harmonic considering only the distortion from α; the others include resonance effects from Equations (22) and (21). For μ_o values below 0.4, the third harmonic increases by up to 12%, so this limit should be respected in designs. In this case, the equivalent THD is 10.21% when only α distortion is considered, and 11.02% when both α and $\mu_o = 0.4$ are included.

In Figure 7, the normalized output current is plotted as a function of α for different values of μ_o. For lower values of α the current efforts are minimized due to the reduction of t_d. For $\mu_o > 0.2$, the output amplitude current is more sensitive to the impact of the under-damped filter, which also reflects in more losses at C_{o1} and C_{o2}.

Besides the fundamental frequency, the switching-frequency harmonics with their multiple sidebands are the dominant source of loss in C_f. Their loss contribution is calculated by (23), by the sum of the loss of each harmonic in the equivalent series resistance (ESR).

$$P_{loss,n} = \sum \mathrm{ESR}(f_n) \cdot I^2_{rms,n} \tag{23}$$

The ESR comprises all resistance phenomena that can contribute to the capacitor's dissipation factor, so its value changes with frequency. According to [43], at low frequencies, there is predominance of dielectric losses, and the approximate ESR is calculated using Equation (24) with $\tan\delta(f)$ given by the manufacturer. At medium frequencies, losses at the capacitor pads are dominant, and ESR becomes practically constant, and at high frequencies, ESR increases at a rate of $\sqrt{(f_s)}$ due to the skin effect. Based on this information, the ESR at different frequencies can be modelled to predict component losses with greater precision.

$$\mathrm{ESR}(f) = \frac{\tan\delta(f)}{2\pi f C} \tag{24}$$

The authors recommend using film capacitors with polypropylene dielectric because this material exhibits lower capacitance variation due to temperature, humidity and frequency, making it more suitable for frequency modulation with $\mu \leq 0.4$ and reducing the risk of input current THD deterioration due to capacitance drop.

3.3 | Capacitor C_b

The boost capacitor C_b filters the current demagnetized by L_{in1} and L_{in2}. Hence, film capacitors are recommended due to their low equivalent series resistance and inductance, which is ideal for filtering high-frequency harmonics.

Due to the interleaved demagnetization of the boost inductors, at each half of the switching cycle, the voltage across C_b abruptly changes in relation to the virtual neutral proportionally to the

DC bus voltage, this fast dV/dt produces common-mode noise that would increase the current at C_o and add unacceptable noise to the load, hence, a coupled inductor (L_c) in common mode configuration must be added between C_b and C_o to work as a filter.

The voltage across C_b is equal to the sum of the voltages of C_{o1} and C_{o2}, that is, the output voltage V_o, since the average voltage across L_c is zero.

The minimum value for C_b in (25) considers the sum of demagnetization currents and the maximum high-frequency voltage ripple specified for the component (ΔV_{C_b}). As C_{o1} and C_{o2} store the energy for the DC bus, and C_b filters mainly high-frequency harmonics, the resulting capacitance is small, and the component is selected based on the maximum RMS current.

$$C_b = \frac{\alpha^2 V_o}{8 f_s^2 L_{in} \Delta V_{C_b} (1-\alpha)} \tag{25}$$

The same Equations (23) and (24) are suitable to calculate losses in C_b. The biggest difference is the DC level and the order of the highest impact harmonics, been the double of the network frequency and the switching frequency since the capacitor receives the demagnetizing current from both boost cells.

3.4 | Semiconductors Devices and Soft-Switching

The SPT is composed of four fast diodes and two switches. The body diode from both switches is used as a boost diode for the adjacent cell, reducing price, volume, and switching losses.

The body diodes do not have reverse recovery losses; the current is inherently reduced to zero during stages one to three and five to seven when the energy from both boost inductors becomes equal. After this point, the current starts to flow through the switch's channel, and the voltage applied to the body diode recovers its depletion area, which is proportional to the switch's channel drop voltage.

The diodes from the bridge rectifier also do not have reverse recovery losses due to the discontinuous current of the boost inductors. However, they must have fast switching features because of the high-frequency current ripple. Additional losses may occur when the boost inductor's current is null due to resonance between its inductance and the rectifier diode's junction capacitance. These losses are reported in [1] and are reduced by selecting diodes with small junction capacitances.

The moment S_1 or S_2 is switched-on, its body diode conducts the resulting current from both cells. The current from the cell storing energy is lower, and the resulting current is always in the same direction as the polarized diode; hence, the moment the switch is commanded, the voltage applied to its terminals is proportional to the body diode forward voltage.

To maintain ZVS, the energy stored in the boost inductor must be higher than the switch's output capacitance C_{oss} as indicated in (26). The critical condition occurs with maximum frequency operation (minimum load) and minimum input voltage. If the energy accumulated in L_{in1} or L_{in2} is insufficient, part of the current used to discharge C_{oss} is diverted from the transistor's channel, resulting in a combination of soft and hard switching.

$$\frac{1}{2} C_{oss} V_o^2 < \frac{1}{2} L_{in} I_{peak}^2 = \frac{V_{cf,pk}}{8 L_{in} f_s^2} \tag{26}$$

Figure 17b presents a graph of the loss distribution in an SPT of 3 kW with rated switching frequency of 79 kHz. S_1 and S_2 are responsible for approximately 45.7% of the overall losses, followed by the four rectifier diodes with 21.3%. To achieve high efficiency, it is necessary to prioritize semiconductor devices with low conduction losses.

One way to improve conduction losses in S_1 and S_2 is to use MOSFET devices with synchronous rectification, linking the power loss to the drain to source channel resistance $R_{DS(on)}$ instead of the diode forward voltage drop (V_f). This is simple to implement because the current always starts to flow in the source-to-drain direction, so it is only necessary to have a MOSFET with a lower voltage drop in $R_{DS(on)}$ than V_f.

The losses from the MOSFETs and the bridge diodes are calculated similarly to L_{in}, summing the losses from each switching cycle since the peak current also varies with the sinusoidal input voltage. The intrinsic variables of each component can be obtained from the datasheet's extrapolation data adjusted to the component's electrical waveforms at the specified operational temperature.

The MOSFET's conduction losses depend on the drain-to-source resistance, which varies with drain-to-source voltage and temperature, and are calculated individually for each switching cycle using (27).

$$P_{cond_s w} = \frac{1}{T_g} \int_0^{T_g} R_{DS(on)}(i_D, T_j) \cdot i_D(t)^2 \, dt \tag{27}$$

The switching losses depend on the gate resistance R_G, the MOSFET's input capacitance C_{iss} which has a non-linear behaviour and reduces according the voltage, the gate threshold V_{TH}, plateau voltages V_{gp}, and gate to source V_{GS} voltages; also the drain to source voltage $V_{DS(D)}$ and equivalent charge $Q_{GD(D)}$.

To compute the switching losses, the energy per switching cycle is calculated based on [44] using transition times, MOSFET's capacitances, and operational voltages applied in Equations (28) and (29) with transition times of (30) and (31).

$$E_{on} = \frac{t_{on} \cdot V_{DS} \cdot I_{DS(on)}}{2} \tag{28}$$

$$E_{off} = \frac{t_{off} \cdot V_{DS} \cdot I_{DS(off)}}{2} \tag{29}$$

$$t_{on} = R_G \left[C_{iss(V_{DS})} \ln\left(\frac{V_{GS} - V_{TH}}{V_{GS} - V_{gp}} \right) + \frac{Q_{GD(D)}}{V_{DS(D)}} \cdot \frac{V_{DS}}{V_{GS} - V_{gp}} \right] \tag{30}$$

$$t_{off} = R_G \left[\frac{Q_{GD(D)}}{V_{DS(D)}} \cdot \frac{V_{DS}}{V_{gp}} + C_{iss(V_{DS})} \ln\left(\frac{V_{gp}}{V_{TH}} \right) \right] \tag{31}$$

Due to the ZVS behaviour of S_1 and S_2 during the switch-on, the loss algorithm uses the relation (26) for each switching cycle, if the energy from L_{in} is enough to discharge the MOSFET's output

capacitors the result from Equation (28) is null for that switching cycle. The critical conditions for ZVS occur at the edges of the line network cycles, where the peak voltage from L_{in} is lower. The switching frequency also reduces the accumulated energy at L_{in} in a quadratic proportion with f_s.

The body-diode and bridge rectifier diode loss model are calculated using Equation (32), which primarily accounts for forward-voltage conduction that varies with current and temperature. Due to the discontinuous current from the boost cells, the losses from reverse-recovery in the bridge rectifier diodes can be ignored, as they switch off with ZCS. The total loss per switching cycle for the diode is calculated using (32), and for the MOSFET using (33). By summing the losses for each switching cycle over one low-frequency line network period, the component's total losses are obtained.

$$P_{cond_d} = \frac{1}{T_g}\int_0^{T_g} \left[V_{SD}(i_D, T_j)\cdot i_D(t)\right]dt \tag{32}$$

$$P_{total_{hf}} = (E_{on} + E_{off})\cdot f_s + P_{cond_s} + P_{cond_d} \tag{33}$$

3.5 | Output Common-Mode Inductor L_c

When S_1 is off during stages five to seven, C_b receives the energy stored in L_{in1}; at this moment, the voltage between C_b and the virtual neutral is equal to V_o. Similarly, when S_2 is off during stages one to three, C_b receives the energy stored in L_{in2} and the voltage between C_b and the virtual neutral is equal to $-V_o$. With these abrupt voltage changes at each half-switching cycle, the current in the output capacitors would have a high RMS value due to the high dV/dt common noise. Hence, a coupled inductor L_c is placed between C_b and the capacitors C_{o1} and C_{o2} to decouple the output and work as a common-mode impedance. The magnetizing inductance is designed according to (34) where ΔI_{Lc} is the peak-to-peak current ripple.

$$L_c = \frac{V_o}{8\Delta I_{Lc} f_s} \tag{34}$$

The winding arrangement creates a high impedance to common-mode current and cancels the flux of differential current, allowing for a core with large inductance and a small gap without saturation. The leakage inductance acts as an additional filter for the differential current, further reducing the RMS value of current in C_{o1} and C_{o2}.

In Figure 8a,b illustrates the reduction in the RMS current value at the output capacitors with an increase in magnetizing and leakage inductances, as determined by a parameter sweep simulation on prototypes of 3 kW with switching frequencies of 20, 50 and 65 kHz. Based on these results, the authors recommend using a ΔI_{Lc} varying between 40% and 50% of the output current ripple to achieve a good trade-off in reducing the current at output capacitors and using a small coil without affecting the rectifier operation. The prototypes with switching frequency of 50 and 65 kHz present a better reduction of the current in C_o for the same values of inductance used in the 20 kHz prototype due the increase of impedance in L_c, so design projects with higher switching frequency also optimizes the volume of C_o.

The leakage inductance depends on the value of L_c and the winding arrangement around the coil. However, expressive reduction in current is achieved with small values of leakage inductance, for example, the current in the SPT of 3 kW is reduced approximately four times using a leakage inductance with 0.5% of the magnetizing value.

Due to the frequency modulation and the reduction in current at C_o for higher values of leakage inductance, it is interesting to minimize the inter-winding capacitance in the winding; consequently, both windings must be assembled separately, not alternating layers. The authors recommend using E or ETD cores, which offer a higher winding-window area per core cross-section, maximizing space for the two windings. The losses from L_c are calculated using the same methodology presented in the Section 3.1 for L_{in}.

3.6 | Output Capacitors

The virtual neutral is extended to the DC bus output, forming a three-level configuration by splitting the output capacitors, where each one has half of the output voltage. This allows the use of low-voltage rating electrolytic capacitors.

Due to L_c and its leakage inductance that filters part of the common and differential mode harmonics, the overall current in the output capacitors is small.

The output capacitances are calculated using (35), which correlates the capacitor's energy to the pulsating power in the DC bus. The maximum allowable low-frequency voltage ripple determines the minimum capacitance.

$$C_{o1} = C_{o2} = \frac{4P_o}{\omega_r(V_{C_{omax}}^2 - V_{C_{omin}}^2)} \tag{35}$$

The same Equations (23) and (24) are suitable to calculate losses in C_o, where the harmonics with biggest impact has double of the line network frequency.

3.7 | Circuit Modulation and Control

To switch-on S_1 and S_2 with ZVS is necessary that the cells work in a complementary way, but is not possible to implement asymmetric modulation because the energy accumulated in L_{in1} and L_{in2} would be different, unbalancing the voltage of the output capacitors and eliminating the advantage of use low voltage rating electrolytic capacitors. Hence, the duty cycle is kept constant at 50%. The switching frequency is modulated to control the power flow through the output, so both cells work in a complementary manner for the same amount of time, and the energy received by the capacitors C_{o1} and C_{o2} is automatically balanced.

It is only necessary to control the output voltage since the currents in L_{in1} and L_{in2} are discontinuous and follow the input voltage V_{in} with a sinusoidal waveform. The simplest way to control it is by using a hysteresis controller, as it is not necessary to know the transfer function $V_o(s)/f_s(s)$.

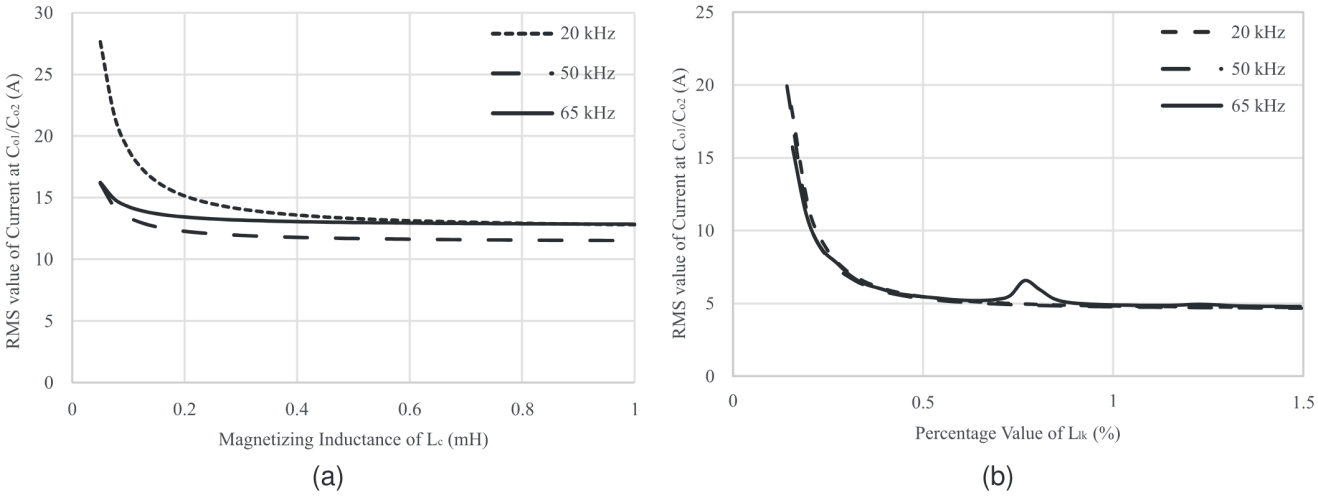

FIGURE 8 | (a) Parameter sweep simulation to evaluate the current at C_o for different values of L_c in an SPT of 3 kW operating with frequencies of 20, 50 and 65 kHz. To optimize L_c, the inductance value chosen for the design should be below 200 μH, before the graphic's linear zone to save turns and reduce core winding area. (b) Parameter sweep simulation to evaluate the current at C_o for different percentage values of L_{lk} to SPT of 3 kW operating at frequencies of 20, 50 and 65 kHz. Even small values of leakage inductance can significantly reduce the current at C_o.

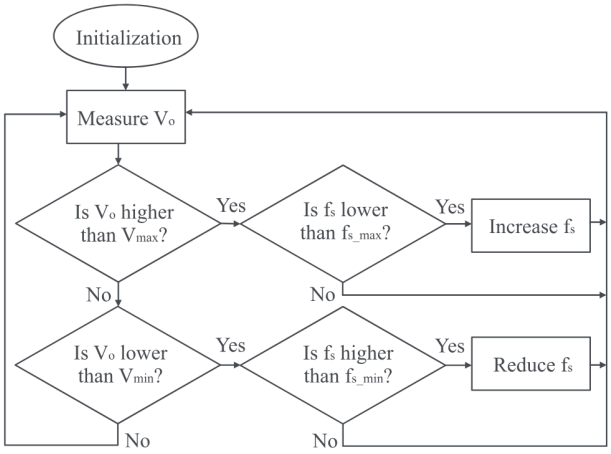

FIGURE 9 | Flowchart of the hysteresis controller to limit the output voltage. F_s is always compared to the design minimum and maximum values before updating the driver switching frequency to avoid extrapolated values at significant load changes near the SPT's operational limits.

The power flowing through the output capacitors increases by reducing the switching frequency; hence, the output voltage is inversely proportional to the switching frequency. Hence, the critical inductance and the minimum switching frequency must be designed for the condition in which the currents in L_{in1} and L_{in2} are higher, ensuring a higher power flow to the load without saturating the inductors.

Figure 9 summarizes in a flowchart the behaviour of the hysteresis controller. The output voltage is measured cyclically to compare with the limit values of V_o. Once a violation occurs, the algorithm checks if the operational frequency limits have been achieved before incrementing or decrementing the switching frequency.

The switching frequency boundaries are necessary to maintain the boost inductors in DCM at heavy loads and to limit switching losses at light loads. Depending on the SPT's features, the switching frequency can reach values unfeasible for maintaining the converter's operation; in these cases, the burst mode operation must be applied as described in [6].

The power limitation of the rectifier is related mainly to the impacts of L_{in}, α and μ_o on the third harmonic. As verified in (7) the inductance of the boost cells is inversely proportional to the rectifier power and switching frequency. The inductance value reduces linearly with the increase of switching frequency or load.

Considering the scope of this article where the application IEC 61000-3-2 class A, the third harmonic must have the maximum value of 2.3 A_{rms}. Figure 10 presents the critical inductance for different designs considering α, μ_o and f_s. Additional care must be taken for lower inductances values not only due the current ripple at the components of the boost cells, but also in relation to resonance with the diode junction capacitance and for the choice of C_f, to have a good trade off between μ_o and input current phase-shift.

4 | Simulations and Experimental Results

To validate the proposed topology, a 3 kW prototype is built according to the information presented in Table 4. The SPT is designed to be applied as a single-stage power supply with a 385 V DC bus. The input voltage ranges from 160 to 220 V, with the output power varying linearly from 2.2 to 3 kW according the input voltage increases. The minimum inductance and switching frequency are designed at the condition where the current in L_{in1} and L_{in2} are higher, at input voltage of 160 V and output power of 2.2 kW. For rated voltage of 220 V, the load can vary from 2.4 to 3 kW, corresponding to a switching frequency sweep between 79 to 98 kHz at the frequency modulation.

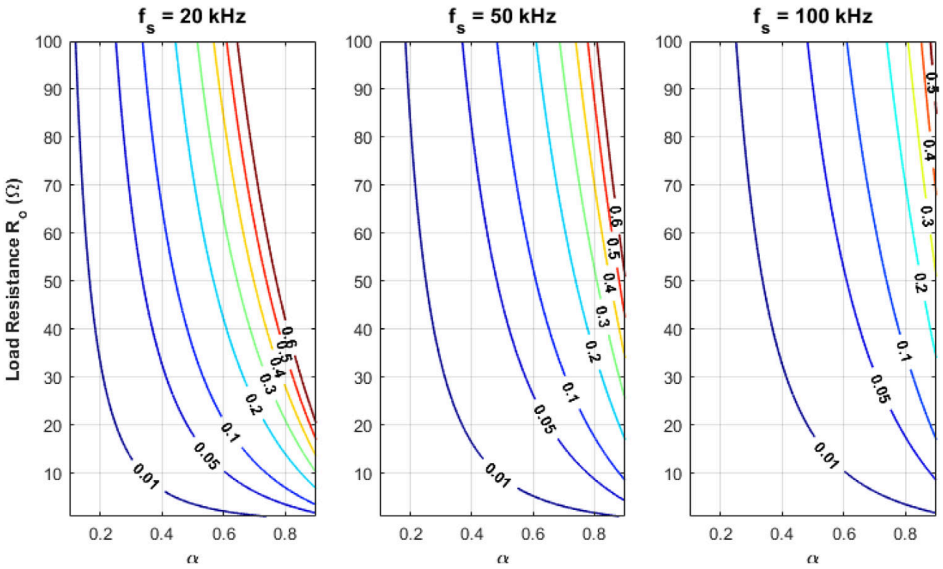

FIGURE 10 | Abacus of L_{in} limits in mH according to load variation and voltage gain for switching frequencies of 20, 50 and 100 kHz.

TABLE 4 | Prototype parameters.

Parameter	Symbol	Value
Output power	P_o	3000 W
Output voltage	V_o	385 V
Input voltage	V_{in}	220 V
Minimum input voltage	$V_{in,min}$	160 V
Minimum switching frequency	f_s	50 kHz
Network frequency	f_r	60 Hz
Quality factor	μ_o	0.25
Maximum high frequency ripple	ΔV_{Cb}	5%
Maximum ripple current at L_c	ΔI_{Lc}	I_o
Maximum voltage ripple at V_o	ΔV_o	10%
Maximum ambient temperature	—	65°C

The boost inductors L_{in1} and L_{in2} have an inductance of 19.6 μH, designed for the boundary condition mode (BCM), which is the critical operating condition with an input voltage of 160 V and a minimum switching frequency of 50 kHz. Each inductor utilizes a PQ 40/40 core of 3C97 MnZn Ferrite, wound with 23 litz wires in parallel, each formed by 22 strands of 38 AWG. It is assembled with 16 turns and a gap of 3.5 mm to optimize the core's window and the fringing flux from the gap into windings. The PQ core offers improved temperature dissipation due to its larger surface area compared to its volume, and also enhances winding coupling as it covers most parts of the winding.

The input filter capacitors C_{f1} and C_{f2} are designed for the same operating condition of L_{in}, each one formed by four film capacitors from TDK (2.2 μF, 4.5 A at 50 kHz, X-type) connected in parallel. It uses polypropylene as a dielectric and metallic plastic film for electrodes (MKP). For safety standards, EMI X-type capacitors are necessary due to their location at the AC side.

The rectifier diodes must block the DC bus voltage, which means a device with at least a 500 V rating, considering the output peak voltage plus a safety margin. It is used the VS-ETL1506-1-M3 (V_{RRM} = 600 V, $I_{F(AV)}$ = 15 A, V_F = 0.85 V @ I_F = 15 A, C_T = 12 pF @ V_{RRM} = 420 V), an ultrafast rectifier diode from Vishay. It has low junction capacitance, reducing oscillation with the boost inductance and avoiding the need for snubber circuits.

The switches S_1 and S_2 also have the maximum voltage equal to the DC bus and should have low output capacitances to require less energy to achieve ZVS. The body diode must have fast switching features, in addition to a low forward voltage, since it conducts part of the cell boost current. It is used the silicon MOSFET IPW60R024CFD7 (V_{DS} = 650 V, $R_{DS(on),max}$ = 24 mΩ, I_D = 49 A @ T_C = 100°C, C_{oss} = 143 pF @ V_{DS} = 400 V, V_{SD} = 1 V @ I_F = 42.4 A, Q_{rr} = 1.3 μC @ V_{RRM} = 400 V and d_{if}/dt = 100 A/μs) from Infineon.

To C_b it is used three small film capacitors from TDK (2.2 μF, 450 V_{DC}, 4.2A A at 50 kHz, MKP) in parallel, the current is mainly composed by high-frequency harmonics, so film capacitors are a good option due its low ESR and capability to support high DC voltage.

The coupled inductor L_c has a magnetizing inductance of 167 μH and leakage inductance of 2.4 μH. It is built using an ETD 59/31/22 core of 3C97 MnZn Ferrite wound with 11 litz wires in parallel, formed by 22 strands of 38 AWG. It is assembled with 30 turns and a gap of 0.19 mm. Each winding is assembled individually in two layers to optimize inter winding intrinsic capacitances. The ETD core is a suitable option for volume optimization, as it features a small cross-sectional area for low common-mode flux compared to a large window area that accommodates multiple-turn windings due to the high inductance and differential current.

TABLE 5 | Parameters for EMI simulation in GeckoCIRCUITS.

Component	Intrinsic parameters for EMI simulation
$D_1 - D_4$	$R_D = 10$ mΩ, $V_{fw} = 1.5$ V, $C_j = 12$ pF, $L_{pad} = 10$ nH
$S_1 - S_2$	$R_{DS} = 27$ mΩ, $C_{DS} = 130$ pF, $L_{pad} = 20$ nH, $R_D = 10$ mΩ, $V_{SD} = 1.1$ V
C_f	$C = 2.2$ μF, ESR = 0.024 Ω, ESL = 10 nH
C_b	$C = 2.2$ μF, ESR = 0.024 Ω, ESL = 10 nH
C_o	$C = 270$ μF, ESR = 0.737 Ω, ESL = 25 nH
L_{in}	$L = 19.6$ μH, $R_w = 2.5$ mΩ, $C_w = 14$ pF
L_c	$L = 167$ μH, $L_{lk} = 2.4$ μH, $R_w = 2.5$ mΩ, $C_{turn} = 2.8$ pF, $C_w = 105$ pF
TO-262AA package	$C_{HS} = 12$ pF@ ceramic insulator
TO-247 package	$C_{HS} = 193$ pF@ ceramic insulator

The output capacitors C_o are formed by four low-voltage-rating electrolytic capacitors in parallel (270 μF, 250 V_{DC}, 1650 mA at 120 Hz).

The hysteresis control algorithm of Figure 9 is implemented in a TMS320F2837xD dual-core microcontroller from Texas Instruments (TI). A delay of 300 μs is added before each measurement to maintain the SPT stable, and the voltage limits are specified, allowing a maximum ripple of 10% of the rated output voltage. V_o is measured with a high precision AMC1301 amplifier from TI with capacitive insulation. The MOSFET's gates are triggered by two UCC5390S isolated gate drivers with split outputs, which individually control the gate's charge and discharge, also from TI.

The rectifier is simulated in the software GeckoCIRCUITS to analyse the impact of the conducted EMI. The intrinsic parasitic parameters of each component are added in simulation as shown in Table 5. It is also added the equivalent capacitances between power components and the heatsink, which contributes to common-mode noise.

The simulation is made for the converter operating in its startup condition @ $V_{in} = 160$ V, $f_s = 50$ kHz, $P_o = 2.2$ kW, which corresponds to the maximum stress of current and critical inductance for DCM operation. The results of differential and common mode noises are presented in Figure 11a. The differential noise dominates the conducted EMI spectrum, reaching a maximum of 110 dBμV at 150 kHz, a multiple of the switching frequency. The common-mode noise has its maximum value at 100 kHz, with 116 dBμV, and the maximum within the CISPR 14 standard is at 200 kHz, with 101 dBμV. The peaks from the common mode spectrum are in the multiples of $2\times f_s$ while the differential noise are in multiples of f_s. Common-mode noise attenuates to 10 MHz, where the intrinsic capacitances become dominant and stabilize the conducted noise.

According to CISPR 14, which applies to electrodomestic equipment and limits EMI conducted emissions from 150 kHz to 30 MHz, the rectifier still requires an EMI filter. Based on that, a two-stage EMI filter is designed according to [45], comprising a single-stage common-mode LC filter coupled with a two-stages differential LC filter. To optimize volume, the common-mode choke's leakage inductance is used to complement the differential inductances of the first-stage differential LC filter. The 50 μH inductance from LISN is used as the differential inductance of the second stage. The component selection for the LC filter follows insertion-loss theory, which involves designing the filter to attenuate a specified dB noise level based on the most harmful harmonic in the EMI spectrum. The components are selected according to (36), where f_h is the frequency of the harmful harmonic, Att_{hdB} is the desired attenuation in decibels, and L and C are the components of the filter for the determined stage.

$$f_{cutoff} = \frac{f_h}{\sqrt{10^{\frac{Att_{hdB}}{20}}}} = \frac{1}{2\pi\sqrt{LC}} \tag{36}$$

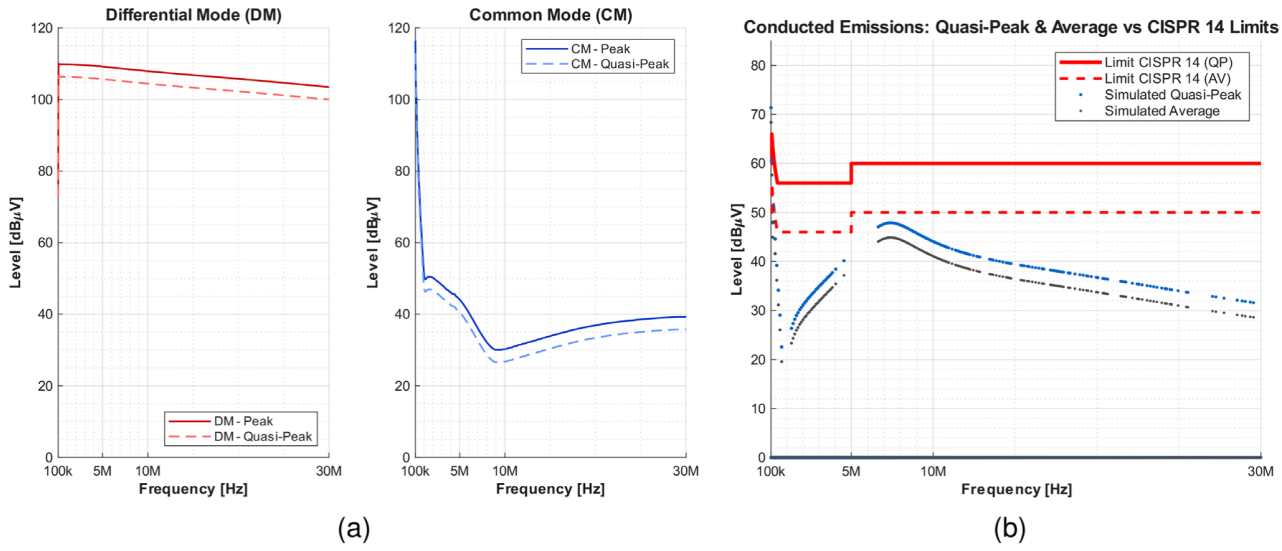

FIGURE 11 | (a) Differential and common-mode conducted noise at the input of the 3 kW SPT, simulated at GeckoCIRCUITS. (b) Total conducted EMI noise at the SPT input after adding the EMI filter, complying with CISPR 14.

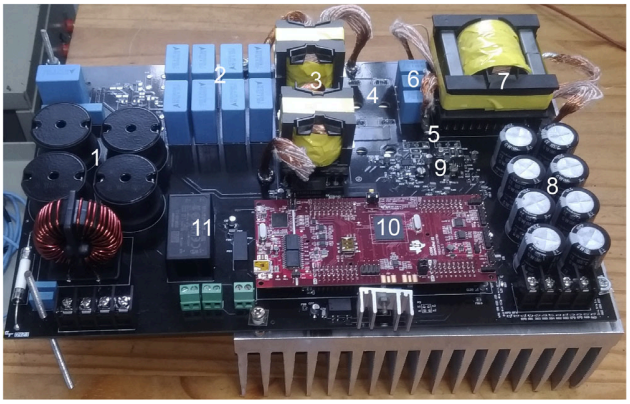

FIGURE 12 | Top view of the prototype for SPT with a minimum switching frequency of 50 kHz and an output power of 3 kW. (1) Two-stage LC input EMI filter. (2) C_{f1} and C_{f2}. (3) L_{in1} and L_{in2}. (4) D_1, D_2, D_3 and D_4 (bottom side of the printed circuit board [PCB]). (5) S_1 and S_2 (bottom side of the PCB). (6) C_b. (7) L_c. (8) C_{o1} and C_{o2}. (9) Gate driver of S_1 and S_2. (10) Signal conditioning, modulation and control circuits. (11) Auxiliary power supplies.

It is recommended that the differential capacitor in the first stage be limited to up to 8 μF to prevent distortions. In the case of the differential filter, the first stage must attenuate more than 50% of the noise and have a cut-off frequency at least one decade below the second stage to avoid oscillations.

The capacitance C_Y for the common-mode stage is selected using Equation (37) to avoid deterioration of the power factor, and is set as a reference to IEC 60950-1 Class I to limit the leakage current to 3.5 mA.

$$C_Y = \frac{I_{leakage}}{1.1 V_{in} 2\pi f_g} \tag{37}$$

The input EMI filter results in $C_{Y1} = 33$ nF, $L_{Y1} = 4$ mH, $L_{X1} = 110$ μH, $C_{X1} = 8$ μF, $L_{X2} = 50$ μH and $C_{X2} = 470$ nF. The total conducted EMI from the input, simulated in GeckoCIRCUITS using the EMI filter and compared with CISPR 14 is presented in Figure 11b.

The virtual neutral is not connected to the network, so the output common voltage of the classical Nabae rectifier varies from $-V_o/2$ to $V_o/2$ at each switching cycle, using the ground of the C_Y EMI filter as a reference. Similarly, the classical interleaved boost rectifier varies from V_o to $V_o/2$ during each switching cycle. Splitting the DC bus with a virtual neutral in the SPT reduces the common-mode voltage to $V_o/4$, also reducing the conducted common-mode EMI noise.

Figure 12 presents the prototype's top view including the EMI filter, auxiliary sources and control circuit.

The SPT is simulated in LTspice to confirm ZVS in S_1 and S_2 at light load, which corresponds to $V_{in} = 220$ V, $P_o = 2.4$ kW, and $f_s = 98$ kHz. Figure 13a presents the simulation results for this condition, where the ZVS occurs. But also, the edge of the sinusoidal current must be analysed, as shown in Figure 13b; this is the critical condition at which the MOSFET starts to lose ZVS due to the low input voltage.

Table 6 lists the instrumentation used for the prototype measurements.

Figure 14a displays the results of the current in L_{in1} and L_{in2} at rated load with f_s equal to 79 kHz. The high-frequency input current is calculated using the oscilloscope's math channel by summing the currents of both inductors. The input current is continuous, and the ripple has a frequency that is twice that of each discontinuous boost cell. The effect of the diode's junction

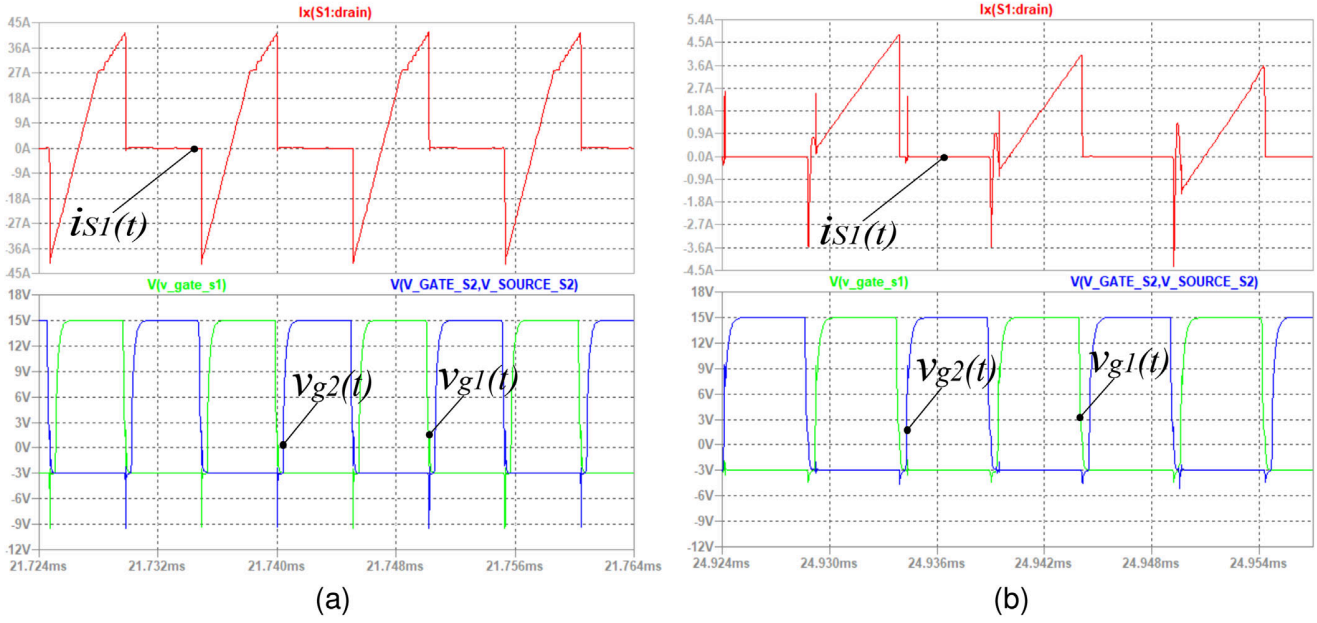

FIGURE 13 | (a) ZVS with maximum input voltage at condition of $V_{in} = 220$ V, $P_o = 2.4$ kW and $f_s = 98$ kHz. (b) Only in the edge of the sinusoidal current, when the input voltage approaches near zero the ZVS is lost.

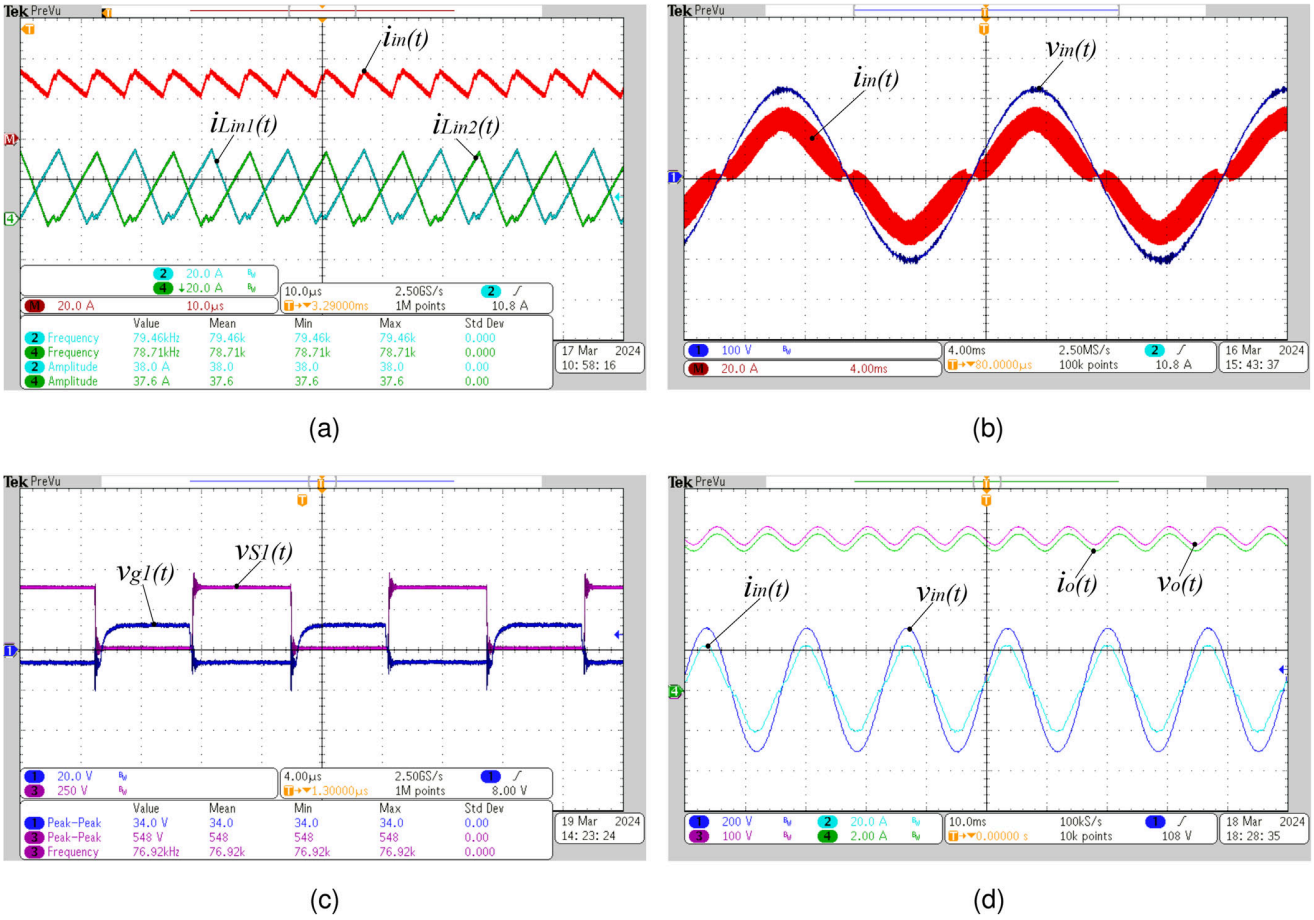

FIGURE 14 | (a) Measurements of the high-frequency interleaved current of L_{in1} and L_{in2}. The measurement utilizes the oscilloscope's math function to sum both waveforms and plot the resulting continuous input current ($i_{in}(t)$) with a ripple twice the switching frequency. (b) Measurements of the input voltage $v_{in}(t)$ and the summed current of L_{in1} and L_{in2}, zoomed in on two cycles of the line network. The equivalent input current ripple is still sufficiently high to require the use of an input EMI filter. (c) Measurements from drain-to-source voltage ($v_{S1}(t)$) and its the gate signal ($v_{g1}(t)$). When $v_{g1}(t)$ rises $v_{S1}(t)$ is already zero, that is, the MOSFET capacitances are discharged and S_1 is switched-on with ZVS. (d) Measurements from input voltage ($v_{in}(t)$) and current ($i_{in}(t)$) followed by voltage and current at load ($v_o(t)$ and $i_o(t)$) at rated conditions. The input current has a sinusoidal waveform due to the EMI filter, which improves the power factor. The load waveforms are 120 Hz, with double the input line network frequency.

TABLE 6 | Instrumentation used to test the SPT.

Equipment	Model/Specifications
Oscilloscope	MSO 3014 - 100 MHz - 2.5 GS/s
Voltage probe	THDP0200 - 200 MHz - 1500 V
Current probe	TCP0030 - 120 MHz - 30 A AC/DC
Power analyser	PA4000

capacitance is noticeable during the period when L_{in} is completely demagnetized, resulting in a slight oscillation.

Figure 14b exhibits a complete view of the equivalent input current without input filter calculated using the math channel. The resulting high-frequency current ripple is significantly reduced compared to the boost cells, but it still requires an EMI filter.

Figure 14c presents the voltage across the drain-to-source and gate-to-source in S_1 at rated input voltage and load to verify the ZVS. The overlapped waveforms confirm that the drain-to-source voltage is null when the gate pulse signal starts to rise, indicating that the MOSFET's intrinsic capacitances have discharged, and S_1 switches on with the forward voltage from its conducting body diode. When part of the discharging current passes through the MOSFET's gate, there is an oscillation in the gate signal waveform.

Figure 14d shows the input and the output voltages and currents using an input EMI filter with rated load. The results from the power analyser that verifies the energy quality are listed in Figure 15a where the converter achieved an efficiency of 92.52%, power factor of 0.99, and input current THD of 12.46%. In Figure 15b, the first 40 current harmonics, for minimum and rated input voltage, are compared to the harmonics from the IEC 61000-3-2 class A standard. The converter complies with the limits, where the fifteenth and the thirty-fifth harmonics are the most critical at rated input voltage. The third harmonic is the most harmful to distort the current waveform with an amplitude of 1.72 A.

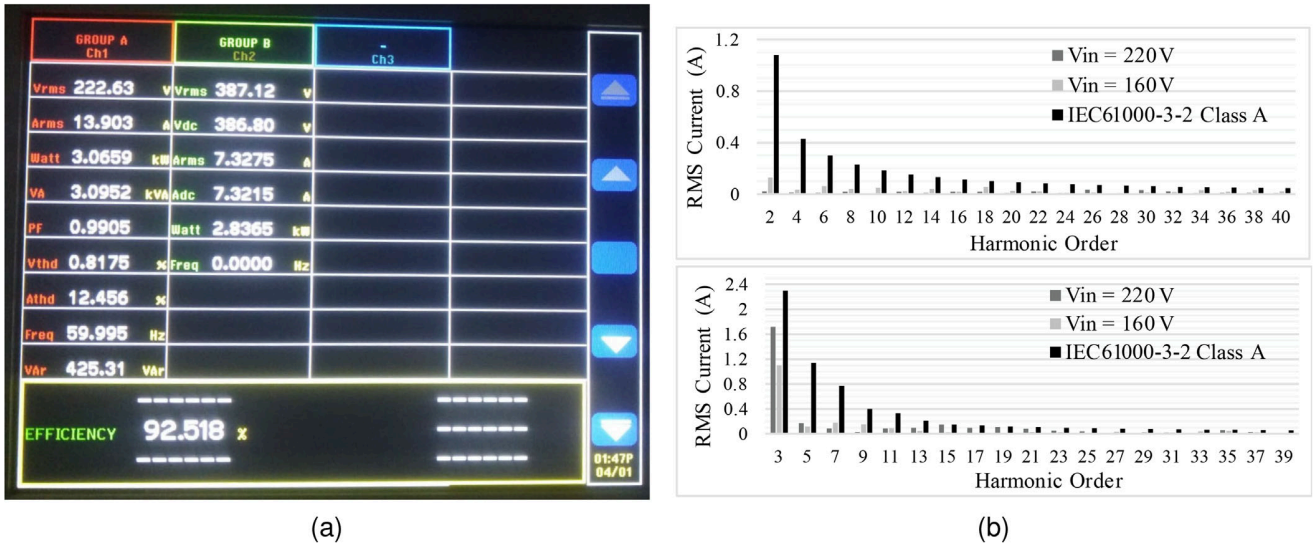

FIGURE 15 | (a) Measurements of SPT power quality. Group A summarizes the measurements from the input and Group B summarizes the measurements from the load. The rectifier achieves a total efficiency of 92.52% at rated conditions. (b) Graphic with the first 40 harmonics of the input current for rated input voltage of 220 V and minimum input voltage of 160 V. Both cases comply with IEC 61000-3-2 Class A limits standard.

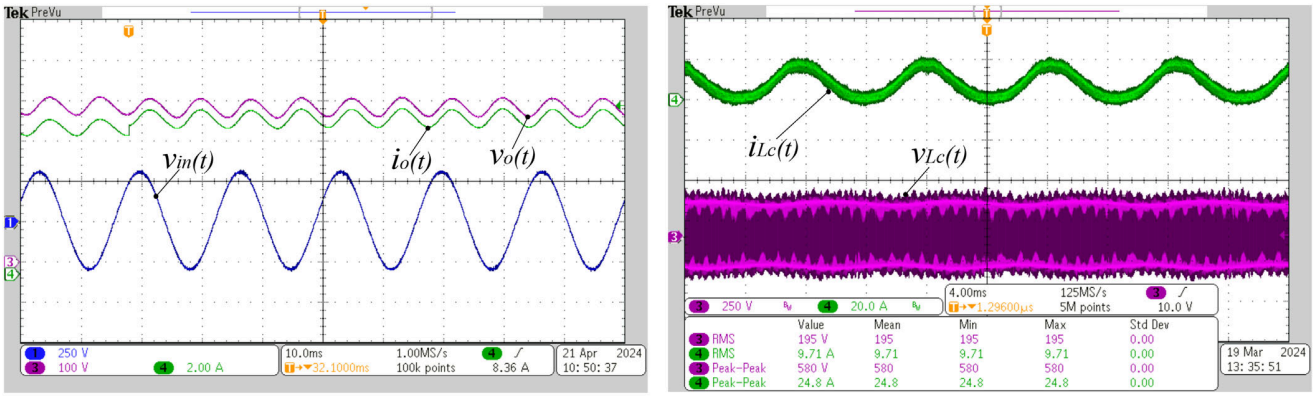

FIGURE 16 | (a) The hysteresis control maintains $v_o(t)$ within the specified limits after a 10% load step, providing a fast dynamic response to control the output voltage. (b) Current reduction in L_c due to the leakage inductance. Despising the leakage inductance, the theoretical value of the current in L_c should be 15.76 A at rated conditions, but due to the leakage inductance of 2.4 μH, the value is reduced to 9.71 A, also reducing the current per capacitor from 3.42 to 1.52 A.

The startup condition of the rectifier, which occurs at a minimum input voltage of 160 V at 2.2 kW and $f_s = 50$ kHz, yields a better THD of 9.25%. This can be explained by the reduction of α, which reduces the deterioration of the odd low-frequency harmonics.

In Figure 16a, the input voltage, along with the output voltage and current, is monitored to test the hysteresis control. The test uses a 10% load step variation with the SPT operating in steady state and rated conditions. During the load step, there is a sudden variation in output current, followed by the regulation of the output voltage.

Figure 17a presents the total efficiency of SPT with rated input voltage of 220 V for three loads of 2.4, 2.7 and 3 kW, where the theoretical values are calculated using the loss equations presented in the previous sections. Figure 17b presents the loss distribution per component. The switches are the main source of losses in the rectifier; in addition, losses increase as the load reduces due to higher switching frequency, which also increases turn-off losses. The maximum switching frequency is around 98 kHz. At this frequency level, the litz wires help reduce losses from skin and proximity effects, thereby reducing the overall losses from L_{in} and L_c. The losses in capacitors also reduce since most harmonics are not in the region dominated by the skin effect. As all sources of losses are decreasing except the turn-off loss from MOSFET, the overall efficiency tends to increase or remain at the same level as presented in Figure 17a, until the critical points are achieved, which are: ZVS loss in most switching cycles, eddy currents dominant at inductors, skin effect dominant at capacitors.

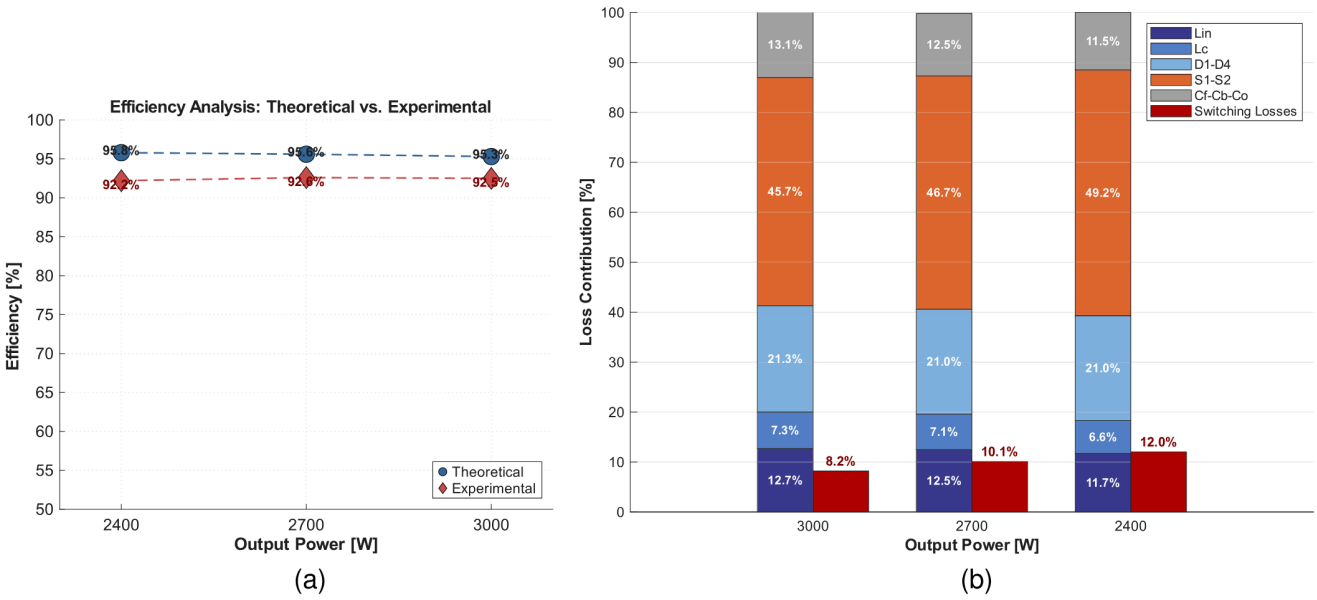

FIGURE 17 | (a) Theoretical and experimental total input efficiency with rated input voltage for loads of 2.4, 2.7 and 3 kW. (b) Loss distribution per component as load decreases. The turn-off loss from the MOSFET represents the main source of loss that increases with frequency.

TABLE 7 | Comparison of the improvement in volume and price of C_o employed in SPT compared to Nabae rectifier due to the virtual neutral and L_c. All capacitors are from Nichicon LGW series, withstanding 3000 h of application of rated ripple current at 105°C.

Rectifier	Model	Voltage (V)	Cap. (μF)	Qty.	Vol. (mm³)	Price (%)	Vol. (%)
SPT	LGW2E271MELZ25	250	270	8	4400	24.9	31.4
Nabae 1	LGW2W271MELA50	450	270	8	10,000	51.9	71.4
Nabae 2	LGW2E271MELZ25	250	270	16	8800	49.7	62.9
Nabae 3	LGW2W561MELC50	450	560	8	14,000	100	100

Figure 16b presents the current and voltage at L_c for rated load conditions. Considering an ideal coupled inductor without leakage inductance, the theoretical value of the current in L_c should be 15.76 A at rated conditions, but due to the leakage inductance of 2.4 μH, the value is reduced to 9.71 A, also reducing the current per capacitor from 3.42 to 1.52 A. As L_c is assembled with litz wires, which reduce eddy currents, it is more interesting to avoid interleaving layers to optimize winding capacitance and use the leakage inductance to reduce the RMS current at C_o.

Table 7 allows a comparison of volume and cost reduction caused by the implementation of a DC bus split with a virtual neutral. It is comparable to the Nabae rectifier designed for the same SPT conditions, but with different capacitor combinations to make C_o. Due to the commercial limitations of electronic capacitors to voltages normally up to 450 V, the three-level output becomes more attractive as the DC bus voltage increases. If the exact same electrolytic capacitors are applied at Nabae and SPT rectifiers, there is a volume reduction of 50% for SPT. By using LGW2W271MELA50 models for 450 V, which can be assembled at the Nabae DC bus without series associations, also results in a volume reduction of approximately 50% to the SPT. At least, using the LGW2W561MELC50 model, which has equivalent capacitance and voltage to the Nabae specifications, results in a reduction of four times the volume of SPT bus capacitors, since it is necessary to assemble more components in parallel due to the high AC current.

5 | Conclusion

In this paper, the TAIPEI rectifier is modified into a single-phase version to be studied as a single-stage PFC rectifier for high-power electrodomestic applications. The topology is an enhancement of the Nabae rectifier, an AC-DC interleaved boost converter with a virtual neutral dividing the switching cells. It uses two complementary DCM boost cells operating in frequency modulation to achieve ZVS and balance the output capacitor voltages. A virtual neutral divides both cells and the output capacitors, providing symmetry and increased immunity to common-mode noise. The virtual neutral along a common-mode inductor splits the output capacitors into two levels, decoupling the DC bus and reducing voltage and current efforts, allowing the use of low-rating electrolytic capacitors. The input current is continuous, with a ripple of double the switching frequency. Changing the voltage gain and the resonance factor of the input LC filters that compose each boost cell improves the input current THD.

TABLE 8 | Single-phase topologies comparison.

Topology	Eff. (%)	THD (%)	PF	P_o (W)	α	f_s (kHz)	μ_o
Nabae rectifier [38]	—	14.20	0.99	75	0.471	10	0.44
Nabae modified with electrolytic caps [39]	83.00	9.20	0.99	85	0.454	52	0.19
Interleaved DCM boost PFC (three-levels) [40]	90.00	10.56	0.99	1000	0.225	40	0.40
Single-phase TAIPEI rectifier	92.52	12.46	0.99	3000	0.404	79	0.24

To analyse the advantages and disadvantages of the rectifier, a 3 kW prototype is developed and tested. At rated conditions the SPT achieves a power factor of 0.99 and complies with IEC 61000-3-2 class A standard, where the third, fifth and seventh harmonics are the most harmful to THD current. Overall, the converter achieves a THD of 12.46% at rated conditions with a switching frequency of approximately 79 kHz. For minimum input voltage and switching frequency of 50 kHz the resulting THD is 9.25%. One of the reasons of this improvement is the reduction of α (0.404 to 0.294), that improves the minimum THD of the input current according to Figure 6a, resulting in reduction of the third harmonic and the others low-frequencies odd harmonics. Deriving the theoretical third harmonic for the input current it is expected to have 11.91% of the amplitude of the fundamental current, the prototype achieves 12.4%. This theoretical value is reduced to 7.4% for an input voltage of 160 V, while the experimentally obtained value is 8.0%. The multiples of the switching frequency with its side-bands do not interfere in these results, since only the first four harmonics are considered.

Table 8 compares the quality features of the SPT with its similar topologies. The lower efficiency of the topology [39] is mainly due to the losses from the two additional diodes applied at the boost cells and by the use of electrolytic capacitors in the input, which have higher equivalent series resistance (ESR) than film capacitors.

The SPT achieves THD and efficiency similar to those reported in [40]. The improved efficiency could be attributed to the reduced number of semiconductors and the higher switching frequency, which benefits overall efficiency through ZVS. A worse THD is related to the voltage gain α, which impacts the demagnetizing time of the boost cells and the amplitude of the odd harmonics.

The semiconductor components are responsible for approximately 67% of the topology losses at rated conditions. Conduction losses are critical due to the large current ripple in each cell; therefore, it is necessary to use semiconductors with low forward voltages and conduction resistances. Switching losses are reduced by ZVS in the transistors and the absence of reverse recovery losses in the diodes, allowing the rectifier to be designed to operate at high frequencies to reduce conduction losses and to optimize volume from the boost cells and the output common-mode inductors.

A simple hysteresis controller is sufficient to maintain the rectifier's stability, as the boost inductor's current naturally follows the sinusoidal input voltage. It is only necessary to control the output DC bus by limiting the low-frequency voltage ripple. At rated conditions, the 3 kW prototype achieves an overall efficiency of 92.52%.

Author Contributions

Rodrigo Heinrich: conceptualization, formal analysis, investigation, methodology, software, validation, writing – original draft. **Yales Romulo de Novaes:** conceptualization, investigation, methodology, supervision, writing – review and editing. **Sergio Vidal Garcia Oliveira:** conceptualization, funding acquisition, investigation, methodology, project administration, supervision, writing – review and editing.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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