A SIMPLE CONTROL SCHEME TO A VOLTAGE REGULATOR BASED IN A CURRENT CONTROLLED STATCOM

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***Abstract* – This work shows a simplified control scheme to a Static Synchronous Compensator (STATCOM) based regulator, used to regulate the voltage magnitude in AC low voltage grids. The system regulates the voltage through injection of reactive power at the point of common coupling (PCC). The regulator was implemented by a three-phase four-wire current-controlled voltage source converter (VSC), connected in shunt with the PCC. The reactive power processed by converter is responsible to regulate the PCC voltage while the active power is responsible for the control of the DC bus voltage. In this paper it is presented the control design and some experimental results of a 4.5kVA implemented prototype.**

***Keywords* – Power Quality, STATCOM, Voltage Regulation.**

I. INTRODUCTION

Nowadays there is an increasingly electrical energy consume that goes together with country growing and leads more and more electrical equipment to suffer with the voltage variations in the electrical distribution grid. Aiming to organize Brazilian electrical scenario, the *"Agência Nacional de Energia Elétrica"* (ANEEL), elaborated the Brazilian Electric Power Distribution Procedures (PRODIST). The PRODIST get together a set of documents prepared by normalizing and standardizing the technical activities related to the operation and performance of the electric power distribution system.

The section 8 of PRODIST [1] classifies the voltage standards in three ranges: adequate, precarious and critical. When the voltage at consumer exceeds the adequate range, the power distribution company has a time deadline to solve the problem and bring the voltage to adequate levels, which are 90 and 15 days for voltages in the precarious and critical ranges respectively.

The solution to solve the regulation problem can requires a lot of time to find a definitive solution, higher than ANEEL deadline. This situation suggests a temporary device able to adequate the voltage level until the electric distributor find out a definitive solution. The features of the device should bring some features for this application, like low volume, fast voltage regulation, and easy installation. To achieve these features, could be used the concept of "*flexible ac transmission systems"* (FACTS) [2], it is static devices that interact and manipulate active and reactive power from the power system to improve the capacity of power transmission and voltage regulation. Several converters topologies were developed to FACTS [3]. Some of these topologies can also be applied in voltage regulation since that reactive power is correlated with the voltage magnitude [4]. One of these topologies applied to voltage regulations are called of *Static Synchronous Compensator* (STATCOM) [5, 6, 7], that basically uses a *Voltage Source Inverter* (VSI) associated with an output filter and a control scheme. This converter has some desired features to be applied in voltage regulation, presenting low volume, good linearity in the reactive power injection and control flexibility that can be adapted in different distribution grids [8].

The main objective of this work is present a voltage regulator based in a current controlled STATCOM with a simple analogic control technique.

II. PROPOSED CIRCUIT

The voltage regulator proposed is based in a three-phase voltage source inverter with center-tapped DC bus to four-wire connections. The converter is shunt-connected with the low voltage utility grid at point of common coupling (PCC) through a high frequency passive LC filter (Inductor and Capacitor). To control the voltage at PCC, the converter emulates a variable reactive load, capacitive or inductive, depending on the voltage magnitude. The Figure 1 shows a basic diagram of the proposed regulator. The design specifications to the regulator are shown in Table I.

Table I
Design specifications

Grid voltage	$V_{grid} = 127\ V_{RMS}$
Grid frequency	$f_{grid} = 60$ Hz
Series inductance of the grid	$L_{grid} = 2.7\ mH$
Series resistance of the grid	$r_{grid} = 0.3\ \Omega$
DC bus voltage	$V_B = 600$ V
Output inductance filter	$L_f = 1100$ µH
Output capacitance filter	$C_f = 4$ µF
DC bus capacitance	$C_O = 1$ mF
Switching frequency	$f_S = 50$ kHz
Attenuator gain from current loop	$K_{ati} = 0.64$
PWM gain	$K_{PWM} = 0.09\ V^{-1}$
Current sensor gain	$K_{s\_i} = 0.068$
Attenuator gain, DC bus total voltage	$K_{at\_tv} = 0.21$
Multiplier gain, direct reference	$K_{md} = 0.1$
Multiplier gain, reference in quadrature	$K_{mq} = 0.1$
Voltage sensor gain from DC bus total	$K_{s\_vt} = 0.01$
Attenuator gain, DC bus diff. voltage	$K_{at\_dt} = 1$
Voltage sensor gain, DC bus diff.	$K_{s\_dt} = 0.01$
Attenuator gain from PCC voltage loop	$K_{at\_PCC} = 0.84$
AC voltage sensor gain	$K_{v\_PCC} = 0.01$
RMS to DC gain	$K_{RMS\_DC} = 0.64$
Resistance of RMS converter	$R_{RMS} = 8$ kΩ
Capacitance RMS converter	$C_{RMS} = 15$µF

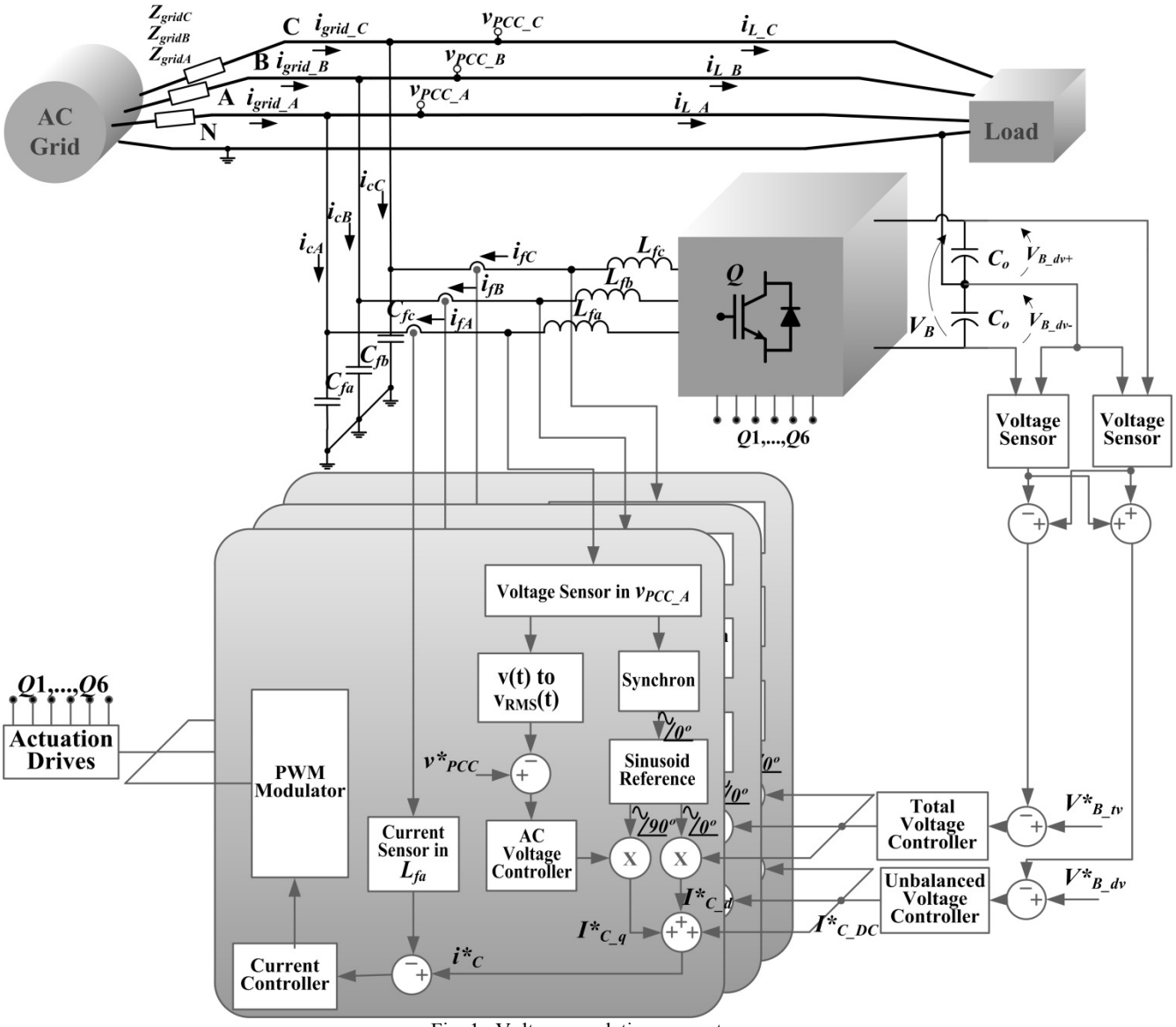

Fig. 1. Voltage regulation converter.

The grid's specifications are used only for the grid where the equipment was projected. If an energy distribution company wants to install it, the same will need to know the features of the grid where it will be installed and introduce this parameters on interface of converter. And then it can project a new control specification (its implementation will be a future work).

The design of the power circuit was presented in [9] and was not discussed in details in this paper.

The limitation of voltage control, that means the maximum reactive power connected in a PCC, is given by maximum current on output of converter, that is 12A, and the maximum transformer's capacity. Where the power of loads summed with the power drained by converter must not be higher than transformer's power.

The STATCOM count with a good regulation of voltage in substation and is helped by an inductivity model of distribution grid. This way is possible to compensate the voltage where the load is located working similar a shunt capacitor compensation, see [4], once that the current of converter is 90 degree phase shifted with PCC's voltage. This way the angle of converter's current change identically the angle of PCC's voltage in relation to voltage of substation.

III. CONTROL DESIGN

The main objective of the control scheme is to regulate the voltage at PCC feeding or draining a sinusoidal current with a displacement of the 90 degrees in relation to PCC voltage, performing a reactive power circulation between the converter and the PCC. The regulator also drains a small portion of active power necessary to regulate the dc-bus voltage, which drops by converter losses. Due to the DC bus has a center-point configuration, an additional voltage equalization control is necessary. The complete description of the derivations of control models is presented in [10].

The project of controls contemplates a phase margin upper than 30º that gives stability to the loops of control.

A. Current Loop

The current loop is shown in Figure 2.

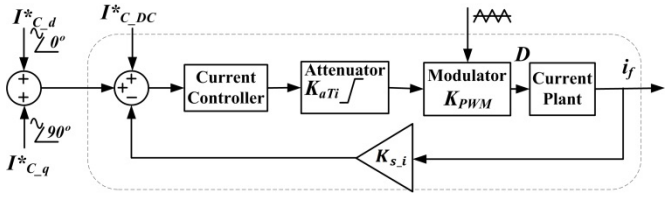

Fig. 2. Current loop block diagram.

The reference of current loop is composite for a sum of three references, the first one ($I^*_{C\_d}$) is in phase with PCC voltage and is related with active power of converter. The second ($I^*_{C\_q}$) is phase shifted at 90 degree of PCC voltage and is related with the reactive power of converter. This both current references are generated by a digital module, it synchronizes the references with the PCC voltage, through zero crossing detection, and available both signals for the analogic circuit, where the controllers are implemented. The third reference, called of DC reference ($I^*_{C\_DC}$) is generated by the differential voltage controller, which is one of two DC bus voltage controllers.

The technique of zero crossing detection was used just for its simplified implementation, but it allows deviation of synchronizes of fundamental voltage. There is robustness techniques as phase locked loop (PLL), which are robust against harmonics presenting on PCC voltage for example, it should be used in a further work.

The attenuator gain is a technique used to limit the saturation value of some signal, as ampop output, where is connected a resistive divisor at its output. This way the maximum value of voltage will be the maximum ampop's voltage multiplied by the resistive divisor gain.

The current controller should track the reference even with the presence of harmonics in the PCC voltage, meaning that the bandwidth of this loop should be high enough, being able to impose current at the fundamental frequency, aging faster than PCC voltage's harmonics. Although this loop is projected for a nonlinear loads connected at PCC, this situation were not implemented by this work. The authors believe on this solution because the plant of current do not changes with power grid harmonic content, see equation (1). A next work will contemplate results with nonlinear loads.

The current plant model is presented in [11] and given by the following equation:

$$Gi_f(s) = \frac{V_B}{s \cdot L_f} \tag{1}$$

The open loop transfer function is given by the following equation:

$$FTLA_i(s) = K_{at_i} \cdot K_{PWM} \cdot Gi_f(s) \cdot K_{s\_i} \tag{2}$$

The current loop implemented uses a PI controller with an additional high frequency pole. The current loop frequency response is shown in Figure 3.

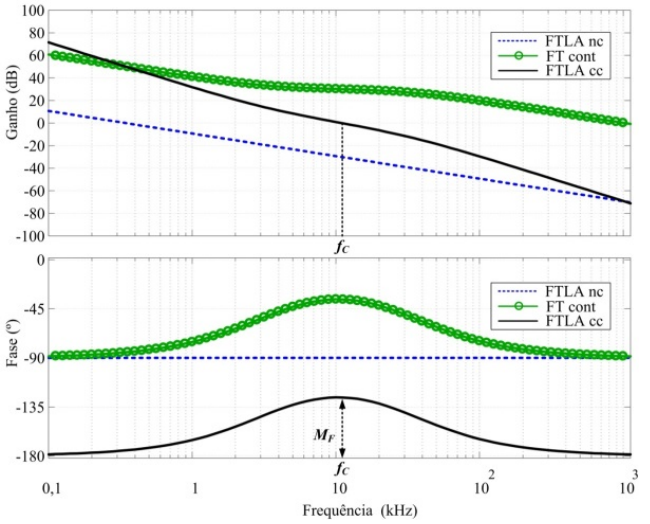

Fig. 3. Current loop frequency response.

The crossing frequency of the compensated system is 11 kHz and phase margin is about 50º. This frequency is around 180 times grid frequency and it allows a very quickly compensation by current's controller, allowing the same to follow its reference and enable the converter to have a sinusoidal current only. The value of 11 kHz is a frequency lower than a quarter of commuting frequency, allowing an analysis of controller by quasi instantaneous mean values in the project of controller.

As the current loop is so faster than other loops it will be considered as a constant gain for them.

B. DC Bus Total Voltage Loop

The total voltage loop of the DC bus is shown in Figure 4.

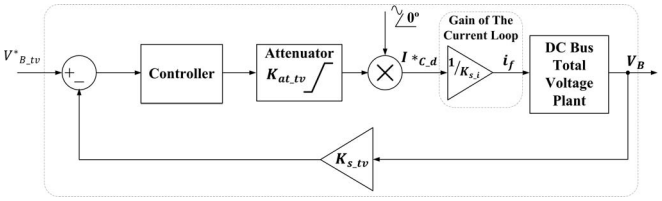

Fig. 4. DC bus total voltage loop.

This control loop is responsible for regulate the total DC bus voltage by feeding or draining active power to the grid. This is possible because the voltage controller acts increasing or decreasing the amplitude of the current in phase with the PCC voltage ($I^*_{C\_d}$). To avoid current distortion, the bandwidth of this controller should be less than $f_{grid}/10$.

The total DC voltage plant model is presented in [11] and given by:

$$G_{VB\_tv}(s) = \frac{3}{2} \cdot \frac{V_{grid\_pk}}{V_B} \cdot \frac{1}{s \cdot C_o} \tag{3}$$

Where:

V_{grid_pk} – Peak voltage at PCC

The open loop transfer function is given by:

$$FTLAtv(s) = K_{at\_tv} \cdot K_{md} \cdot \frac{1}{K_{s\_i}} \cdot G_{VB\_tv}(s) \cdot K_{s\_tv} \tag{4}$$

The total voltage loop implemented also uses a PI controller with an additional high frequency pole, and its frequency response is shown in Figure 5.

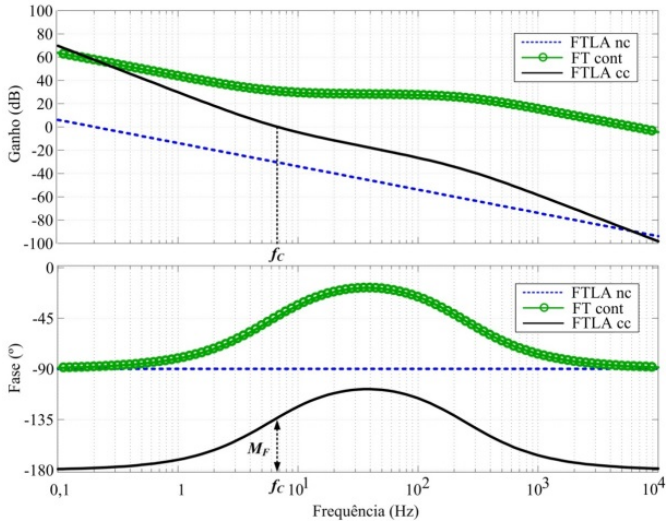

Fig. 5. Total DC bus voltage loop frequency response.

The crossing frequency of the compensated system is 7 Hz and phase margin is about 35º, being a stable loop into of f_{grid}/10 value.

C. DC Bus Differential Voltage Loop

The differential voltage loop of the DC bus is shown in Figure 6.

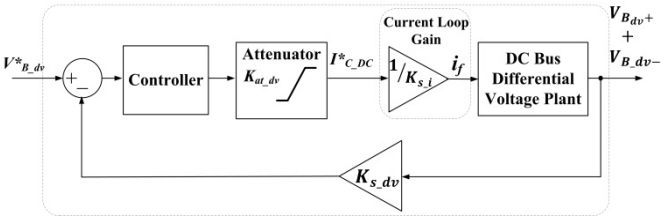

Fig. 6. DC bus differential voltage loop.

This control loop is responsible to eliminate DC bus voltage imbalances by adding a DC level in the current loop reference. This DC level injection allows dispatching a different active power to each capacitor of the DC bus, regulating the voltage imbalances. To avoid an interaction with the total voltage loop, this control bandwidth should be less than f_{grid}/30.

The DC bus differential voltage plant model is presented in [11] and it is given by:

$$G_{VB\_dv}(s) = \frac{3}{2 \cdot s \cdot C_o} \tag{5}$$

The open loop transfer function is given by:

$$FTLA_{VB\_dv}(s) = K_{at\_dv} \cdot \frac{1}{K_{s\_i}} \cdot G_{VB\_dv}(s) \cdot K_{s\_dv} \tag{6}$$

The differential voltage loop also was implemented using a PI controller with an additional high frequency pole, and its frequency response is shown in Figure 7.

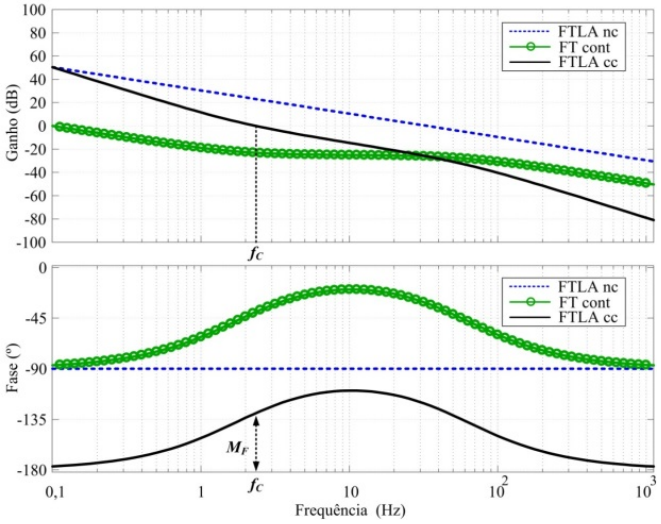

Fig. 7. DC bus differential voltage loop frequency response.

The crossing frequency of the compensated system is 2 Hz and its phase margin is about 50º, being a stable loop and into f_{grid}/30 value.

D. PCC Voltage Loop

The PCC voltage loop is shown in Figure 8.

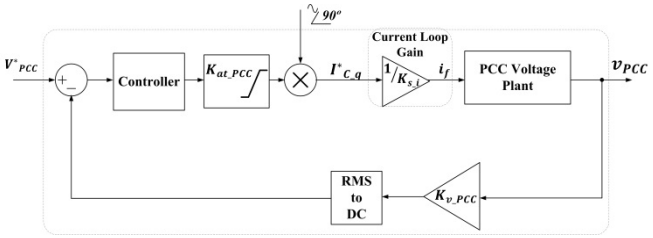

Fig. 8. PCC voltage loop.

This control loop is responsible for regulate the PCC AC voltage by feeding or draining reactive power to the grid. This is possible because the voltage controller acts increasing or decreasing the amplitude of the current ($I^*_{C\_q}$) which is with 90º of phase shift in relation to PCC voltage. To avoid current distortion, the bandwidth of this controller also should be less than f_{grid}/10.

The PCC voltage plant model is presented in [10] and it is given by:

$$G_{VPCC}(s) = \frac{v_{PCC}(s)}{i_f(s)} = \frac{\frac{1}{C_f} \cdot \left(s + \frac{r_{grid}}{L_{grid}}\right)}{s^2 + s\frac{r_{grid}}{L_{grid}} + \frac{1}{L_{grid} \cdot C_f}} \tag{7}$$

The PCC open loop transfer function is given by:

$$FTLA(s) = K_{at\_PCC} \cdot K_{mq} \cdot \frac{1}{K_{s\_i}} \cdot G_{VPCC}(s) \cdot K_{v\_PCC} \cdot G_{rms}(s) \cdot K_{RMS\_DC} \tag{8}$$

Where the transfer function of RMS to DC converter is given by:

$$G_{rms}(s) = \frac{1}{s \cdot R_{RMS} \cdot C_{RMS} + 1} \tag{9}$$

The PCC voltage loop also was implemented using a PI controller with an additional high frequency pole, and its frequency response is shown in Figure 9.

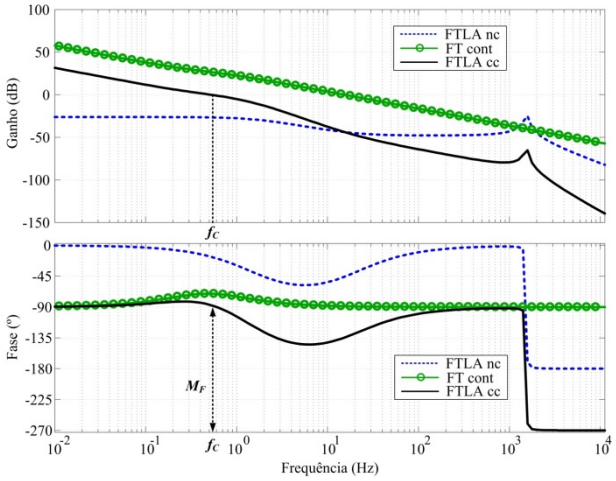

Fig. 9. PCC voltage loop frequency response.

The crossing frequency of the compensated system is 0.5 Hz and phase margin is about 90º. It is a stable loop and was projected with such a low frequency to avoid oscillation on controller's output.

As seeing at equation (7), the parameters of grind (resistance and inductance) are included in PCC voltage model, this way the controller are projected with its parameters fixed, for a future work the controller should be digital where the customer could insert the parameters of the grid and then the PCC controller will be projected automatically by a digital module on a digital controller. Nowadays it is projected only for specific features of grid.

IV. EXPERIMENTAL RESULTS

A 4.5kVA prototype was built to validate the proposed project and it is shown at Figure 10.

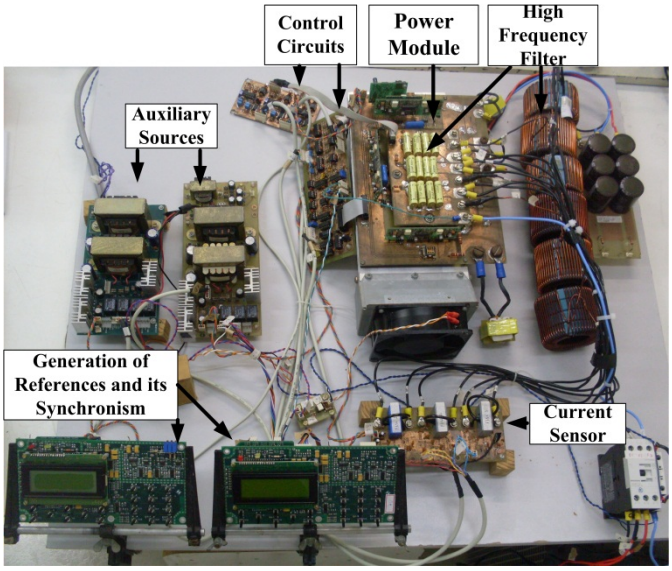

Fig. 10. Prototype implemented.

The design specifications was presented in Table I and the load description is presented in Table II.

Table II
Load description

Active power	6 kW
Reactive power	7 kVAr
Power factor	$0.7_{\text{inductive}}$

The experimental results were obtained through sampling by a Tektronix® oscilloscope, model TPS 2024, and after that, the set of points were reconstituted using the software MATLAB®, without using any type of filtering.

Figure 11 shows the PCC voltages and grid currents at full load and without voltage regulation. The voltage magnitudes are 113 V*rms*, 115 V*rms* and 114 V*rms* to the phases A, B and C phases respectively and the current in the grid is 23.5 A*rms*. According to PRODIST, in this case the PCC voltages are considered in precarious range.

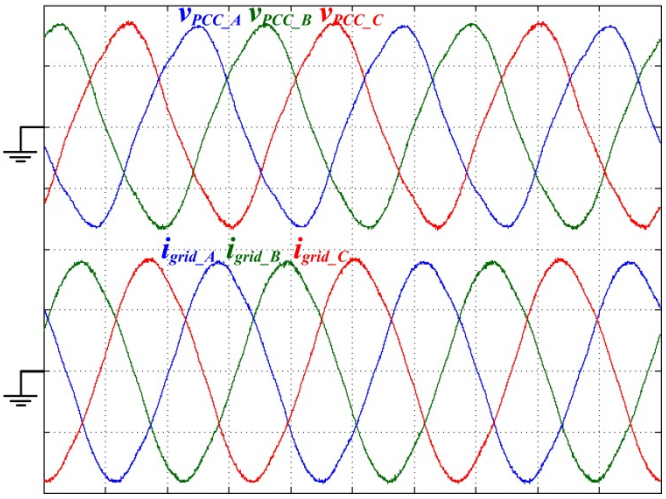

Fig. 11. PCC's voltage and grid's current under full load and without compensation (100 V/div, 20 A/div, 5ms/div).

Figure 12 shows the PCC voltages, grid currents at full load with voltage regulation and converter's current (i_C). The PCC voltages in all phases are 118 Vrms, and the grid currents are 22.1 Arms, 23.5 Arms and 22.7 Arms to the phases A, B and C respectively. The currents in the voltage compensator are 7.7 Arms, 4.4 Arms and 7.5 Arms to the phases A, B and C respectively. According to PRODIST, with the regulator active the PCC voltages is considered inside of the adequate range.

Although the grid current did not have its current reduced, the power drained of load had an increase of around 6% for the same power drained from the grid. It occurs because the converter is supplying a parcel of reactive load to compensate PCC's voltage.

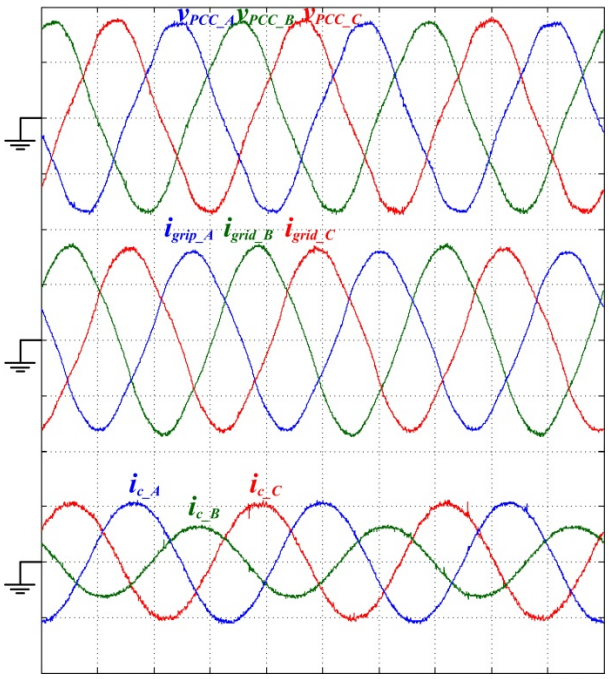

Fig. 12. PCC voltages, grid currents and regulator currents at full load and with compensation (100 V/div, 10 A/div, 10 A/div, 5 ms/div).

To simulate variation in PCC's voltage, and variations of load features, the Figure 13 shows the behavior of RMS PCC voltage in all 3 phases during a 100% to 10% load step and a 10% to 100% load step. Right after the load reduction, the PCC voltages increases up to 140 Vrms and in approximately 100ms it returns to the adequate level. In the same way approximately 450ms after the load increasing the PCC voltage gets the adequate level. As seeing in [1], at item 2.7.1.1 (that mention its item 2.6.2.1 and makes reference to its table 9), voltage variation up to 3 seconds are not considerate in calculus of voltage classification. This way the dynamic of converter is enough to avoid penalty to energy distribution company, still do not mitigate some voltage variation in very short periods.

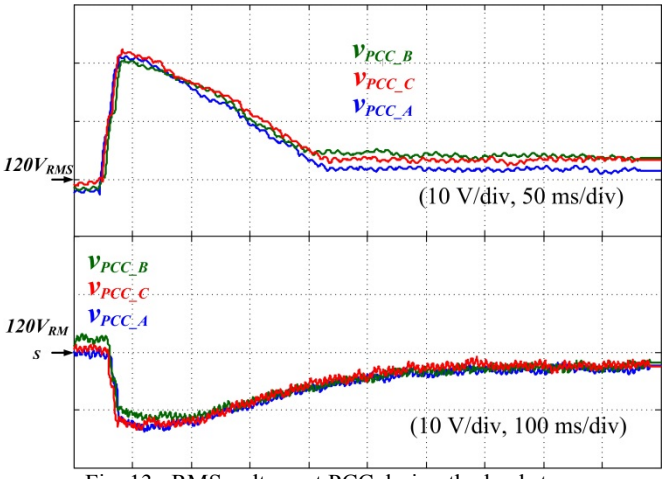

Fig. 13. RMS voltage at PCC during the load steps.

Figure 14 shows the PCC voltage, grid current and regulator current to the phase A during a 100% to 10% load step. As can be observed, before the load step the PCC voltage was regulated in 118 Vrms and the grid current was 23 A. After the load step, the PCC voltage increases until 134 Vrms and then the regulator act draining its maximum reactive power to regulate the PCC voltage in 122 Vrms. A similar situation occurs with other phases.

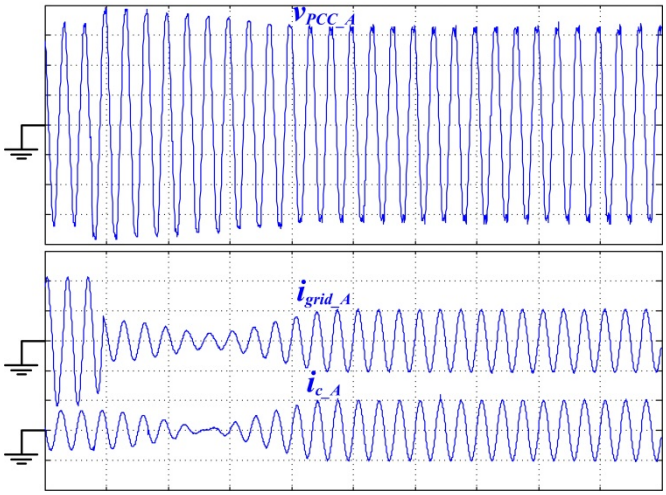

Fig. 14. PCC voltage, grid current and regulator current during a load step. (50 V/div, 15 A/div, 50 ms/div).

The DC link voltages are presented in Figure 15. After the loads steps the control of DC bus voltage keeps it on its specified value, which is 300V.

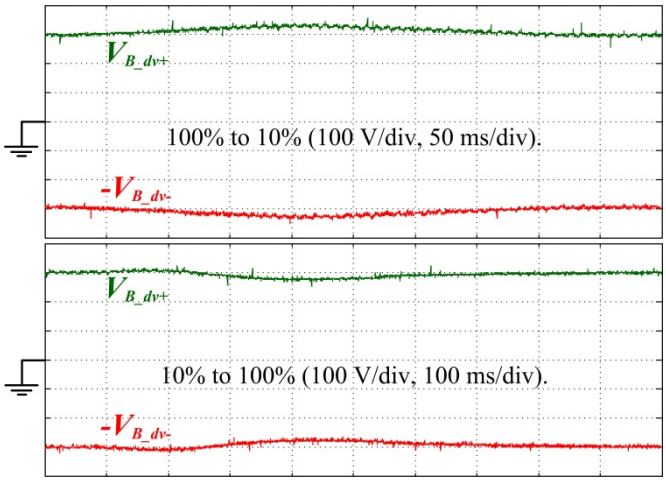

Fig. 15. DC link voltage during load steps.

The harmonics on the current of the converter is shown in Figure 15. Its respectively *Total Harmonic Distortion* (THD) are presented in Table III.

Table III
Load description

Phase A	3.2%
Phase B	4.2%
Phase C	4.0%

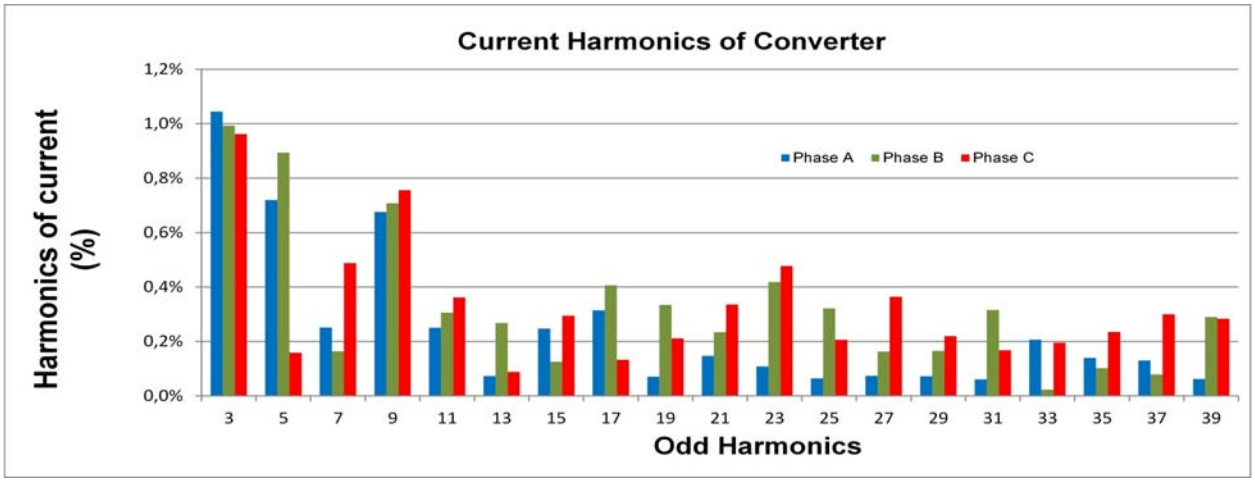

Fig. 15. Converter's current harmonics

V. CONCLUSION

This paper presented a single control scheme to a three-phase voltage regulator based in a current controlled STATCOM.

It has presented a complete control design including the current loop, total and differential DC bus loops and the PCC AC voltage loop.

Experimental results to a 4.5kVA regulator confirm that the proposed control scheme works fine and can be a simple and good option to STATCOM based regulators.

The PCC voltage was maintained in an adequate level even under the loads steps, presenting a fast dynamic enough to comply with the PRODIST standards required by ANEEL. The output current of the converter is keeping sinusoidal, injecting only the reactive power needed to the PCC voltage regulation. The total voltage and the differential voltage of the DC bus kept regulated even when the converter works with maximum reactive power.

VI. ACKNOWLEDGEMENTS

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