COMPARISON BETWEEN A HYBRID MULTILEVEL CONVERTER EMPLOYING HALF-BRIDGE MODULES AND A HYBRID MULTILEVEL CONVERTER EMPLOYING H-BRIDGE MODULES

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***Abstract* - The Hybrid Cascaded Half-Bridge (HC$^1/_2$B) converter is a multilevel circuit topology that is able to replace a Hybrid Cascaded H-Bridge (HCHB) converter regarding voltage vector generation, modularity and other features. However, there is not a complete correspondence between the converters since they present different operation principles. This work presents a comparison between the (HC$^1/_2$B) and the (HCHB). The converters are analyzed in their four-level versions, but the results are valid for other configurations. The comparison comprehends the power semiconductors, the generated voltages, the isolated dc supplies and the dc-link capacitors. It is shown that the main differences are with the dc link capacitors. Thus, these are analyzed in detail and a modeling procedure to design and compare them is proposed.**

***Keywords* – Multilevel converters, Hybrid converters, PWM modulation, Three-phase inverters.**

I. INTRODUCTION

Medium voltage (MV) applications involving high power converters have seen rapid development in recent years with the wide spread deployment of multilevel converters. Several converter topologies [1–14] are responsible for the observed development in this field of Power Electronics. Some of the MV application areas are high power motor drives, flexible ac transmission systems (FACTS), high power uninterruptible power supplies (UPS), wind power generation and power quality among others. Typical MV multilevel converters are the neutral (diode) clamped converters (NPC), the capacitor clamped converter (FC), the cascaded H-bridge converter (CHB), the hybrid Voltage Source Inverter plus cascaded H-bridge converters (HCHB) and the active neutral clamped converters (ANPC).

Hybrid multilevel topologies employing three-phase two-level VSI or NPC cascaded in each phase with series connected H-bridge modules (HCHB) have been proposed in works such as [5, 8, 15–17] as an alternative to the CHB. Another hybrid solution has been proposed in [18, 19], where a three-phase two-level inverter is series connected to pairs of half-bridge modules (HC$^1/_2$B). In these topologies the number of semiconductor components is similar to the CHB given the same number of voltage levels. An advantage is that the three-phase converter presents more favorable operating conditions due to reduced dc-link capacitor current and voltage efforts. Thus, the requirements for the insulation transformers and for the main capacitive dc-link storage are lessened. Both converter topologies have their asymmetric versions presenting advantages and drawbacks depending on the specific application and available switch technology. Even though several works have been published regarding both hybrid converters, a comparison between them lacks in the literature.

This work presents a comparison between the (HC$^1/_2$B), as shown in Fig. 1(a), and the (HCHB), which is shown in Fig. 1(b). The converters are presented with a three-phase VSI cascaded with three single-phase bridge modules in their four-level version, i.e. $V_x = V_y$. Both topologies can have a higher number of cascaded single-phase bridges leading to higher ac-side voltage levels. However, a comparison employing the circuits given in Fig. 1 suffice in the sense that further cascaded modules would present similar characteristics as the ones considered here. This analysis involves the number of components and their voltage and current efforts, the output voltages total harmonic distortion (THD), the required number of dc isolated sources, the power processed by each dc source, conduction and switching losses and the number of dc-link capacitors. A design procedure to compute the required capacitance for a given dc-link voltage ripple and the rms current of the dc-link capacitors is proposed to better accomplish the aimed comparison.

II. DC- LINK CAPACITORS DESIGN FOR CASCADED SINGLE-PHASE MODULES

The dc-link capacitors in the single-phase bridge modules are highly stressed devices in a cascaded multilevel converters [20,21]. Therefore, this section presents an analytical procedure to determine voltage ripple and current stress expressions that are used in the following comparison among hybrid converters.

Two parameters are typically used in the dimensioning of dc-link capacitors, namely: (*i*) the maximum dc-link voltage ripple and, (*ii*) the capacitor current. The dc-link capacitors in cascaded multilevel inverter topologies can influence the harmonic distortion in the output ac voltages of the inverter. This is due to the fact that the dc-link voltages in cascaded single-phase bridge modules supplied by multipulse rectifiers with finite dc-link capacitance present voltage ripple with pronounced second harmonic contents. Assuming no second order effects, the ac voltages result from the multiplication of the dc-link voltages by the inverter switching functions. Therefore, compensation techniques are required to eliminate the influence of the dc-link voltage ripple in the quality of the ac volta-

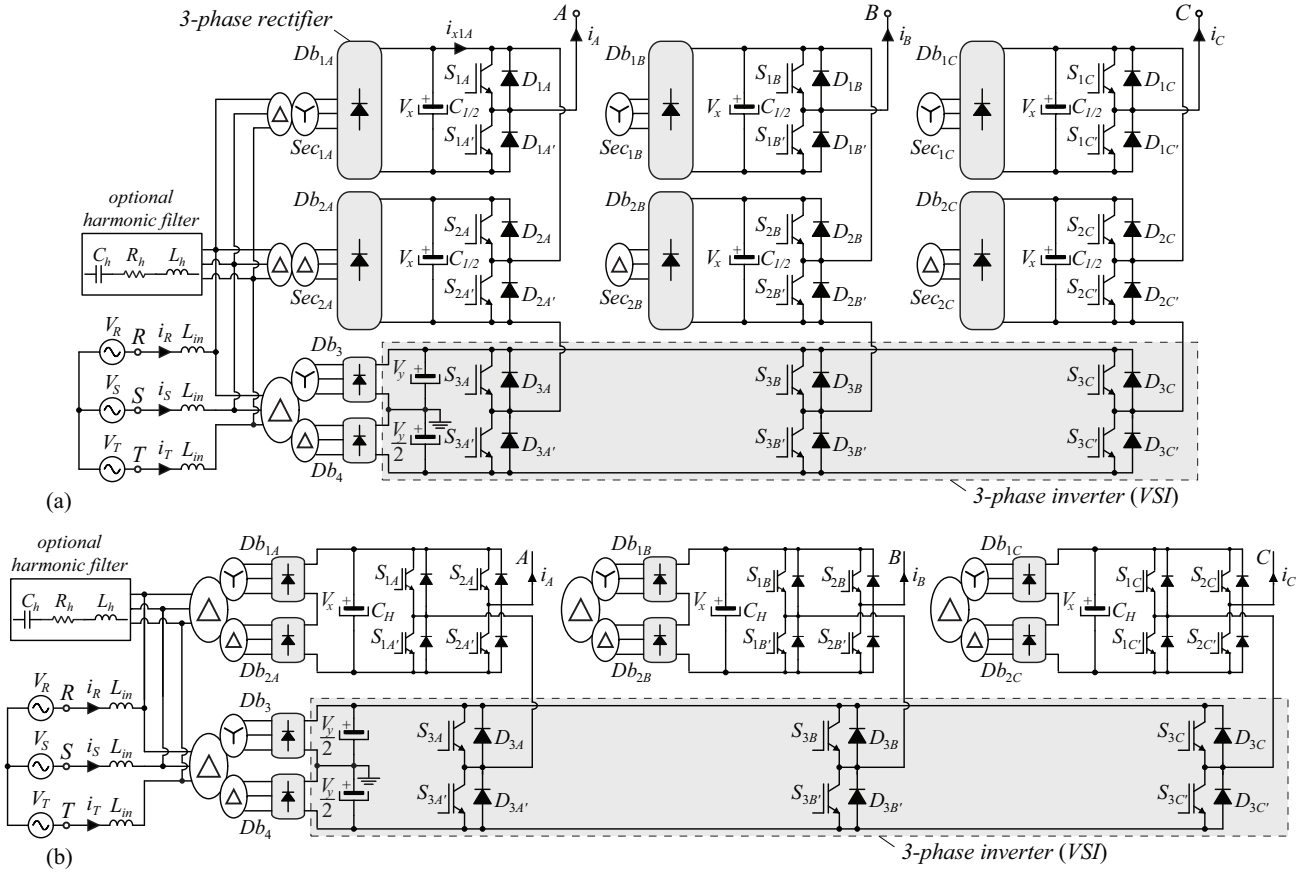

Fig. 1. : (a) Circuit schematic of the proposed hybrid multilevel converter employing half-bridge modules and a three-phase inverter. Further pairs of half-bridge modules can be connected in series at each phase-leg. (b) Circuit schematic of the hybrid multilevel converter employing full-bridge modules and a three-phase inverter.

ges or the dc-link capacitors are required to present very high capacitance values. Each dc-link capacitor in a cascade multilevel inverter is a costly component. In some cases the total capacitors cost represents more than 50% of the cost in a multilevel power module [20]. Thus, the main defining physical parameter to design a dc-link capacitor assembly in such converters is their temperature rise. This is defined by the construction (type of capacitor), which leads to a given equivalent series resistance (ESR) and thermal impedance characteristics. The ESR models the loss generation mechanism in the capacitors, where a capacitor power losses P_C are given by

$$P_C = \text{ESR} \cdot I^2_{C,\text{rms}}, \tag{1}$$

where $I_{C,\text{rms}}$ is the capacitor rms current. These losses generate heat in the component, which must be adequately handled in order to keep dielectric temperatures under safe operating conditions. In summary, the capacitor rms current is ultimately the main physical quantity for the dimensioning of the dc-link capacitors in cascaded multilevel applications for a given capacitor construction technology.

Applying Kirchhoff's current law to the circuits in Fig. 1 show that two currents form the dc-link capacitors current in the single-phase bridge modules. This leads to the simplified circuits shown in Fig. 2, where currents $I_{dc,j}$, with $j = {}^1\!/_2, H$, model the rectifier-side currents in the half-bridge and H-bridge modules, respectively. Whereas, $i_{inv,j}$ represent the inverter-side currents. Thus,

$$i_{c,j} = I_{dc,j} - i_{inv,j}, \tag{2}$$

which is used in the following to find the main capacitor design parameters for both converters. Currents $I_{dc,j}$ are highly

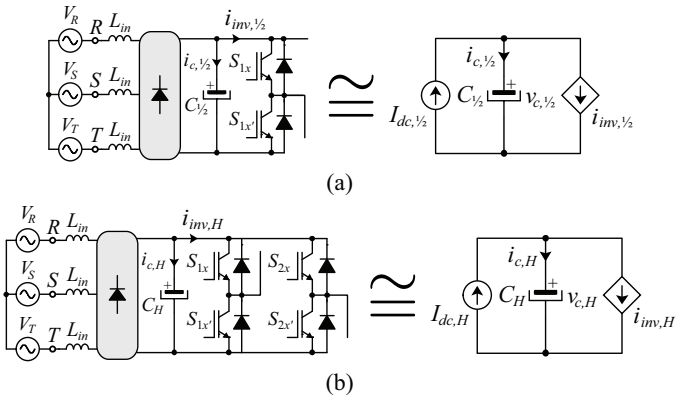

Fig. 2. : Simplified models to calculate the capacitance and the RMS current of the rectifier capacitors. (a) Simplified model for half-bridge converters and (b) simplified model for full-bridge converters

complex non-linear waveforms that depend on the inverter current, grid and inverter frequency, multipulse rectifier configuration, transformer leakage inductance, grid-side impedance, switching frequency, inverter modulation pattern and circuit voltage levels. In order to reduce the complexity of the proposed model, this current is assumed to be a pure dc current, i.e. high rectifier inductances are assumed. The validity of this assumption will be evaluated in section III. Furthermore, this section addresses only the local average values of the current, i.e. the switching frequency components are neglected.

A. Cascaded Half-Bridge Modules

The current that is fed to the inverter $i_{inv,1/2}$ is dependent on the modulation pattern that drives each inverter. The adopted modulation strategy drives the 3-phase inverter at the fundamental frequency while the half-bridge modules switch at the switching frequency. This pattern has been presented in details in [18]. The rectifier-side current is modeled with the constant dc current $I_{dc,1/2}$. The peak currents of the input rectifiers are not considered in the model due to this simplification. However, this methodology allows to obtain closed form expressions for comparing the dc-link voltage ripple and the rms current in the capacitors of both hybrid converters. Furthermore, the following assumptions are made for the analysis: (i) the switching devices and the capacitor are ideal. i.e. lossless; (ii) parasitics are neglected; (iii) the output current is purely sinusoidal and in phase with the reference phase voltage.

Using the switch S_{1A} and diode D_{1A} duty-cycle expressions given in [19], the half-bridge inverter-side current local average value is expressed as

$$i_{inv,1/2}=\begin{cases}\left[\frac{-1}{2}+\frac{3}{2}m_a\sin(\varphi)\right]I_p\sin(\varphi) & ;\theta_M\le\varphi\le\pi-\theta_M\\ \left[\frac{1}{2}+\frac{3}{2}m_a\sin(\varphi)\right]I_p\sin(\varphi) & ;\pi\le\varphi\le\pi+\theta_M\\ \left[\frac{1}{2}+\frac{3}{2}m_a\sin(\varphi)\right]I_p\sin(\varphi) & ;2\pi-\theta_M\le\varphi\le2\pi\\ 0 & ;\text{otherwise}\end{cases}, \tag{3}$$

where

$$\theta_M=\sin^{-1}\left(\frac{1}{3m_a}\right), \tag{4}$$

I_p is the output peak phase current, $\varphi=\omega t$ is the converter ac phase angle and m_a is the modulation index.

The dc current value supplied by the rectifier is computed with

$$I_{dc,1/2}=\frac{1}{2\pi}\int_0^{2\pi} i_{inv,1/2}\,d\varphi=I_p\left(\frac{3m_a}{8}-\frac{1}{2\pi}\right). \tag{5}$$

The current through capacitor $C_{1/2}$ is found with

$$i_{c,1/2}=I_{dc,1/2}-i_{inv,1/2}, \tag{6}$$

which shows that only the ac components in $i_{inv,1/2}$ ideally circulate through $C_{1/2}$. The $i_{c,1/2}$ behavior for a fundamental output voltage period is exemplarily shown in Fig. 3 considering $m_a=0.9$ and $I_p=50\sqrt{2}$ A. The half-bridge inverter requires a pulsed current from the dc-link capacitor with a high crest factor, defined as the peak value over the rms value. The first harmonic of this current is in the same frequency of the output. Thus, large voltage ripple are expected if low capacitance values are employed.

The voltage across the dc-link capacitor is found with the solution of the differential equation

$$i_{c,1/2}(t)=C_{1/2}\frac{dv_{c,1/2}(t)}{dt}, \tag{7}$$

which is

$$v_{c,1/2}(t)=\frac{I_p}{8\pi\omega C_{1/2}}\{3\pi m_a[\sin(2\omega t)-\omega t]-4[\pi\cos(\omega t)+\omega t]+4\pi\}+V_{c,1/2}(0) \tag{8}$$

Finding $\frac{d}{dt}v_{c,1/2}(t)=0$ leads to the angles where the maxima and minima of the capacitor voltage occur. These angles, named here ωt_1 and ωt_2, are respectively

$$\omega t_1=\cos^{-1}\left\{\frac{1}{6}\sqrt{27+\frac{2}{m_a}\left[\frac{6}{\pi}-\frac{1}{m_a}-\sqrt{\frac{\pi(1+9m_a^2)-12m_a}{\pi m_a^2}}\right]}\right\} \tag{9}$$

and

$$\omega t_2=\pi-\omega t_1. \tag{10}$$

Replacing ωt_1 and ωt_2 into (8) gives the maximum and minimum voltage values

$$V_{c,1/2}^{\max}=\frac{1}{24\pi\omega C_{1/2}}\begin{Bmatrix}I_p\left\{\frac{\pi}{2}m_a\rho\sqrt{36-\rho^2}+12\pi-\right.\\ -\cos^{-1}\left(\frac{1}{6}\rho\right)(12+9\pi m_a)-\\ \left.-2\sqrt{\pi}\rho\right\}+24\pi\omega C_{1/2}V_{c1}(0)\end{Bmatrix} \tag{11}$$

and

$$V_{c,1/2}^{\min}=\frac{1}{24\pi\omega C_{1/2}}\begin{Bmatrix}I_p\left\{9m_a\pi\left[\cos^{-1}\left(\frac{1}{6}\rho\right)-\pi\right]+\right.\\ +2\sqrt{\pi}\rho+12\cos^{-1}\left(\frac{1}{6}\rho\right)-\\ \left.-\frac{\pi}{2}m_a\rho\sqrt{36-\rho^2}\right\}+\\ +24\pi\omega C_{1/2}V_{c1}(0)\end{Bmatrix}, \tag{12}$$

where the auxiliary variable ρ is written as

$$\rho=\sqrt{27+\frac{1}{m_a}\left(\frac{12}{\pi}-\frac{2}{m_a}-\sqrt{9-\frac{12}{\pi m_a}+\frac{1}{m_a^2}}\right)}. \tag{13}$$

The peak-to-peak voltage ripple value across the dc-link is given by

$$\Delta V_{c,1/2}=V_{c,1/2}^{\max}-V_{c,1/2}^{\min}. \tag{14}$$

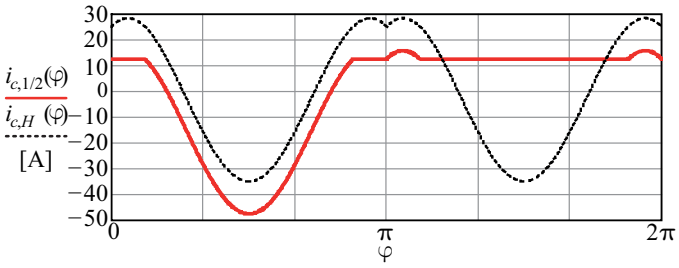

Fig. 3. : Current in the capacitors of half- (solid line) and H-bridge (dashed) modules for peak current $I_p=50\sqrt{2}A$ and modulation index $m_a=0.9$.

Replacing (11) and (12) into (14) and performing some mathematical manipulation, the expression that allows to design the capacitance for the half-bridge modules given a maximum dc-link voltage ripple is

$$C_{1/2}^{\min} = \frac{I_p}{24\pi\omega\Delta V_{c,1/2}} \left\{ \begin{array}{l} \pi m_a \rho \sqrt{36-\rho^2} + 9\pi^2 m_a - \\ -18\pi m_a \cos^{-1}\left(\frac{1}{6}\rho\right) - 4\pi\rho - \\ -24\cos^{-1}\left(\frac{1}{6}\rho\right) + 12\pi \end{array} \right\} \quad (15)$$

In most applications the capacitance value for a given voltage ripple is not enough to specify a capacitor. The rms current through the capacitor must be found to accomplish a complete specification. Considering that the rectifier-side current is constant, the dc-link capacitor rms current value $I_{c,1/2}^{\text{rms}}$ is found with

$$I_{c,1/2}^{\text{rms}} = \sqrt{{I_{inv,1/2}^{\text{rms}}}^2 - I_{dc,1/2}^2}, \quad (16)$$

where the inverter-side rms current value is given by

$$\begin{aligned} {I_{inv,1/2}^{\text{rms}}}^2 &= \frac{1}{2\pi}\int_0^{\pi} {i_{inv,1/2}}^2 d\varphi \\ &= \frac{1}{2\pi}\int_0^{\pi} \left[\tfrac{-1}{2} + \tfrac{3}{2} m_a \sin(\varphi)\right] \left[I_p \sin(\varphi)\right]^2 d\varphi, \end{aligned} \quad (17)$$

which finally results in the hybrid C1/2B dc-link inverter-side rms current value given by

$$I_{inv,1/2}^{\text{rms}} = \frac{\sqrt{2} I_p}{4}\sqrt{\frac{8m_a - \pi}{\pi}}. \quad (18)$$

Considering (5), (16) and (18) the capacitor rms current value considering only the low frequency harmonic components is

$$I_{c,1/2}^{\text{rms}} = \frac{I_p}{8\pi}\sqrt{-9\pi^2 m_a^2 + 88\pi m_a - 8\pi^2 - 16}. \quad (19)$$

B. Cascaded H-Bridge Modules

The same procedure that is used to specify the dc-link capacitors of a cascaded half-bridge module is applied to an H-bridge module. The assumptions made in the previous section are valid here. The first harmonic of the current fed to the inverter occurs at twice the inverter output fundamental frequency for the H-bridge modules. The local average value of this current is

$$i_{inv,H} = \left[\tfrac{-1}{2} + \tfrac{3}{2} m_a \sin(\varphi)\right] I_p \sin(\varphi); 0 \le \varphi \le \pi \quad (20)$$

and exemplarily shown in Fig. 3. Based on (20), the expressions of the capacitance C_H and rms current value $I_{c,H}^{\text{rms}}$ for the H-bridge dc-link capacitors are, respectively,

$$C_H = \frac{I_p}{12\omega\pi\Delta V_{c,H}} \left\{ \begin{array}{l} -2\sqrt{18\pi^2 + \frac{24\pi - 12\pi^2\rho_H}{m_a}} + 12\pi - \\ -24\arcsin(\rho_H) + 18\pi m_a \rho_x \sqrt{1-\rho_H^2} \end{array} \right\} \quad (21)$$

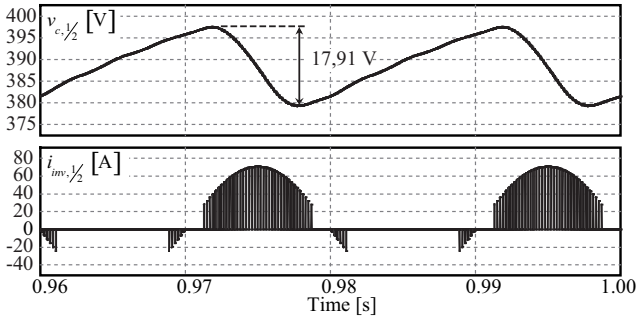

Fig. 4. : Voltage and current of half-bridge capacitors for $L_{in} = 5\%$, $m_a = 0.9$ and $\Delta V_{c1} = 4\%$.

and

$$I_{c,H}^{\text{rms}} = \frac{I_p}{4\pi}\sqrt{-9\pi^2 m_a^2 + 56\pi m_a - 4\pi^2 - 16}, \quad (22)$$

where

$$\rho_H = \frac{\pi + \sqrt{18\pi^2 m_a^2 - 24 m_a \pi + \pi^2}}{6\pi m_a}, \quad (23)$$

and $\Delta V_{c,H}$ is the maximum dc-link voltage ripple.

III. HYBRID CONVERTERS SIMULATION AND EXPERIMENTAL RESULTS

This section presents simulation results for both converters and compares them with the analytical expressions derived in the previous section in order to evaluate the validity of the adopted modeling procedure.

Both hybrid inverters were analyzed through numeric circuit simulations. The analyzed converters present the same operation parameters, namely: the output current peak is set at $I_p = 70$ A; dc-link voltage $V_{dc} = 400$ V; modulation frequency $f_o = 50$ Hz; switching frequency $f_s = 1.05$ Hz; and, null load displacement angle. The capacitor is set as function of modulation index and given maximum voltage ripple and the line inductances are constant. The multipulse rectifier parameters are presented in Table I.

TABLE I: Multipulse rectifier parameters for an exemplary desing.

m_a	$\Delta V_{c,1/2/H}$	$C_{1/2}$ [µF]	C_H [µF]	$L_{in,1/2}$ [mH]	$L_{in,H}$ [mH]
0.9	2% = 8 V	21,640	13,200		
0.9	4% = 16 V	10,820	6,600		
0.9	10% = 40 V	4,328	-		
0.7	2% = 8 V	13,700	9,000	1% = 0.562	1% = 0.281
0.7	4% = 16 V	6,851	4,500	2% = 1,124	2% = 0.562
0.7	10% = 40 V	2,741	-	5% = 2,808	5% = 1,404
0.5	2% = 8 V	5,980	-		
0.5	4% = 16 V	2,990	-		
0.5	10% = 40 V	1,196	-		

Fig. 6 shows the dc-link voltage and the inverter-side current for a half-bridge module included in a HC1/2B. The peak-to-peak ripple is approximately 17.91 V. The inverter-side current does not change much with the multipulse rectifier parameters. However, the rectifier-side current time behavior is strongly influenced by the employed inductances. The sensitivity of the dc-link capacitor rms current computed with (19) to different rectifier inductance values and dc-link voltage ripple is observed in Fig. 6, where higher errors are seen for low inductance values and higher dc-link voltage ripple. Fig. 6 shows the sensitivity of the peak-to-peak dc-link voltage ripple value to variations of modulation index and rectifier inductance. Lower errors are found for lower dc-link voltage ripple.

Experimental verification is carried out in a small scale IGBT based laboratory prototype of the HC1/2B. The prototype presents all dc sources with galvanic insulation through three-phase transformers, which are fed by the mains via three-phase variac in order to control of the input voltages. The input line reactive impedances have been added to give 5% per phase. Three-phase diode bridges rectify the voltages in the secondary side of the transformers and electrolytic capacitors smooth the rectified voltages in order to achieve low ripple dc voltages in all dc sources. The average voltage value for the dc-links is set to approximately 400 V. The capacitors are rated at 3,300 μF and 450 V. This capacitance is able to provide a peak-to-peak voltage ripple of approximately 2 V. The employed IGBTs are manufactured by Semikron in half-bridge modules (SKM75GB063D) rated for 600 V and 75 A. The switching frequency for the half-bridge converters is set to 1.02 kHz, while the output fundamental voltage is 60 Hz. The hardware is built to offer safe operation margins and flexibility and thus is not optimized for specific operation conditions. The employed RL load presents $R = 180\ \Omega$ and $L = 111$ mH

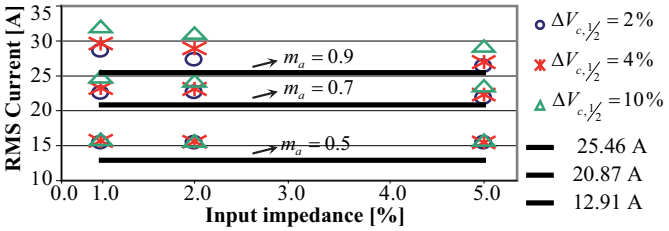

Fig. 5. : RMS half-bridge capacitor current as function of perceptual input line impedance and ripple voltage .

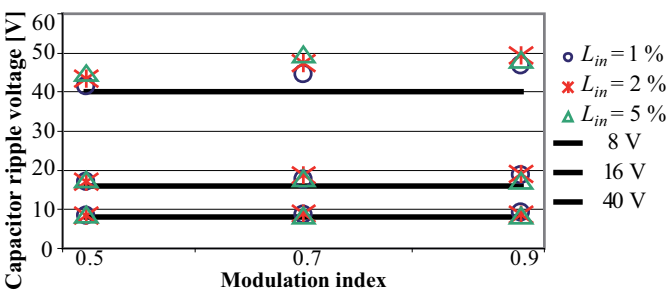

Fig. 6. : Ripple voltage of half-bridge capacitors as function of modulation index and input line impedance.

Y-connected, leading to a current displacement angle around 13° at 60 Hz.

The modulation patterns generation is performed in a DSP, model TI TMS320F2812, where the gate signals are generated in an open-loop scheme. The modulation employs the DSP's event manager (EVA and EVB) and a few I/O pins. The high frequency PWM pulses are produced by the DSP's PWM modules, while the low frequency signals are software generated by comparing the modulating signals to zero. The sinusoidal references are internally computed through a routine that cal-

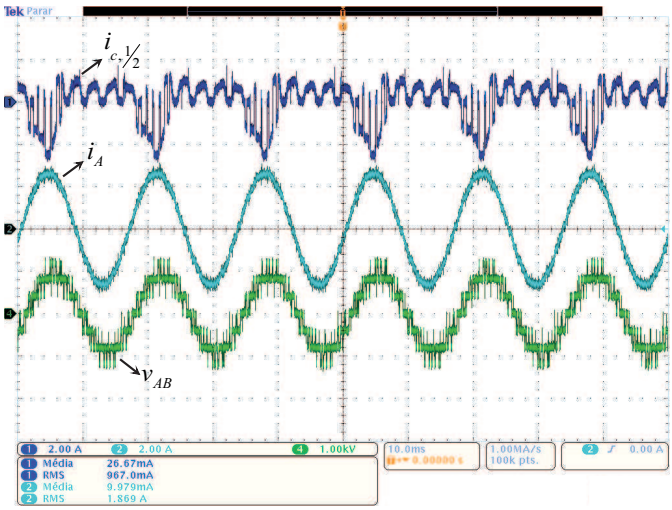

Fig. 7. : Experimentally obtained: Ch. 1 - capacitor current for a half-bridge converter, Ch. 2 - output line current and Ch. 4 output line voltage. The inverter is operating with the following parameters: $V_x = V_y = 400$ V; $m_a = 0.9$; $I_p = 3$ A; load is a Y-connected RL load with $R = 180\ \Omega$ and $L = 111$ mH.

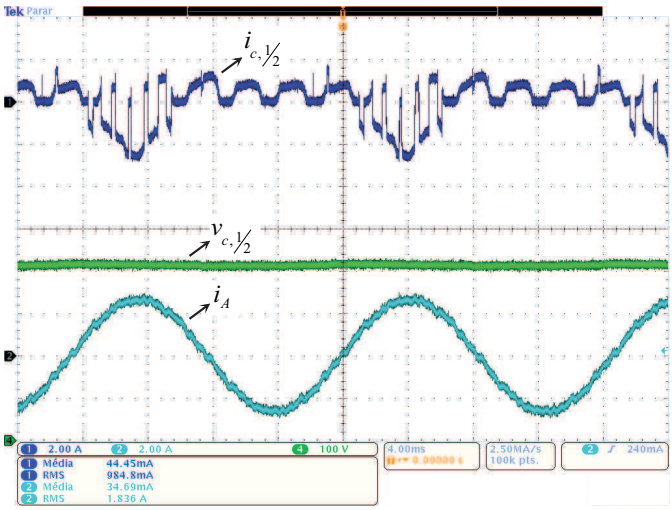

Fig. 8. : Experimentally obtained: Ch. 1 - capacitor current for a half-bridge converter, Ch. 2 - output line current and Ch. 4 capacitor voltage for a half-bridge converter. The inverter is operating with the following parameters: $V_x = V_y = 400$ V; $m_a = 0.9$; $I_p = 3$ A; load is a Y-connected RL load with $R = 180\ \Omega$ and $L = 111$ mH.

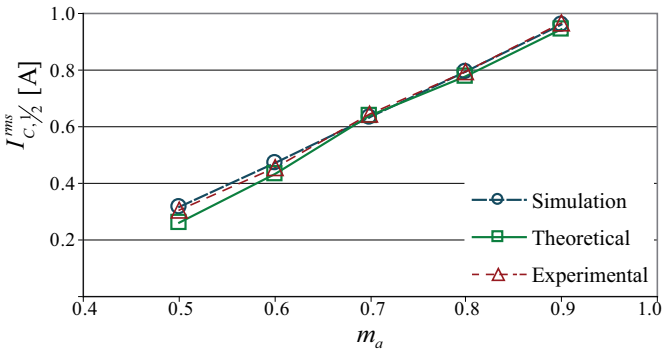

Fig. 9. : Rms current value at the half-bridge dc-link capacitors for $L_{in} = 5\%$, $m_a = 0.9$, $C_{1/2} = 3,300$ μF, $R = 180$ Ω and $L = 111$ mH Y-connected.

culates 60 Hz sinusoidal signals displaced by 120°. A zero crossing detector is virtually implemented in order to compare the polarity of the sinusoidal references. Depending on the instantaneous value of the modulating function an algorithm adapts the function levels to the DSP's PWM modulator.

Experimentally obtained results of the inverter presented in Fig. 1(a) are shown in Fig. 7 and Fig. 8. Fig. 7 presents the half-bridge capacitor current, the output phase current and the output line voltage. These waveforms present the predicted time behavior, including the capacitor current, which has a low frequency component originated from the input rectifier. Fig. 8 shows the half-bridge capacitor current, the output phase current and the half-bridge capacitor voltage. The voltage ripple presented in the capacitor voltage is low as designed.

Computer simulations have been done in order to compare the experimental results with the theoretical and simulation ones some. The same parameters as the experimental prototype are used in the simulations. The results are compared in Fig. 9. The half-bridge modules dc-link capacitor current rms value presents very close results to the analytical calculations, numerical simulations and the experimental results, specially at high modulation indexes. These results validate the proposed method to calculated the rms current in the capacitors of the half-bridge converters and agree with the previous analysis, where low dc-link voltage ripple conditions lead to more precise theoretical results.

IV. HYBRID CONVERTERS COMPARISON

This section presents comparison results based on similar modulation strategies applied to both converters. Considering that two half-bridge modules are able to ideally present the same voltage generation capability of an H-bridge one, the voltage and current waveforms in both converter modules are similar. This leads to the comparison results shown in Table II Both converters require the same amount of semiconductors and all semiconductors find their equivalent parts in each of the converters. This implies in that the voltage and current efforts in the power semiconductors for the topologies are the same. The number of voltage levels is also similar. Therefore, the hybrid multilevel inverters are able to generate the same output voltage vectors and, for a given modulation strategy, the same voltage THD. The differences apparently start

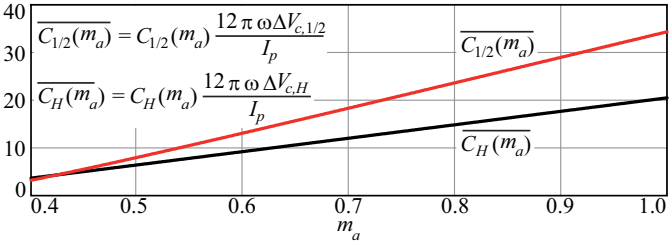

Fig. 10. : Total required capacitance for half- and full-bridge modules parametrized as functions of I_p, $\Delta V_{c,j}$ and ω.

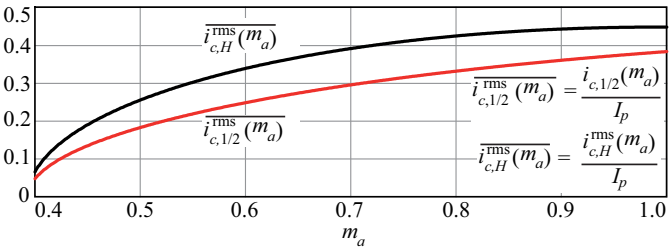

Fig. 11. : RMS current in the capacitors of half- and full-bridge converters parametrized as function of I_p.

with the isolated dc sources, which are twice the number in the half-bridges based converter. However, the active power processed in each of the half-bridge modules dc sources is half of the power in an H-bridge. Thus, regarding average current values, both topologies lead to the same required multipulse rectifier diodes silicon area. In summary, the multipulse rectifier diodes, transformers and inductors will be very similar, even of the number of diodes and transformer secondaries are different.

It appears that the main difference between the hybrid inverters is their single-phase modules dc-link capacitors. A comparison based on section II is presented in the following. Fig. 10 shows the required dc-link capacitance for both topologies as a function of the modulation index in order to limit a given voltage ripple. It is clear the the H-bridge modules need lower capacitance values with increasing modulation index. For instance, the total required capacitance for a half-bridge module (here understood as two cascaded half-bridge conver-

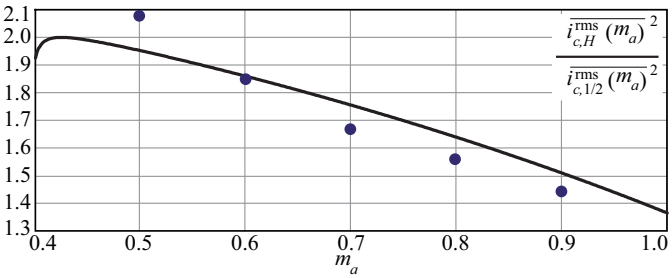

Fig. 12. : Quadratic rms current values at the dc-link capacitors of a half-bridge module divided by the quadratic rms current value at the capacitors of an H-bridge converter. This ratio is proportional to the ratio of the dc-link capacitors losses.

TABLE II: Comparison between 3-phase VSI cascaded with half-bridge converters and 3-phase VSI cascaded with full-bridge converters.

Parameters	**3-phase VSI cascaded with half-bridge converters**	**3-phase VSI cascaded with full-bridge converters**
Number of controlled semiconductors (switches)	6 per phase	6 per phase
Number of controlled semiconductors (diodes)	6 per phase	6 per phase
Number of isolated dc sources (except 3-phase VSI)	6	3
Power processed for each isolated dc source $m_a = 0.9$ (except 3-phase VSI)	8.80 % of total processed power	17.60 % of total processed power
Number of electrolytic capacitors (except 3-phase VSI)	6	3
Number of levels at the phase voltage	4, 5 or 6	4, 5 or 6
Number of levels at line voltage	7, 9 or 11	7, 9 or 11
THD at phase / line output voltage $m_a = 0.9$	17 % / 22 %	17 % / 22 %
Allow to employ low switching frequency at VSI	Yes	Yes
Current and voltage efforts in the power semiconductors	Same	Same
Losses at the power semiconductors	Same	Same

ters) is approximately three times larger than for an H-bridge one at $m_a = 0.8$. This means that a half-bridge based module requires three times the capacitance of an H-bridge one.

The dc-link capacitors rms current values in an H-bridge module are higher than in a half-bridge. This is seen in Fig. 11. However, a direct comparison of the currents does not completely clarify the issue, since the physical quantity that limits capacitor utilization is the power loss in a component as given in (1) and that is proportional to the square of the current rms values. Therefore, it is sensible to compare the relation between ${I_{c,1/2}^{\text{rms}}}^2$ and ${I_{c,H}^{\text{rms}}}^2$ as shown in Fig. 12. The loss relation is much favorable to the half-bridge converter, reaching an advantage of $3/2$ for $m_a = 0.9$. Therefore, considering similarly built capacitors, an H-bridge module requires 1.5 times more capacitors for $m_a = 0.9$. Nevertheless, the total number of capacitor for the HC$^1/_2$B converter is twice the number in a HCHB one.

V. CONCLUSIONS

The 3-phase 2-level VSI cascaded with H-bridge modules (HCHB) and the 3-phase 2-level VSI cascaded with half-bridge modules (HC$^1/_2$B) hybrid multilevel converters have been compared. The two inverters present similar performance in aspects such as: number of semiconductors, efforts on semiconductors, output voltage THD and input rectifier. The HC$^1/_2$B employs twice the number of isolated dc sources. However, it was shown that both topologies lead to the same required silicon area for a multipulse recitifier. Thus, the dc-link capacitors of their single-phase modules are the main point for discussion. A design procedure of these capacitors considering the dc-link voltage ripple and the capacitors rms current was proposed. The rms current in the dc-link capacitors is the most relevant parameter. It was shown that the H-bridge requires from 1.5 to 2 times more capacitors than the half-bridge converter depending on the modulation index m_a. Considering that a half-bridge module uses two capacitors, the advantage is with the H-bridge converter with a margin that depends on m_a.

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