A DUAL UNIFIED POWER QUALITY CONDITIONER USING A SIMPLIFIED CONTROL TECHNIQUE

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***Abstract* – This paper presents a dual three-phase topology of unified power quality conditioner (UPQC) composed of two filters, a series active filter and a parallel active filter, aimed to compensate both, the current and voltage, harmonics and unbalance. Different from conventional UPQC, the dual UPQC has the series filter controlled as a sinusoidal current source and the parallel filter controlled as a sinusoidal voltage source. Therefore, the PWM controls of the dual UPQC deal with a well known frequency spectrum, since it is controlled using voltage and current sinusoidal references, differently from the conventional UPQC which is controlled using nonsinusoidal references. In this paper it is presented the analog control project and some experimental results of the developed prototype.**

***Keywords* - Active Filters, Analog Controller, Power Quality, Sinusoidal References, Unified Conditioner.**

I. INTRODUCTION

The usage of power quality conditioner in the distribution system network has increased during the past years due to the steady increase of nonlinear loads connected to the electrical grid. Because it drains current with high harmonic content, the nonlinear loads distorts the voltage sourced by the utility grid, it directly affects the behavior of other more sensitive loads to this kind of distortion.

By using power quality conditioner it is possible to guarantee sinusoidal, with low harmonic distortion, balanced and regulated voltages to the load and at the same time to drain from the utility grid undistorted currents, even if the grid voltage and the load current have harmonic contents.

The unified power quality conditioners present a topology consisted by two different filters, the series active filter and the parallel active filter. The parallel active filter is usually current controlled, which is responsible for compensating the harmonic current of the load, while the series active filter is voltage controlled, which is responsible for compensating the grid voltage distortion [1-5]. In this case, the voltage and the current the filters must compensate have harmonic contents whose reference must also have harmonic contents, and these references are obtained through complex methods.

Dias [6] presented a control technique with sinusoidal references in order to find a solution for the complexity that is the reference generation for these conditioners. The reference generation works well but the leakage impedance of the connection transformer interferes in the voltage compensation generated by the series filter, since it is applied to the distribution system network.

The article presented by Moran [7] in 1989, shows a dual single-phase CSI line voltage conditioner where series active filter is current controlled and the parallel active filter is voltage controlled. In this way, the signals to be controlled are sinusoidal and therefore the references are also sinusoidal. Some authors have applied this idea in Uninterruptable Power Supplies (UPS) [8-9], while others in Unified Power Quality Conditioners (UPQC) [10], the latter is highlighted by the work of Aredes [11], who presents a three-phase unified power quality conditioner designated by him iUPQC. The advantage of the iUPQC is that it works only with sinusoidal references, although the control used uses the p-q theory which makes the unified power quality conditioner control complex, because it is necessary to determine in real time the positive sequence components of the voltages and of the currents.

The aim of this paper is to present a dual three-phase unified power quality conditioner to be used in the distribution system network using a simplified PWM analog control; it will also present the control project, the power flow in the structure, the pre-charge sequence used and the experimental results obtained with a prototype.

II. PROPOSAL FOR A UNIFIED POWER QUALITY CONDITIONER

The conventional UPQC structure is composed by a series active filter and by a parallel active filter, as shown in Fig. 1. In this configuration the series active filter is voltage controlled in order to compensate the grid distortion, allowing the load voltage to be consisted only by the fundamental content. This way, the voltage compensated by the series active filter is composed by a fundamental content in order to compensate the sags/swells and the voltage unbalance, and by the harmonics, the same harmonics which are intended to compensate from the grid voltage, 180° phase shifted.

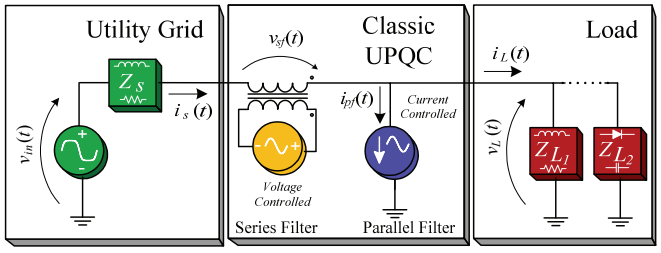

Fig. 1. Conventional Unified Power Quality Conditioner (UPQC).

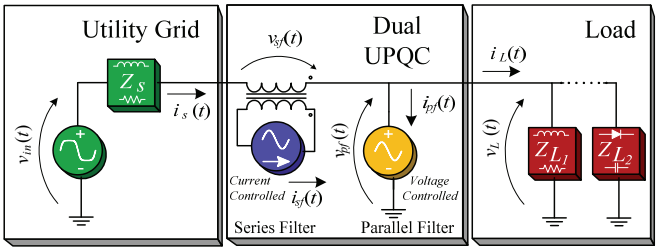

Fig. 2. Dual Unified Power Quality Conditioner (UPQC).

The parallel filter is current controlled and it is responsible for draining the load current complementary harmonic contents, allowing a sinusoidal grid current. The parallel filter may still drain a fundamental content in order to compensate the load displacement power factor.

The series filter connection to the utility grid is made through a transformer, while the parallel filter is most of the time connected directly to the load connection, in low voltage grid applications.

The disadvantages of this unified power quality conditioner are the following:

- Complex voltage and current control reference generation;
- Voltage and current references with harmonic contents;
- The leakage impedance of the connection transformer interferes in the voltage compensation generated by the series filter.

In order to find a solution to these disadvantages the dual UPQC is presented in this paper and shown in Fig. 2. It is possible to see that the structures that form this unified power quality conditioner are similar to the conventional UPQC, diverging only from the way the series and parallel filters are controlled.

In this dual topology the series active filter is current controlled behaving as a current source which imposes a sinusoidal input current synchronized with the grid voltage. The parallel active filter behaves as a voltage source since it is voltage controlled, imposing sinusoidal load voltage synchronized with the grid voltage.

In this way, the UPQC control uses sinusoidal references for both active filters. This is a major point to observe against the classic topology since the only request of reference generation is that it must be synchronized with the grid voltage.

The series active filter acts as a high impedance for the current harmonics. This filter indirectly compensates the load voltage since the connection transformer voltage equals the difference between the grid voltage and load voltage. Therefore, all unbalance, sags/swells and harmonic voltages are on the connection transformer. The voltage controlled parallel filter indirectly compensates the grid current, providing low impedance for harmonic load current.

The guarantee of the power factor compensation of the structure is due to the imposed sinusoidal current synchronized with the grid voltage, allowing the parallel filter to supply the reactive power to the load, regulating the load voltage as well. The active filters that form the structure of the dual UPQC consist by four wire three-phase inverters and it has a center tapped DC link shared by the two inverters, as shown in Fig. 3. Both inverters have high frequency filters on the output, although only the series filter uses connection transformers. Table I shows the power and control specifications of the dual UPQC.

III. CONTROL

The dual UPQC control structure consists in the association of the parallel and series active filter control. The series active filter consists in a current control loop in order to guarantee a sinusoidal grid current and synchronized with the grid voltage. The parallel filter has a voltage control loop in order to allow a balanced, regulated, synchronized, with low harmonic distortion voltage to the load. These control loops are independent one from the other since they act independently in each active filter. The DC link voltage control is made by the current controlled active filter because of the cascade control characteristics, where the voltage loop gives the reference to the current loop, which works with higher frequencies.

This way, the series active filter control strategy uses an input current and a DC link voltage feedback, while the parallel active filter control uses the load voltage feedback.

The control sinusoidal references are generated by a digital signal processor, DSP, which guarantees the grid voltage synchronism through the PLL circuit.

A. Series Active Filter Control

The series active filter controller consist of three identical current feedback loops, one for each phase, in order to control the input current, one voltage feedback loop to control the DC link voltage and another one unbalanced-voltage feedback loop to keep the voltage on the DC link capacitors balanced.

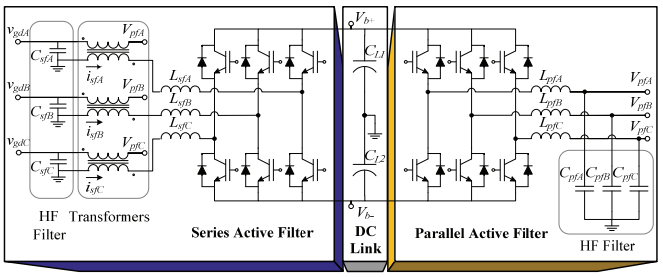

Fig. 3. Power circuit of the dual UPQC.

TABLE I
Power and control specifications of the dual UPQC

Input Nominal Phase-to-Neutral Voltage	$V_{in} = 127V_{RMS}$
Output Nominal Power	$P = 2500VA$
Series Filter Inductance	$L_{sf} = 650\mu H$
Parallel Filter Inductance	$L_{pf} = 650\mu H$
DC Link Voltage	$V_b = 400V$
DC Link Capacitance	$C_b = 3mF$
High Frequency filter Capacitance of the series active filter	$C_{sf} = 1\mu F$
High Frequency filter Capacitance of the Parallel Active Filter	$C_{pf} = 10\mu F$
Switching Frequency of the Series Active Filter	$f_{sf} = 20kHz$
Switching Frequency of the parallel Active Filter	$f_{pf} = 20kHz$
Transformer Ratio	$n = 1$

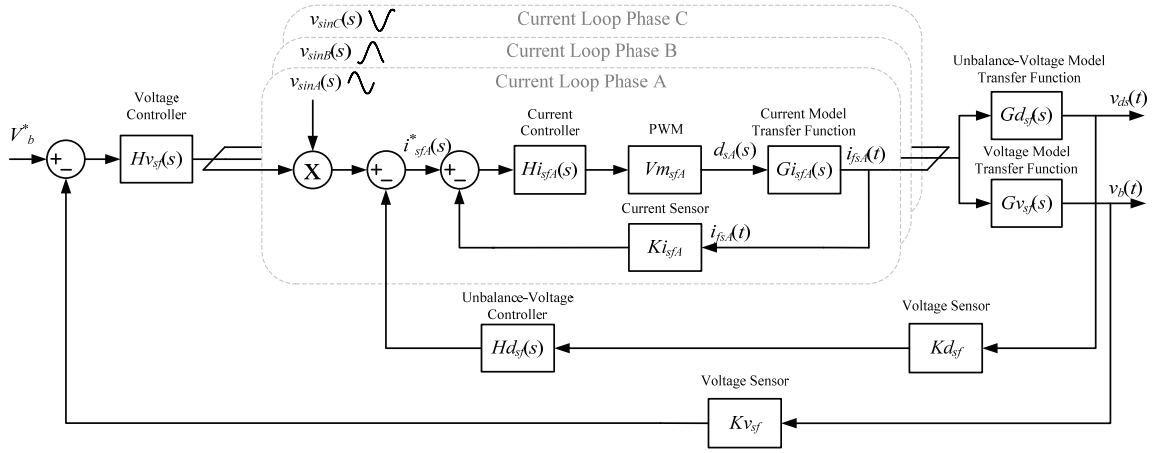

Fig. 4. Control block diagram of the series active filter controller.

The voltage control loop has a low response and determines the reference signal amplitude of current controller. In this way the higher the load power the higher will be the DC Link consumption resulting in higher input current amplitudes. The unbalanced-voltage control loop, is a DC level loop, acts on the average reference value of the current controller, in order to keep the DC link voltage balanced. The current control consists of three identical current loops, except for the 120 degrees phase shit from each other. The current loops have a fast response, allowing the decoupling of this with the voltage loop. The Fig. 4 shows the control block diagram of the series active filter controller.

The current, voltage and unbalance-voltage control chosen were PI controls with an additional pole, whose cutoff frequencies are 5kHz, 4Hz and 0.5Hz, respectively. All controls have phase margin between 30º e 90º. In order to obtain a better phase margin and bigger high frequency attenuation, this kind of controller was used duo to the models characteristics which have a pole in the origin.

The current loop transfer function is given by

$$Gi_{sf}(s) = \frac{V_b}{L_{sf} \cdot s} \cdot \frac{Hi_{sf} \cdot Ki_{sf}}{Vm_{sf}} \tag{1}$$

The voltage loop transfer function is given by

$$Gv_{sf}(s) = \frac{3}{2} \cdot \frac{m_a}{C_b \cdot s} \cdot \frac{Hv_{sf} \cdot Kv_{sf} \cdot K_m}{Hi_{sf}} \tag{2}$$

The unbalance-voltage transfer function is given by

$$Gd_{sf}(s) = \frac{3}{2 \cdot C_b \cdot s} \cdot \frac{Hd_{sf} \cdot Kd_{sf}}{Hi_{sf}} \tag{3}$$

Where:

C_b - DC Link Capacitance;
Hd_{sf} - Unbalance-Voltage Sensor Gain;
Hi_{sf} - Current Sensor Gain;
Hv_{sf} - Voltage Sensor Gain;
Kd_{sf} - Unbalance-Voltage Control Attenuation;
Ki_{sf} - Current Control Attenuation;
Kv_{sf} - Voltage Control Attenuation;
K_m - Multiplier Gain;
L_{sf} - Series Filter Inductance;
m_a - Modulation Ratio;
V_b - DC Link Voltage;
Vm_{sf} - Pulse Width Modulator Gain.

The K_m gain is obtained considering the gain of the multiplier integrated circuit used and the sinusoidal signal peak value to be multiplied. The modulation ratio m_a is the relation between the output peak voltage of the series active filter and the DC link voltage. The Vm_{sf} modulator gain equals the inverse peak value of the triangular carrier.

The proposed controller transfer function is given by

$$C_{sf} = \frac{R_1 \cdot C_2 \cdot s + 1}{R_2 \cdot s \cdot (C_1 + C_2) \cdot \left(\frac{R_1 \cdot C_2 \cdot C_1}{C_1 + C_2} \cdot s + 1 \right)} \tag{4}$$

Each controller has a distinct gain, poles and zeros. The current loop frequency response is shown in Fig. 5, while the voltage and unbalance-voltage loops frequency response are shown in Fig. 6 and Fig. 7, respectively. The proposed PI controller with an additional pole is shown in Fig. 8.

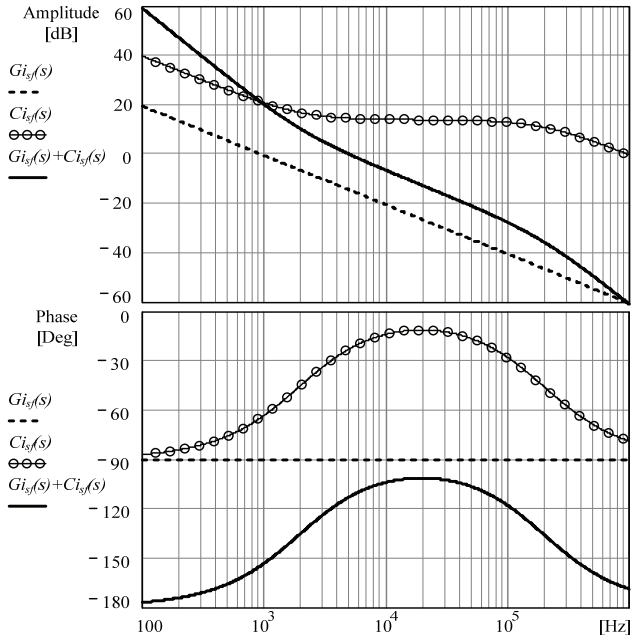

Fig. 5. Current loop frequency response of the series active filter.

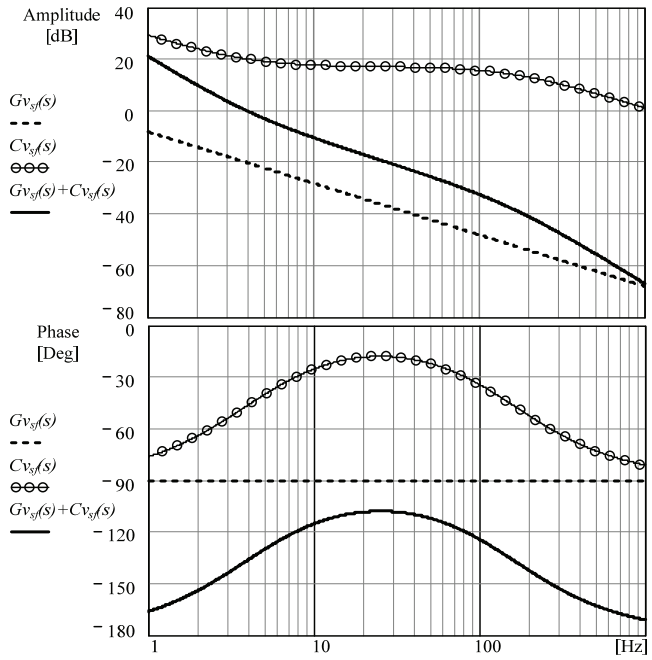

Fig. 6. Voltage loop frequency response of the series active filter.

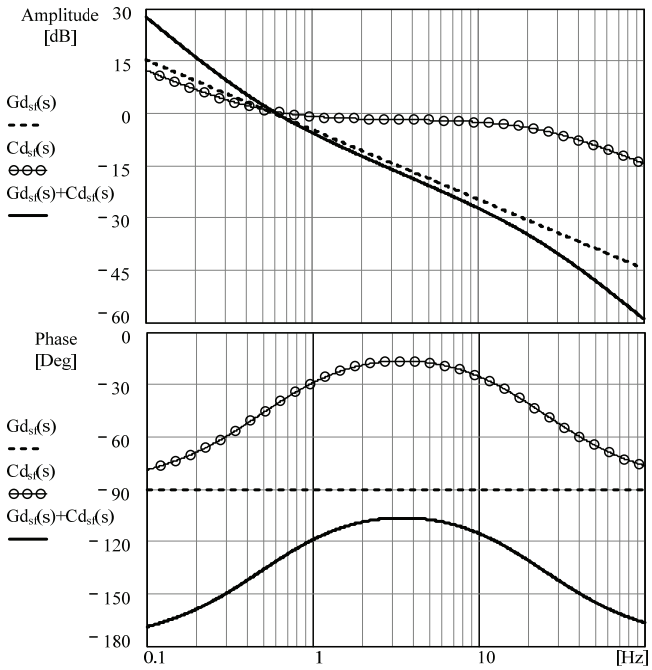

Fig. 7. Unbalance-Voltage loop frequency response of the series active filter.

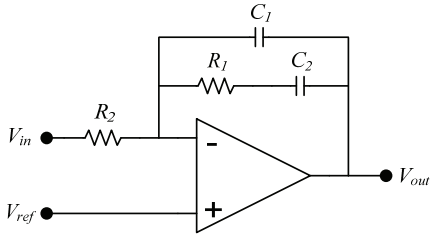

Fig. 8. Controller of the series active filter.

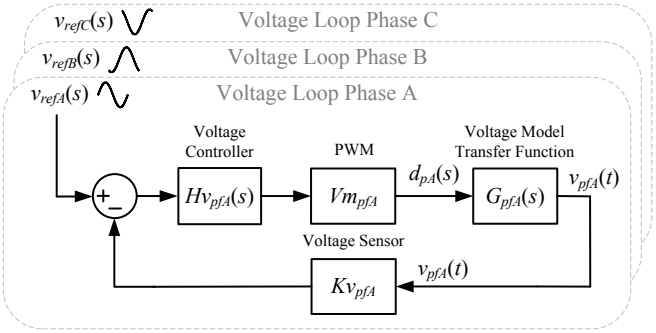

Fig. 9. Control block diagram of the parallel active filter controller.

B. Parallel Active Filter Control

The parallel active filter controller is composed by three identical voltage feedback loops, one for each phase, acting on the error signal generated by comparing the load voltage signal and a sinusoidal reference. The Fig. 9 shows the control block diagram of the parallel active filter controller.

Duo to the circuit model characteristics which has no poles in the origin and crosses the 0dB with a higher inclination angle than 20dB/dec, the voltage control chosen for the parallel active filter was a PID control with an additional pole. The cutoff frequency is 5kHz and the phase margin is equal to 34º.

The voltage loop transfer function is given by

$$G_{pf}(s) = \frac{Hv_{pf}Kv_{pf}}{Vm_{pf}} \cdot \frac{\dfrac{V_o}{L_{pf}C_{pf}}}{s^2 + s\left(\dfrac{1}{C_{pf}R_L}\right) + \dfrac{1}{L_{pf}C_{pf}}} \quad (5)$$

Where:

C_{pf} - Output Capacitance of the parallel filter;
Hv_{pf} - Voltage Sensor Gain;
Kv_{pf} - Voltage Control Attenuation;
L_{pf} - Parallel Filter Inductance;
V_o - Output Voltage;
Vm_{pf} - Pulse Width Modulator Gain;
R_L - Load Resistance.

The proposed PID controller with an additional pole is shown in Fig. 10 and its transfer function is given by

$$C_{pf} = \frac{R_1}{R_3} \cdot \frac{\left(s + \dfrac{1}{C_1R_1}\right) \cdot \left(s + \dfrac{1}{C_2R_2}\right)}{s \cdot \left(s + \dfrac{R_2 + R_3}{C_2R_2R_3}\right)} \quad (6)$$

The voltage loop frequency response is shown in Fig. 11.

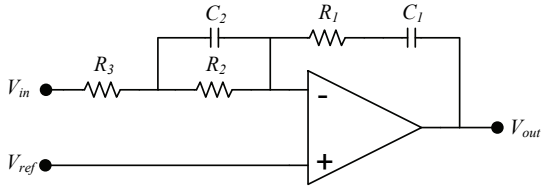

Fig. 10. Voltage controller for the active parallel filter.

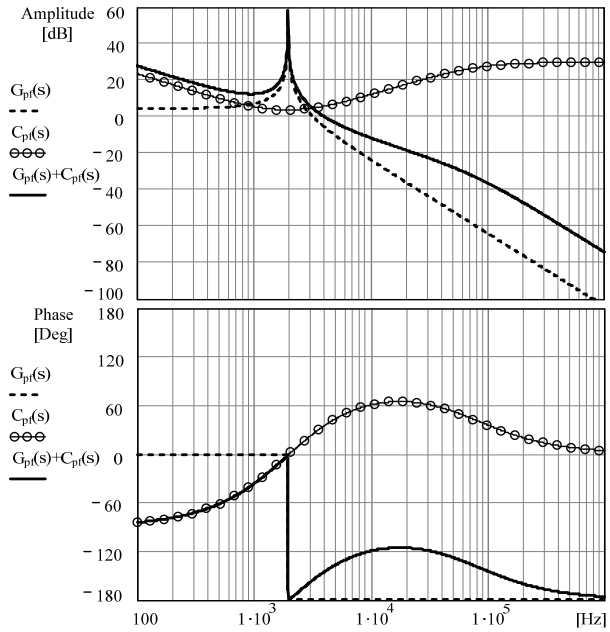

Fig. 11. Voltage loop frequency response of the parallel active filter.

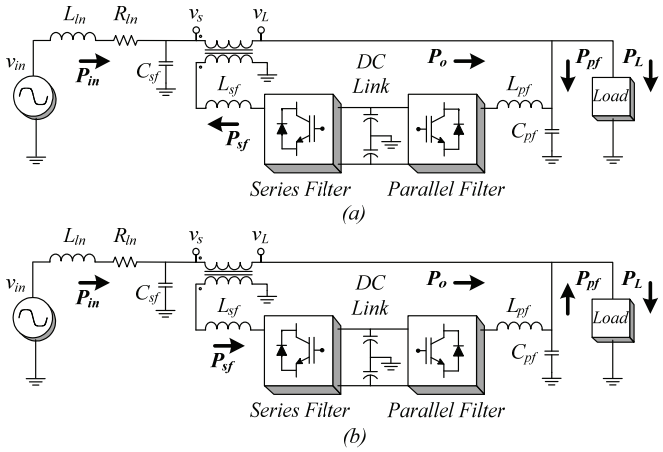

Fig. 12. Power flow of dual UPQC.

IV. POWER FLOW

The active power flow of the dual unified power quality conditioner is shown in Fig. 12. In Fig. 12(a) the supply voltage v_s has a lower amplitude than the load voltage v_L. In this case, the series active filter supplies active power to the load while the parallel active filter consumes active power. In Fig. 12(b) the supply voltage v_s has a higher amplitude than the load voltage v_L. In this case, the series active filter consumes active power while the parallel active filter supplies active power to the load.

The power drained from the electrical grid equals the sum of the load power and the dual UPQC power losses.

V. PRE-CHARGE SEQUENCE

The pre-charge of the dual UPQC must happen without changing the load voltage. In this way, the used pre-charge sequence is shown in Fig. 13.

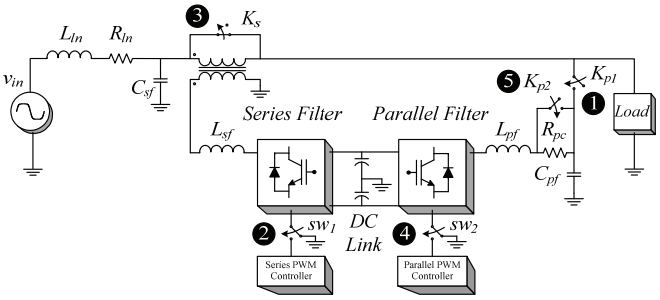

Fig. 13. Pre-charge sequence of dual UPQC.

The pre-charge circuit has three contactors, K_s, K_{p1} and K_{p2}, and one In-Rush resistor, R_{pc}, to limit the initial current. The switches s_{w1} and s_{w2} are used symbolically to show the switching turning on time.

The K_{p1} and K_{p2} contactors are initially opened, while the K_s contactor is initially closed and the switching of both active filters is initially disable. The pre-charge sequence starts when the contactor K_{p1} closes, providing the charge of DC link capacitors through diodes present in the parallel active filter structure. After 340ms, the switching of the series active filter is enabled, raising the DC link voltage and, after 1s, the K_s contactor is opened. After 10ms the switching of the parallel active filter is enabled, regulating the load voltage. After 100ms the K_{p2} is closed, finishing the pre-charge sequence. Fig. 14 presents the DC link voltage and the load voltage during the pre-charge sequence of the dual UPQC.

VI. EXPERIMENTAL RESULTS

A 2500W prototype was built in order to prove the dual UPQC would succeed. The prototype is made by two Semikron B6U+B6I+E1IF three-phase inverter modules in addition to the passive filters made by capacitors and inductors, according to Table I project specifications, and the structures show in Fig. 3. Each module is made by three SK 45 GB 063 semiconductors and three SKHI 20op drivers. The prototype is shown in Fig. 15.

In order to emulate a harmonic distorted current we used a three-phase rectifier with capacitive filter as load, a single-phase rectifier with RL load connected to the phase A and another connected to the phase B, all rectifiers being uncontrolled. The power drained by the load equals 1700W due to the current limit of the transformers used in the dual UPQC connection.

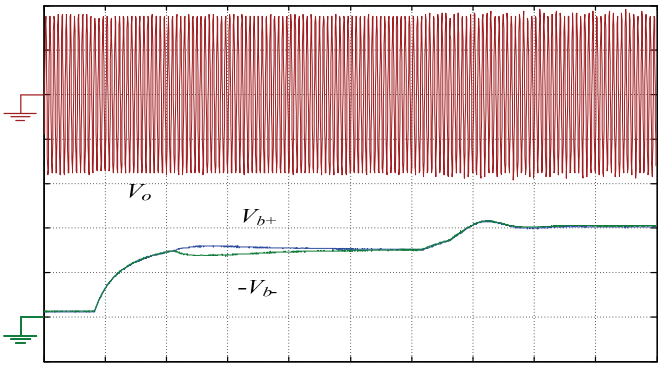

Fig. 14. Link DC voltages (50V/div, 250ms/div) and output voltage (100V/div, 250ms/div) during pre-charge.

In order to emulate a distorted grid voltage and evaluate the voltage distortion compensation, we used the UPQC supplied by a power source able to provide voltage harmonics. The power source represented a distorted source with 20% of third harmonic in phase A, 10% of fifth harmonic in phase B, and 10% of seventh harmonic in phase C.

Fig. 16 shows the source voltage, the load voltage, the source drained current, and the load current for the three phases. It is possible to see that the source drained currents are sinusoidal, balanced and synchronized with the source voltage, allowing power factor be equal to 0.980, 0.994 and 0.994 for phases A, B, C respectively. The THDs of the load currents equal 32.1%, 3.21% and 65.1%, while the source drain currents have THDs equal to 1.06%, 1.80% and 1.34%.

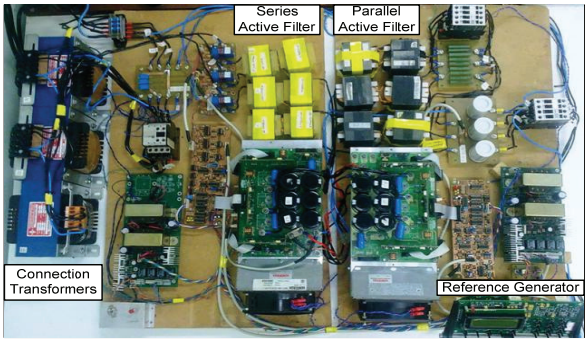

Fig. 15. The dual UPQC prototype.

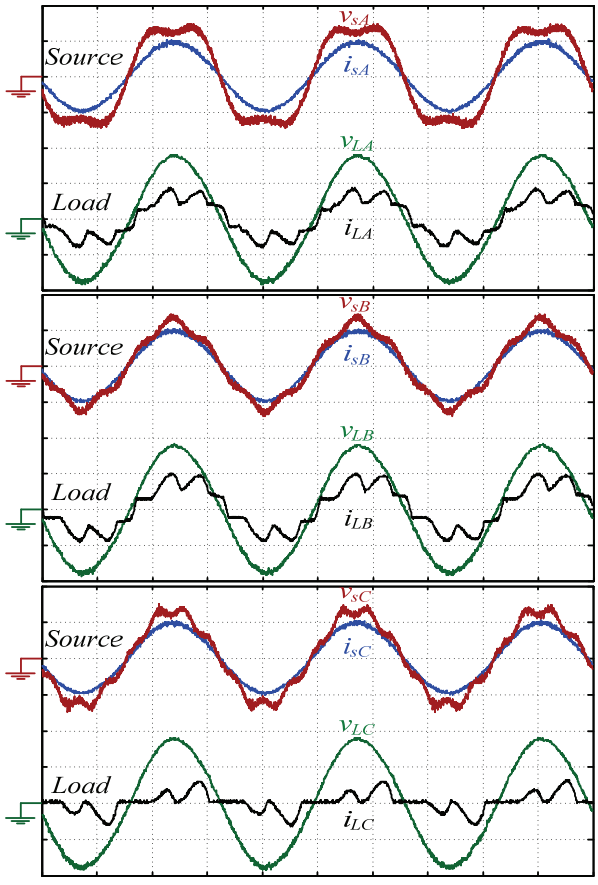

Fig. 16. Source and load voltages (100V/div, 5ms/div), source and load currents (10A/div, 5ms/div).

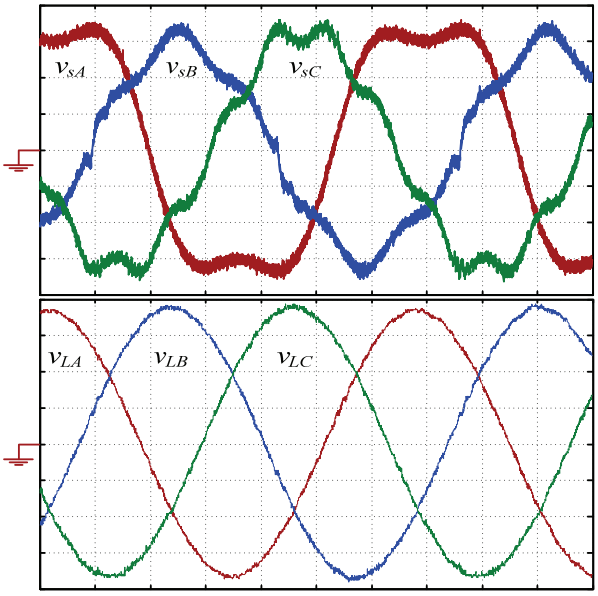

Fig. 17. Source voltages (40V/div, 2.5ms/div) and load voltages (48V/div, 2.5ms/div).

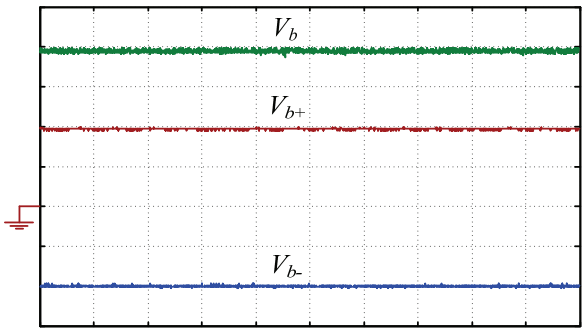

Fig. 18. DC link voltages (100V/div, 2.5ms/div).

Fig. 17 shows the source distorted voltage as well as the load voltage already compensated. The THDs of the source voltage equal 20.0%, 10.8% and 10.4% for phases A, B and C, respectively, while the load voltages have THDs equal to 0.53%, 0.69% and 0.38%.

Fig. 18 shows the DC link voltages whose voltages are controlled in 200V and -200V for each of the capacitor banks.

The following figures show the dynamic response of the dual UPQC. Fig. 19 shows the source voltages and the load voltages during a voltage dip in phase A. Fig. 20 shows the source voltage and the load voltage during a voltage swell. During the voltage swell the source voltage amplitude increases 20% and the dual UPQC guarantees the right voltage to the load.

The load voltage and the load current are shown in Fig. 21 during a load step from 50% to 100%. Fig. 22 shows the load voltage and the load current during a load step from 100% to 50%. Fig. 23 shows the DC link voltages and the load current in phase A during a load step.

Fig. 24 shows the source currents during a fault in phase A. It is possible to see that the source current in other phases have the amplitudes increased in order to keep the right voltages to the load.

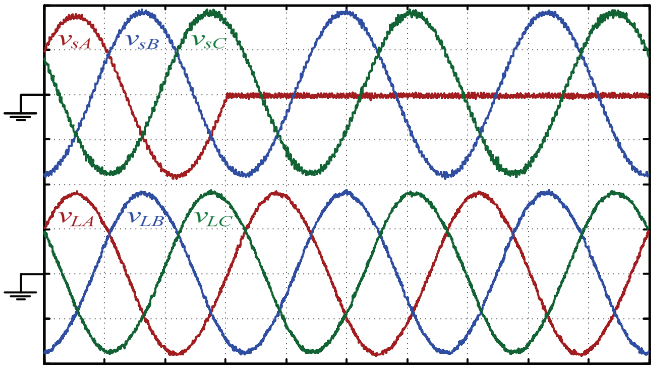

Fig. 19. Source voltages and load voltages (100V/div, 5ms/div) during a voltage dip in phase A.

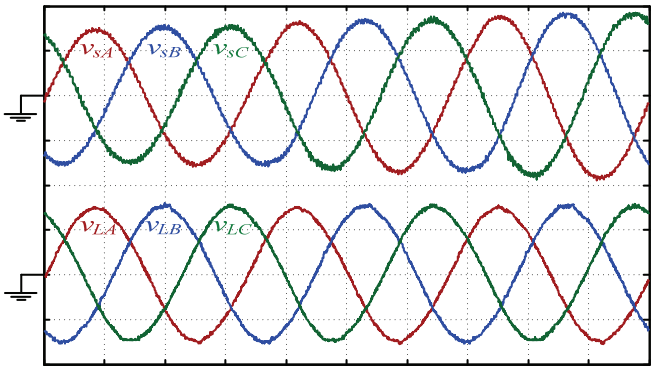

Fig. 20. Source voltages and load voltages (100V/div, 5ms/div) during a voltage swell.

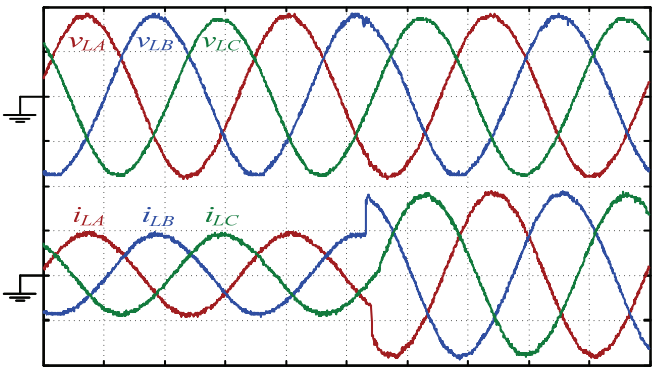

Fig. 21. Load voltages (100V/div, 5ms/div) and load currents (5A/div, 5ms/div) during a load step from 50% to 100%.

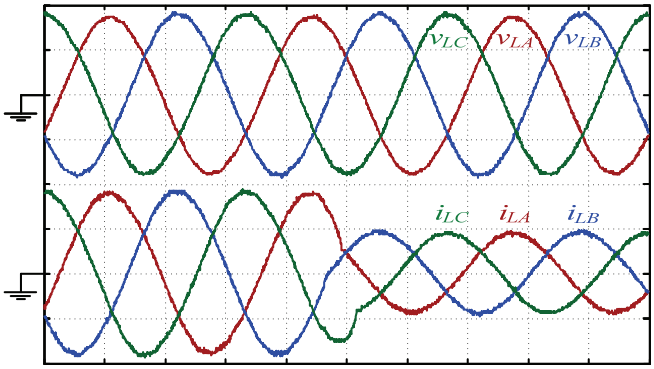

Fig. 22. Load voltages (100V/div, 5ms/div) and load currents (5A/div, 5ms/div) during a load step from 100% to 50%.

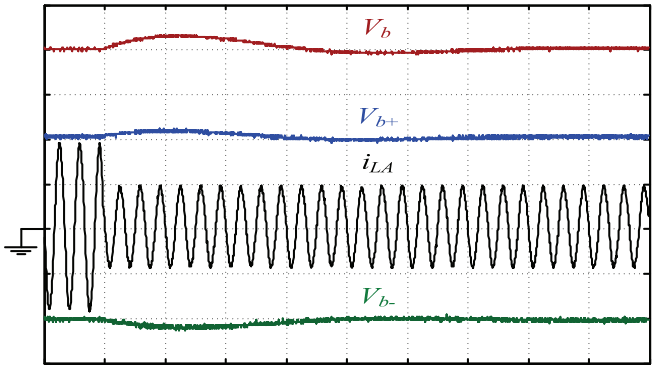

Fig. 23. DC link voltages (100V/div, 50ms/div) and load current (5A/div, 50ms/div) during a load step from 100% to 50%.

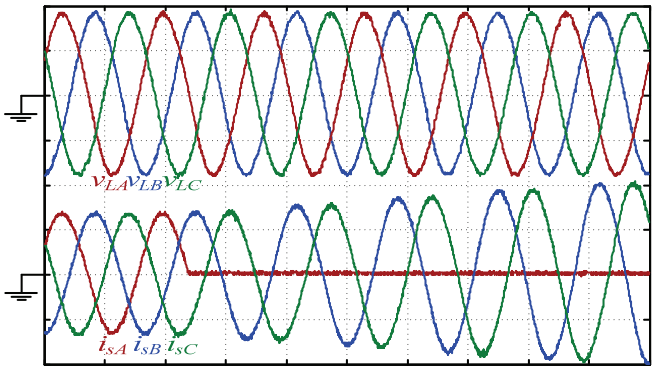

Fig. 24. Load voltages (100V/div, 10ms/div) and source currents (5A/div, 10ms/div).

VII. CONCLUSION

The results obtained with the dual UPQC showed that it is able to compensate the nonlinear load currents and also guarantee the sinusoidal voltage for the load in all the three phases.

The main advantage of the dual UPQC against the conventional structure is the utilization of sinusoidal references for both series and parallel active filter controls. The dual UPQC references do not have harmonic contents, the only requirement is the synchronism with the grid voltage. Another positive aspect of the dual UPQC in low voltage applications (distribution system network) is the non interference of the leakage impedance voltage of the series active filter connection transformer in the load voltage compensation.

The results validate the dual UPQC structure and its control techniques, proving that the power quality can be meaningfully better with a simple control method which uses only sinusoidal references.

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