NEW ZVS PWM STEP-UP/STEP-DOWN DC-DC CONVERTER WITH ACTIVE CLAMPING TECHNIQUE

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***Abstract* – This paper presents a new regenerative step-up/step down *DC-DC* converter, with active clamping and soft commutation. The losses in the switches are reduced due to implementation of the simple active snubber circuit, that provides *ZVS* conditions to all the interrupters of the converter, also in the auxiliary. Its main advantages are: small number of components, simple command strategy, robustness, reduced size and weight and high efficiency.**

***Keywords* – active clamping, *AGV*, *DC-DC* converter, regeneration and soft commutation.**

I. INTRODUCTION

In the industry, in the last years, the *DC* power drives have largely lost its popularity to the alternating current (*AC*) ones. The preference tor the induction machines is known, manly due to low maintenance, durability and reduced cost. However, in certain applications, *DC* machines are not easy to be replaced. They are still found, for example, in *AGV's* (*Automatic Guided Vehicles*) and in the electric fork lift trucks, used in great part of the industrial environment.

Currently, amongst the problems associated to the *AGV's*, has been pointed out the low relative autonomy of the batteries, and the necessity of the use of special machines and low voltage *DC* power drives, that usully have high cost and are difficult to be found.

This paper has as one of the main objectives, to present an alternative to power drive industrial vehicles using batteries, but making possible the use of *AC* machines and inverters, easily found in the market under reduced costs.

II. DEVELOPMENT

A.. Alternative Topology For The Power Circuit

The classic topology of the power circuit of an *AGV* can be observed in the *Figure 1*. A critical point related to the efficiency of the *DC-DC* converter is verified, and as consequence, in the autonomy of the equipment. Moreover, for the power driving, special machines are used, what increases the final cost of the product.

A possible alternative is a step-up/step-down *DC-DC* converter reversible in current, with a *CA* power drive, as illustrated on *Figure 2*.

This converter must increase the voltage of the batteries for a level that makes possible the use of power inverters and *AC* machines.

In the stage step-up/step-down, the classic converters, have low efficiency, caused by the commutation losses, with are increased due to the high frequencies, and the high levels of voltage and current on the switches. The use of this alternative topology with a soft commutation, becomes sufficiently interesting.

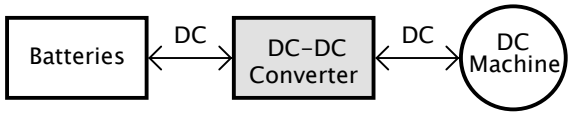

Fig. 1 Classic power topology of an AGV

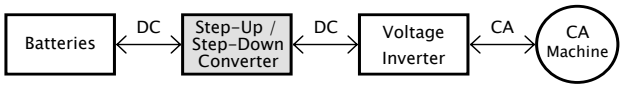

Fig. 2 Alternative power topology to an AGV

The possibility of the use of *CA* machines present considerable advantage, as already mentioned. Moreover, the energy regeneration to be used, during the braking, will contribute to make the time of use of the vehicle longer. And still, through the diverse developed techniques, the frequency inverters also allow the vehicle control with great precision.

B. Commutation Switches Considerations

The architectures that use the bridge configuration have some peculiar characteristics. At the moment that the main switch turns on, the anti-parallel diode of the bridge complementary switch begins its reverse recovery phase. During this stage the switches are submitted to a high current ramp rate *(di/dt)* and a high peak reverse recovery current I_r. Both contribute significantly to the increasing of the commutation losses and produce electromagnetic interference.

To solve this problem, diverse works had been developed by the scientific community in the last years and can be divided in two groups: Passive Techniques [1], [2], [3], [4] and [5], and Active Techniques [6], [7], [8], [9] and [10]. The main difference between the two is that the second group use controlled switches in the auxiliary circuit that helps the commutation.

Recently, some researches were made using the reverse-recovery energy from the diodes to obtain soft commutation

in the switches of the pre-regulated rectifiers with high power factor [11] and [12].

In this paper, a *new ZVS PWM step-up/step-down DC-DC converter, with active clamping technique*, is proposed. Your structure uses the reverse-recovery energy from the diodes to obtain soft commutation in all switches of circuit, including the auxiliary one.

C. Presentation And Analysis Of The Circuit

The proposed converter can be observed in the *Figure 3*. It is similar to a classic current reversible converter, with the inclusion of one auxiliary switch, one clamping capacitor and one small inductor. The capacitor *Cs* is responsible for the storage of the diode reverse recovery energy and for the clamping of switches voltage. The inductor *Ls* is responsible for the control of the *di/dt* during the diode reverse recovery time [13]. The *Figures 04* and *05* illustrate the switches commands for the modes "step up" and "step down" respectively.

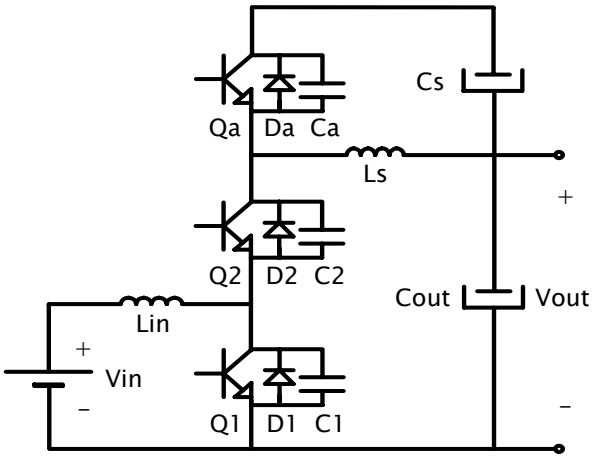

Fig. 3 Regenerative ZVS converter circuit

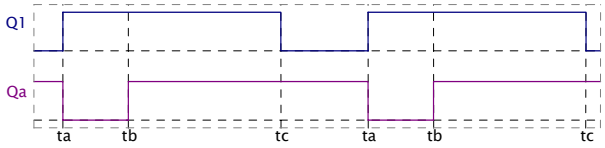

Fig. 4 Switches commands in "step up" mode

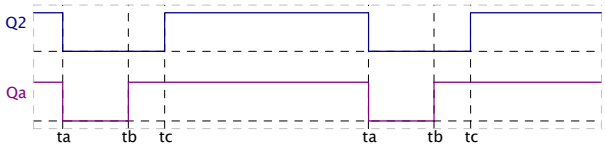

Fig. 5 Switches commands in "step down" mode

D. Operation Stages (Positive Half-Cycle)

The operation of the proposed converter is symmetrical for both positive and negative semi cycles. Thus, only for the first half cycle of the operation the circuit analysis will be made.

Some simplifications to facilitate the sketch of the operation stages of the converter will be also considered: The voltage in the capacitors C_{out} and C_s, and the current in the inductor L_{in} will be considered constant during a period of switching. Finally, the set formed by the input voltage V_{in} and the inductance L_{in}, will be simplified by a current source, called of I_{in}.

First stage (t0-t1): This interval initiates with the input current I_{in} delivering energy to the source V_{out} via diode D_2 and the inductor L_s. At the same time, the additional current i_{Cs} flows around the loop, formed by Q_a, L_s and C_s. In the end of this stage, the current i_{Cs} will reach its maximum value, called of I_f.

Second stage (t1-t2): This stage starts when the auxiliary switch Q_a is blocked. The current i_{Cs} begins the charge of the capacitor C_a from *zero* to V_{out}+V_{Cs}, and discharges C_1 from V_{out}+V_{Cs} to *zero*.

Third stage (t2-t3): At this stage the voltage across C_1 reaches *zero*, and it is clamping by the anti-parallel diode D_1. So, the switch Q_1 conducts with *ZVS* condition. At this moment, the voltage V_{out}, is applied across the inductor L_s and the currents i_{Ls} decrease linearly. The diode D_1 conducts the current i_{Ls}, while D_2 conducts the current i_{Ls}+I_{in}.

Fourth stage (t3-t4): It begins when the current i_{Ls} inverts its direction and flows through the switch Q_1. The current *i*n D_2 continues to decrease until inverting its direction, starting its reverse recovery phase. The inductor L_s limits the di_{Ls}/dt. In the end this stage the current in L_s is equal to I_r.

Fifth stage (t4-t5): This stage starts when the diode D_2 finishes its reverse recovery phase. The current i_{Ls} begins the charge of the capacitor C_2 from *zero* to V_{out}+V_{Cs} and the discharge of C_a from V_{out}+V_{Cs} to *zero*.

Sixth stage (t5-t6): At this stage the voltage across the capacitor C_a reaches *zero*, and it is clamped by the diode D_a. Thus, the auxiliary switch Q_a conducts with zero-voltage switching. The current i_{Ls} increase, due the application of the voltage V_{Cs} across the inductor L_s. This stage finishes when the current in L_s reaches *zero*.

Seventh stage (t6-t7): This stage begins when the current i_{Ls} changes its direction and flows through the switch Q_a. The current i_{Ls} continues to increase linearly.

Eighth stage (t7-t8): At this stage the switch Q_1 is blocked, and the current in C_s inverts its direction and flows through the diode D_a. The capacitor C_1 is charged from *zero* to V_{out}+V_{Cs} and the capacitor C_2 is discharged from V_{out}+V_{Cs} to *zero*.

Ninth stage (t8-t0): It begins when the voltage across the capacitor C_2 reaches *zero*, and it is clamped by the diode D_2. The current i_{Ls} continues increasing. This stage finishes when i_{Ls} is equal to I_{in}, and flows through the auxiliary switch Q_a, restarting the first operation stage.

The circuital sketch of the mentioned stages of operation, and the respective waveforms, can be visualized in Figures 06 and 07, respectively.

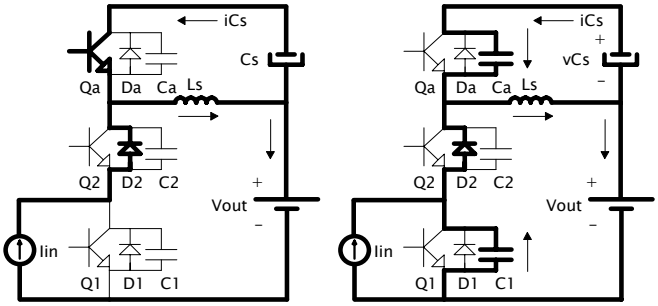

Fig. 6.a First stage (t0-t1) and Second stage (t1-t2)

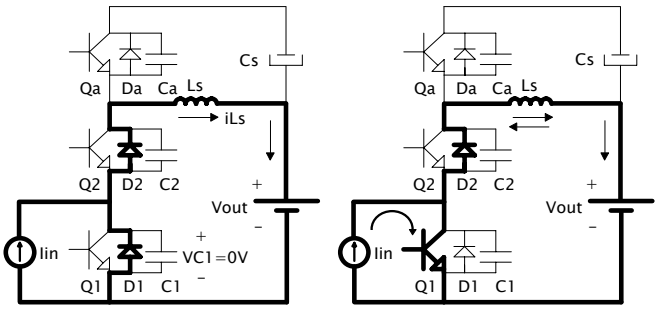

Fig. 6.b Third stage (t2-t3) and Fourth stage (t3-t4)

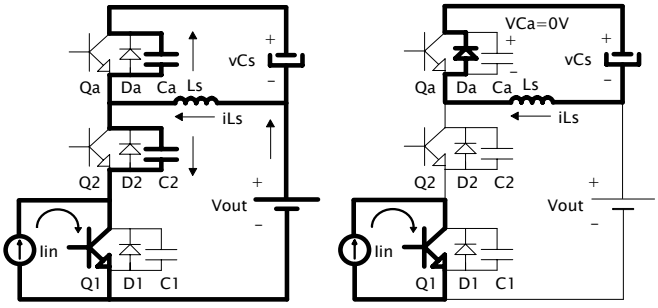

Fig. 6.c Fifth stage (t4-t5) and Sixth stage (t5-t6)

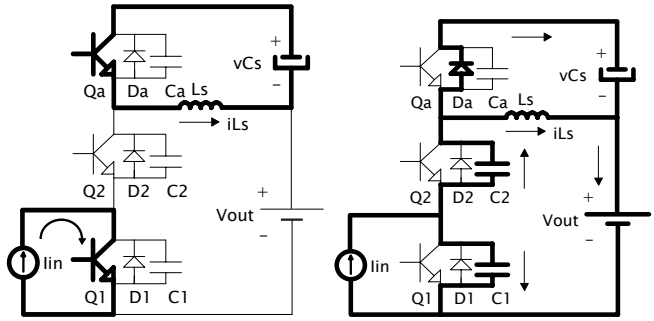

Fig. 6.d Seventh stage (t6-t7) and Eighth stage (t7-t8)

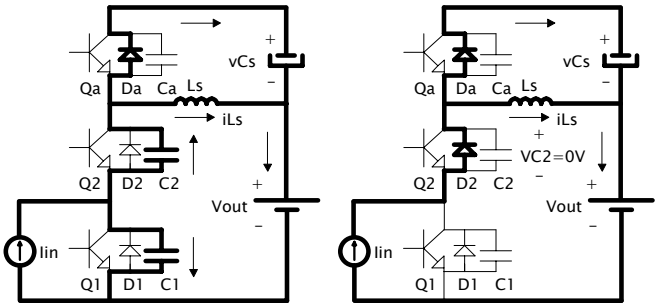

Fig. 6.e Eighth stage (t7-t8) and Ninth stage (t8-t0)

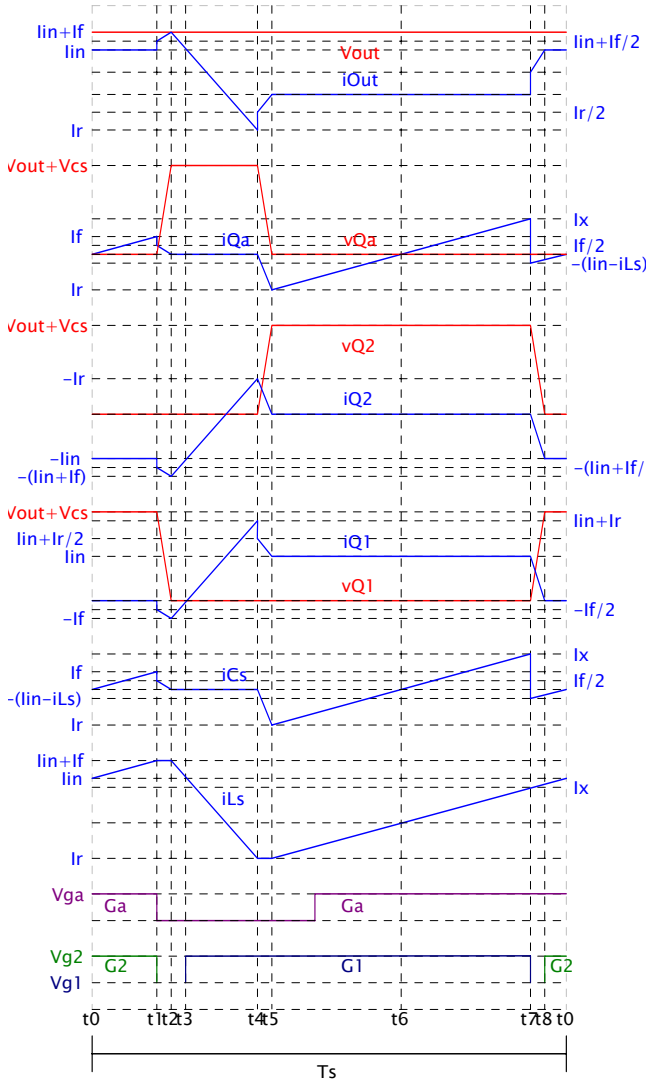

Fig. 7 Theoretical waveforms

E. Mathematical Analysis

The output voltage converter is controled by the duty cicle *D*, as follow:

$$D = \frac{Vout - Vin}{Vout} \qquad (1)$$

The inductor *Lin* can be calculed by the use of the equation (2), as follow:

$$Lin = \frac{Vin \times Ts}{\Delta Iin} \cdot D \tag{2}$$

One of the most important caracteristics of the proposed converter is the voltage clamping over the switches. As indicated previously, its maximum voltage applied is *Vcs* + *Vout*. For the correct specifications of the components its necessary to know *Vcs*. The average current in *Cs* must be zero to one period of switching in steady state conditions. Thus, its not dificult to see the follow relation:

$$iCs_{ave} = \frac{1}{Ts}\left[\int_{0}^{t7}\left(\frac{Vcs}{Ls}\cdot t - Ir\right)dt + \int_{t7}^{t1}\left(\frac{Vcs}{Ls}\cdot t - Iin - Ir\right)dt\right] \tag{3}$$

Where, *Ts* is the switching period.

Solving (3) and considering the expressions (4), (5) and (6), its possible to get the equation (7).

$$D = \frac{t7}{Ts} \tag{4}$$

$$t1 \approx Ts \tag{5}$$

$$iCs_{ave} = 0 \tag{6}$$

$$Vcs = \frac{2Ls}{Ts}\left[Ir + Iin(1-D)\right] \tag{7}$$

The input current *Iin* can be calculed by the use of the equation (8), as follow:

$$Iin = \frac{Pout}{\eta \cdot Vin} \tag{8}$$

Where, η is the efficiency of the converter.

By link of the equations (7) and (8) its possible to get the equation (9):

$$Vcs = \frac{2 \cdot Ls}{Ts}\left[Ir + \frac{Pout(1-D)}{\eta \cdot Vin}\right] \tag{9}$$

As mentioned previously, *Ir* is the maximum value of the reverse recovery current of the anti-parallel diode. There it can be obteined by the equation (10), as follow:

$$Ir = \sqrt{\frac{4}{3} \cdot Qrr \cdot \frac{Vout}{Ls}} \tag{10}$$

Where, *Qrr* is the reverse recovery charge.

To guarantee *ZVS* conditions, it is necessary, in the second stage, that the stored energy in the inductor *Ls* be sufficient to discharge the capacitor *C1* and to charge *Ca*. Thus, by inspection of Fig. 6.a (Interval t1-t2) the following condition can be formulated:

$$Ls \cdot If^{2} \geq (Ca + C1)(Vout + Vcs)^{2} \tag{11}$$

Where *If* is the maximum current in *Cs*, and *Vcs* is maintained constant during a switching period. Assuming *Vcs*<<*Vout* we have:

$$If\ \min \geq Vout\sqrt{\frac{C1 + Ca}{Ls}} \tag{12}$$

Where, its possible to use *C1* = *Ca*.

The equation (12) to indicate the minimum value that the current *If* must be to agree the ZVS commutation in all range to a determined condition of load.

An expression to the current *If* can be obtained by the analysis of the current in the capacitor *CS*. Thus:

$$If = \frac{Vcs}{Ls} \cdot Ts - \frac{Iin}{2} - Ir \tag{13}$$

This way, *If* can be obtained by use of equation (13), but your value must be bigger than the obtained in the equation (12).

The inductor *Ls*, that is responsible to the control of the current ramp rate, can be calculed by the use of the equation (14), as follow:

$$Ls = \frac{Vout}{di/dt} \tag{14}$$

F. Project Results Summary

Following the equations of the mathematical analysis, the information had been concentrated through tables.

Thus, the initial design specifications, and the main results can be observed in the *Tables 01* and *02*, respectively.

TABLE I
Initial Design Specifications

V_{in} = 48Vcc	Input Nominal Voltage
V_{out} = 200Vcc	Output Nominal Voltage
P_{out} = 1000W	Output Nominal Power
η = 95%	Esteem Efficiency

TABLE II
Main Results

D = 0,76	Modulation Factor
F_s= *40kHz*	Switching Frequency
L_s = *10μH*	Auxiliary Inductance
L_{in} = *830μH*	Input Inductance
I_{in} = *22A*	Input Current
I_r = *28A*	Reverse Recovery Current
V_{Cs} = *13,5V*	Clamping Voltage
I_f = *28,5A*	Current on the Capacitor C_s
I_{out} = *5A*	Output Current
C_{out} = *475μF*	Output Capacitor

TABLE III
Main Components Specifications

Q_1, Q_2, Q_a	Switches: *APT5010B2VR*
D_1, D_2, D_a	Switches Intrinsic Diodes
C_1, C_2, C_a	Switches Intrinsic Capacitances *(≅5nF)*
L_{in}	Iron-Silicon Inductor: *Ap*=34,81cm^2, *Ac*=6,8cm^2, *Wa*=5,12cm^2, *nfp*=36, wires=23AWG, 21 turns, and *lg*=0,041cm.
L_s	Ferrite Inductor: *IP6-EE42/20*, *nfp*=20, wires=23AWG, 17 turns, and *lg*=12,85mm.
C_s	Electrolytic Capacitor: 2 x 470uF/400V
C_{out}	Electrolytic Capacitor: 2 x 470uF/400V

G.Experimental Waveforms

In *Figure 8* are presented the signals to the command of the switches Q_1, Q_2 e Q_a. In the *Figures 9* and *10* are showed the voltage and current in Q_1. Of similar form, in the *Figures 11* and *12* are showed the voltage and current in Q_a. Finally, on *Figure 13* is presented the voltage over de capacitor C_s, and on *Figure 14* the efficiency.

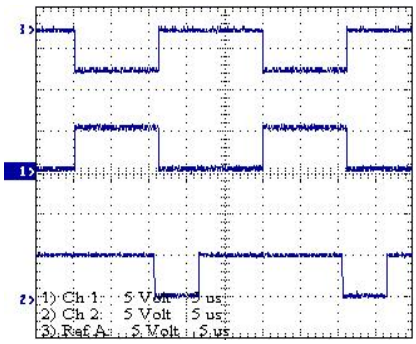

Fig. 8 Signals OUT 1 (Ch1), OUT 2 (RefA) and OUT A (Ch2) - 5V/div

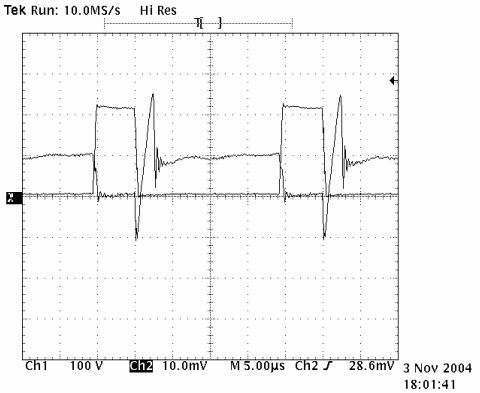

Fig. 9 Voltage (100V/div) and Current (5A/div) in Q_1

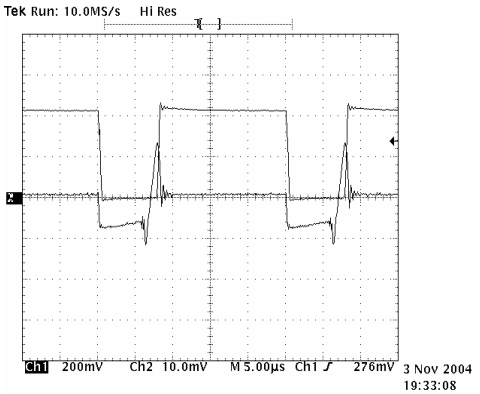

Fig. 10 Voltage (100V/div) and Current (5A/div) in Q_2

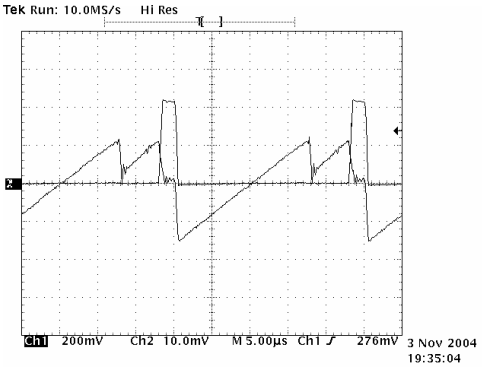

Fig. 11 Voltage (100V/div) and Current (5A/div) in Q_a

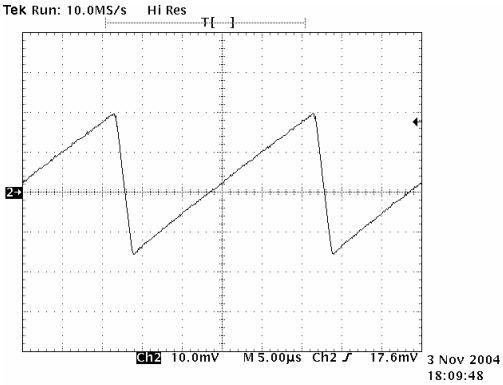

Fig. 12 Current in L_s (5A/div)

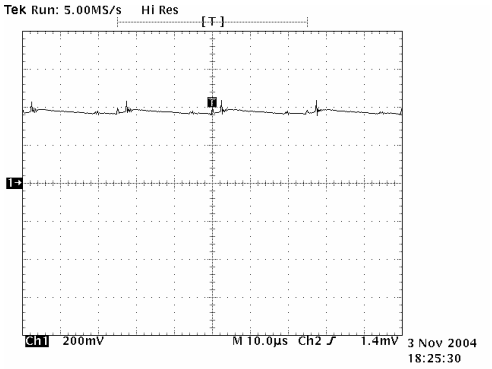

Fig. 13 – Voltage (10V/div) on Capacitor C_s

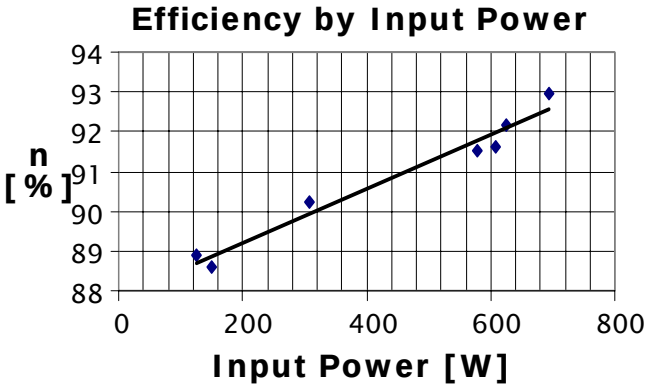

Fig. 14 Converter Efficiency

III CONCLUSIONS

This paper showed a *new ZVS PWM step-up/step-down DC-DC converter, with active clamping technique*. Was presented the operational stages, the values obtained of the equations, the mains waveforms and experimental results.

The converter was not tested in the nominal rated power because a limitation of our laboratory equipament. However, with base on others works already elaborated, and with the gotten results, many conclusions had become possible. The voltage in the clamping capacitor it revealed low, privileging the sizing of the switches - low stress voltage. It was verified soft commutation, confirming the theoretical studies, and the losses in the switches had been inside of the waited one. As consequence, could have been used small heat dissipations, reducing the weight, the volume and the costs.

Beyond of that was said previously, it could be affirmed that the soft commutation brings, inherently, a reduction of the electromagnetic interference generated by the converter.

Finally, the main advantages associates were: use of a small number of components, simple command strategy, robustness, reduced size and weight, low harmonic distortion of current and high efficiency.

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