FREQUENCY COMPENSATION FOR STAND ALONE VOLTAGE-CONTROLLED DSTATCOM

Rubens Tadeu Hock Júnior, Yales Rômulo de Novaes, Alessandro Luiz Batschauer
Santa Catarina State University, Joinville – Santa Catarina, Brazil
rubens.t.hock@ieee.org, novaes@ieee.org, alessandrobatschauer@udesc.br

***Abstract* – This paper presents a simple control loop for voltage-controlled DSTATCOMs able to mitigate the effects of grid frequency deviation, greatly increasing the voltage regulation autonomy. The DSTATCOM consists of a three-phase four-wire Voltage Source Inverter (VSI) connected to the grid through a second order low pass filter. The control structure is composed of the conventional loops: three for the output voltage with active damping, and two for dc bus voltages, along to the frequency loop. The inclusion of the frequency loop makes the grid voltage phase information no longer needed. In other words, only the PCC voltage information is needed for the DSTATCOM operation. Experimental results prove its features and the effectiveness of the new loop.**

***Keywords* – DSTATCOM, Frequency Compensation.**

I. INTRODUCTION

The available voltage for end users in low voltage distribution grids may drop below the minimum or rise above the maximum rms voltage, as described in [1]. Also, the energy distribution company has a constrained time frame to provide the final solution when this issue is detected. If the time to solve the issue is longer than the allowed time frame, the energy distribution company may be penalized and affected consumers are refunded.

Aiming to avoid these penalties or investments on infrastructure with short deadline, a mobile voltage regulator is proposed. The voltage regulator must have some features: fast voltage regulation, low volume and easy installation. Among the voltage regulation possibilities, a voltage-controlled DSTATCOM is proposed [2]. DSTATCOMs inject quadrature current (lagging or leading) with the PCC voltage, emulating an inductive or a capacitive reactance [3].

Voltage-controlled DSTATCOMs need a reference to their angular position [4]. This can be achieved by measuring the grid voltage and using PLL circuits [5]. This method has a significant problem: in real distribution networks the grid voltages are distant from the PCC, represented in Figure 1 by a distributed model of grid impedance and loads.

In previous papers, voltage-controlled DSTATCOMs use the grid voltage phase or zero crossing information to compose the PCC voltage reference [5-7], making this an unlikely solution and difficult to implement in a real application due the distance between the PCC and the grid voltage. Figure 2 presents a real distribution grid which voltage phase information (at the transformer) is around 130 meters away from the PCC.

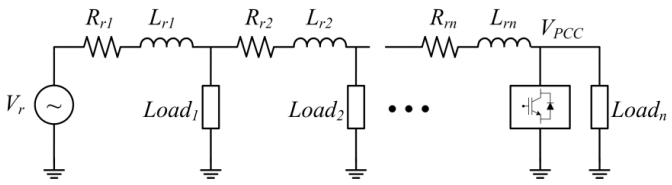

Fig. 1. Grid representation with distributed loads

As soon as the converter is connected to the PCC, the information about the grid voltage instantaneous frequency and angle can be obtained by the grid voltage and impedances. At this stage, PLL circuits provide the initial angular position to the DSTATCOM. Once the converter begins its compensation, the PCC voltage is replaced by the converters voltage. After that, that information is lost and the PCC frequency and angle is given by the DSTATCOM.

This paper proposes a simple method to acquire the grid frequency through the PCC voltage making the DSTATCOM independent of the grid voltage measurements.

II. CONTROL STRUCTURE

The control structure for the DSTATCOM is shown in Figure 3, which is composed by three output voltage loops, one total dc bus voltage loop, one differential dc bus voltage loop and the proposed frequency loop.

The output voltage loops are composed by three active damping controllers and three output voltage controllers. The damping controllers attenuate the resonant peak of the equivalent LCL filter, composed by the converter LC filter and the grid series inductance. The damping controller outputs are subtracted from the output of the output voltage controller and attenuate resonant dynamics on the PCC voltage.

The output voltage loops are responsible for the synthesis of three sinusoidal, balanced voltages at the PCC. The output

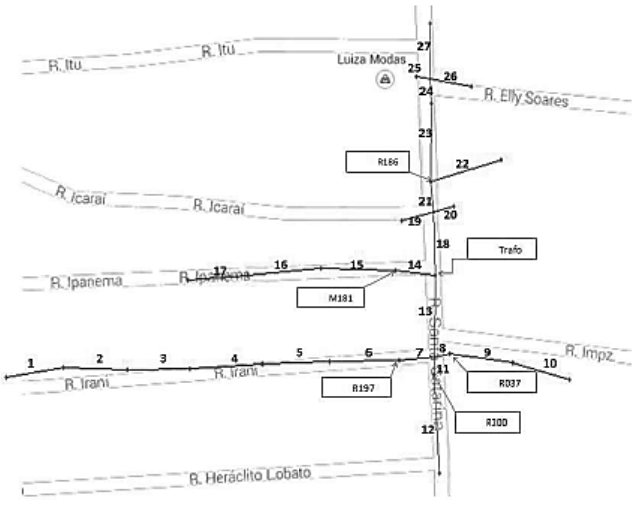

Fig. 2. Real grid with voltage regulation issue at point 4 [8]

978-1-4799-8779-5/15/$31.00 ©2015 IEEE

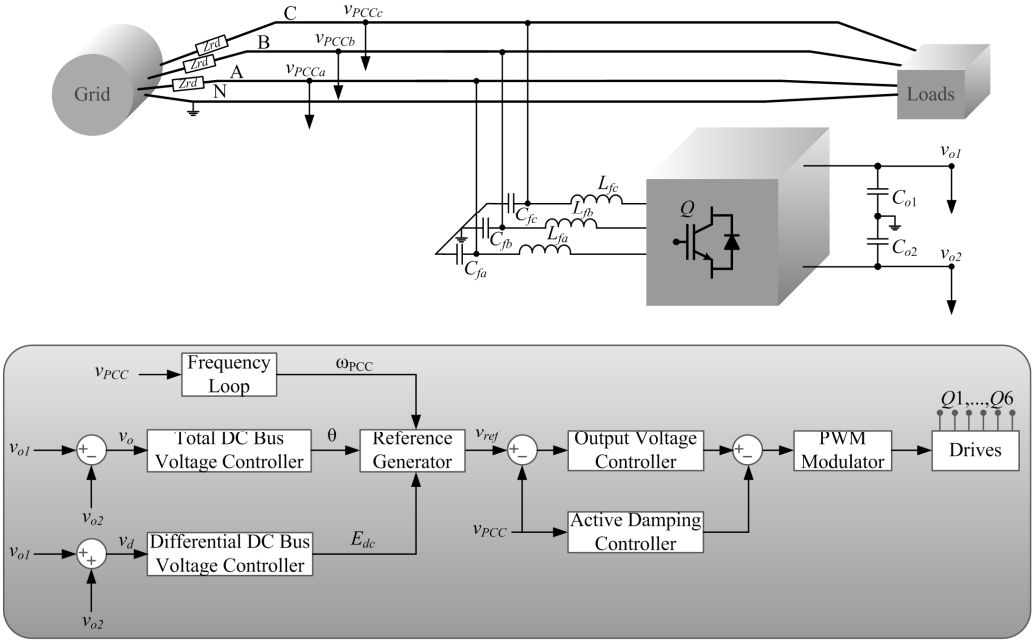

Fig. 3. Proposed control structure including the frequency loop

voltage controllers are greatly influenced by the active damping loop which shall be designed posteriorly.

The dynamic model for the output voltage loop is given by:

$$\frac{v_{Cf}(s)}{d(s)} = \frac{s \cdot V_o \cdot L_r + V_o \cdot R_r}{s^3 \cdot L_f \cdot L_r \cdot C_f + s^2 \cdot R_r \cdot L_f \cdot C_f + s \cdot L_f + L_r + R_r} \quad (1)$$

The active damping controller is a double stage lead controller tuned on the resonance peak of (1) and the output voltage controller is a PID. The crossover frequency of the output voltage loop is 2.6 kHz with the phase margin of 81.8º.

The total dc bus voltage loop regulates the total voltage, v_o, through the change in the angle θ of the reference voltages, absorbing a small amount of active power to supply the losses. The dynamic model for the total bus voltage loop is [9]:

$$\frac{v_o(s)}{\theta(s)} = -\frac{3 \cdot V_r \cdot V_{PCC}}{s \cdot \omega \cdot L_r \cdot C_{oeq} \cdot V_o} \quad (2)$$

The total dc bus voltage controller is a PI plus a high frequency pole. The crossover frequency is 26 Hz with phase margin of 77.7º

The differential dc bus voltage loop adds a little dc component, E_{dc}, in the voltage references, in order to keep the difference between the voltages across the capacitors, v_d, near to zero. The dynamic model for the differential bus voltage loop is:

$$\frac{v_d(s)}{v_{PCC}(s)} = \frac{3}{s \cdot R_r \cdot C_o} \quad (3)$$

The differential dc bus voltage controller is also a PI plus a high frequency pole. The crossover frequency is 1.2 Hz with phase margin of 76.5º.

The frequency loop calculates the PCC frequency by capturing the PCC voltage zero crossings and replaces the past frequency measurement by the new one through a DSP TMS320F28335 from Texas Instruments®.

The reference generator creates three-phase balanced sine waves according to (4) using the angle θ, the reference frequency (f_{ref}) and the dc component E_{dc}. The amplitude E is kept constant at a value related to the nominal PCC voltage, i.e. 311 V. An example of variation in E in order to minimize the reactive power of the DSTATCOM can be found in [2].

$$v_{ref\_k} = E \cdot \sin\left(2 \cdot \pi \cdot f_{ref} \cdot t - \theta - \frac{2 \cdot \pi}{3} \cdot k\right) + E_{dc} \quad k = 0,1,2 \quad (4)$$

III. FREQUENCY LOOP

The grid frequency has variations around the nominal value due the continuously load changes and many loads operate regardless of the grid frequency variations. However, voltage-controlled DSTATCOMs may have a compromised operation and, depending of the variation magnitude/duration, the disconnection is inevitable.

A. Grid Frequency Variation and the dc Bus Controller

The voltage reference (v_{ref}) of the DSTATCOM is composed by four input signals, as seen in (4). Disregarding the amplitude and the dc components, the simplified voltage reference is given by (5), highlighting the two main information for this analysis: reference frequency (f_{ref}) and compensation angle θ.

$$v_{ref} = \sin\left(2 \cdot \pi \cdot f_{ref} \cdot t - \theta\right) \quad (5)$$

If the grid frequency (f_r) is constant, one can assume that the f_{ref} is equal to the PCC frequency (f_{PCC}) and θ is constant. When f_r changes, the total dc bus voltage controller ensures

that f_{PCC} is the same as f_r through a no constant control action. The compensating angle is composed by a constant (Θ) and a time variant ($\theta(t)$) component, according to (6).

$$\theta = \Theta + \theta(t) \tag{6}$$

The voltage reference is, therefore, written as:

$$v_{ref} = \sin\left[2 \cdot \pi \cdot f_{ref} \cdot t - \theta(t) - \Theta\right] \tag{7}$$

The term f_{ref} - $\theta(t)$ is the effective frequency at the PCC (f_{PCC}).

$$f_{PCC} = f_{ref} - \frac{\theta(t)}{2 \cdot \pi} \tag{8}$$

B. Impacts of the Grid Frequency Variation

Any deviation between f_r and f_{PCC} has two main impacts on the voltage-controlled DSTATCOM: a no constant total dc bus action control and a steady time error for the total dc bus voltage [9].

The steady time error can be great and depends on the frequency deviation magnitude and the total dc bus controller bandwidth. If the steady time error is negative, the modulation index increases and can reach the unity, compromising the PCC voltage quality. If positive, there is an overvoltage across the dc bus capacitors, which can be higher than the rated voltage.

The no constant control action has a significant impact when it is composed of analog circuits: the total dc bus voltage controller has limited control actions. When the minimum or maximum compensating angle (θ) is achieved, the angle is kept to the limit value and, therefore, the controller cannot regulate the total dc bus voltage. In this case, there is no option but shutting down the converter, implying in serious consequences to PCC costumers and the energy distribution company.

C. Proposed Method

The proposed method to compensate the impact of the grid frequency variation is done by equalizing the PCC frequency (f_{PCC}) and the grid frequency (f_r). This is performed by the natural behavior of the total dc bus controller. Through the measurement of f_{PCC}, f_r is obtained. Periodically updating the reference frequency (f_{ref}) by the measured f_{PCC}, the main goal of the frequency loop is achieved, which is to bring the term θ(t) to zero in (8) at each frequency update.

One easy way to get this information is counting the time between each zero cross of the PCC voltage. The measured frequency feeds the reference generator every 100 ms. To grant robustness, a low pass filter is included, removing possible multiple zero crossings. Also, to avoid miscalculations, only frequency measurements between 58 Hz and 62 Hz are considered.

Figure 4 presents the relationship between the frequencies when a 0.1 Hz step is applied to f_r, emphasizing that the f_{PCC} will be equal to f_r due the total dc bus controller, regardless of the f_{ref}. With the frequency loop, updated in 0.3 s, f_{ref} is equal to f_{PCC} and, therefore, equal to f_r.

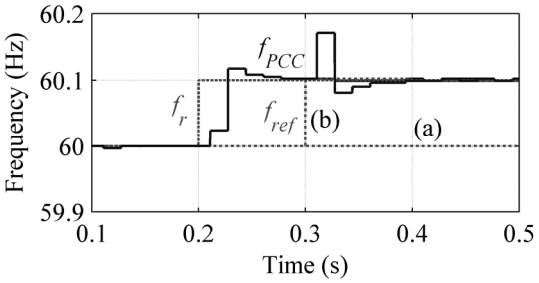

Fig. 4. Simulation result: relationship between the grid, PCC and reference frequencies (a) without and (b) with the frequency compensation

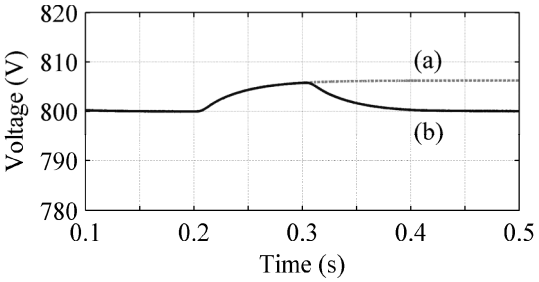

Fig. 5. Simulation result: total dc bus voltage during the grid frequency variation (a) without and (b) with the frequency compensation

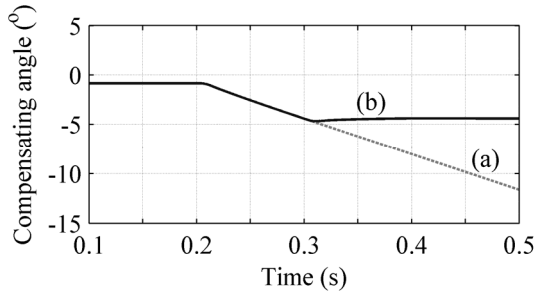

Fig. 6. Simulation result: compensation angle during the grid frequency variation (a) without and (b) with the frequency compensation

The grid frequency step causes a small steady time error around 5 V in the total dc bus voltage. With the frequency loop, the dc bus voltage returns to nominal value when the grid and reference frequencies are equal, as seen in Figure 5.

Figure 6 presents the effect in the total dc bus controller under the same frequency step. Without the frequency loop, the compensating angle will decrease indefinitely, whereas with the frequency loop the compensating angle stop decreasing when the frequencies became equal.

The compensating angle, with the method, doesn't return to previous value when the grid and reference frequencies are balanced. Therefore, the effect of the unequal frequencies is accumulated in the compensating angle, which may lead the controller to saturation.

If the saturation is imminent, a protective routine is enabled, forcing the compensating angle to return to 0 rad by adding a constant factor in f_{ref}. After that, the frequency loop returns to its normal operation.

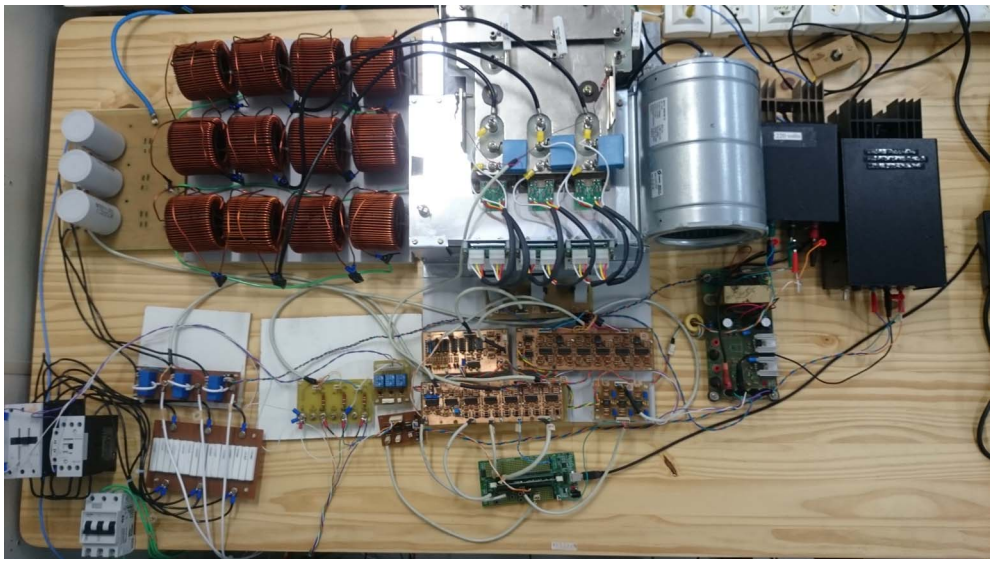

Fig. 7. Experimental prototype

IV. EXPERIMENTAL RESULTS

The frequency loop was implemented in a 30 kVA VSI prototype, seen in Figure 7, with the parameters listed in Table I.

Figure 8 shows the PCC frequency measurement (f_{PCC}), the updated reference frequency (f_{ref}) and the grid frequency (f_r) obtained via internal memory of DSP.

The following experimental results were obtained via oscilloscope csv files edited in MATLAB®.

The compensating angle from the total dc bus voltage controller for a large amount of time is presented in Figure 9 with the proper voltage/frequency scale. One can see that the compensating angle has ripples, with a similar behavior as the measured frequency. Even though, the frequency loop was capable of maintaining the converter operation with a low angle increasing through 100 seconds. During this time, the converter was able to operate without reaching the limits, so the control loop achieved its purpose.

The dc bus voltages are regulated at the nominal value with low voltage ripple due the continuous frequency updates, as shown in Figure 10.

As mentioned in Section III, only the frequency update cannot guarantee the operation under any type of disturbances and indefinitely. In this case, a frequency protection routine was implemented, where the routine decreases the PCC voltage frequency by a constant factor, bringing the compensation angle back to zero. An example of the protection routine can be seen in Figure 11.

TABLE I
DSTATCOM parameters

Nominal Power	S_o	30 kVA
Nominal dc bus voltage	V_o	800 V
Grid voltage	V_r	220 V
Grid frequency	f_r	60 Hz
Switching frequency	f_s	20 kHz
Equivalent dc bus capacitance	C_{oeq}	3500 µF
Output filter inductance	L_f	560 µH
Output filter capacitance	C_f	47 µF
Grid resistance	R_r	0.685 Ω
Grid inductance	L_r	1.82 mH

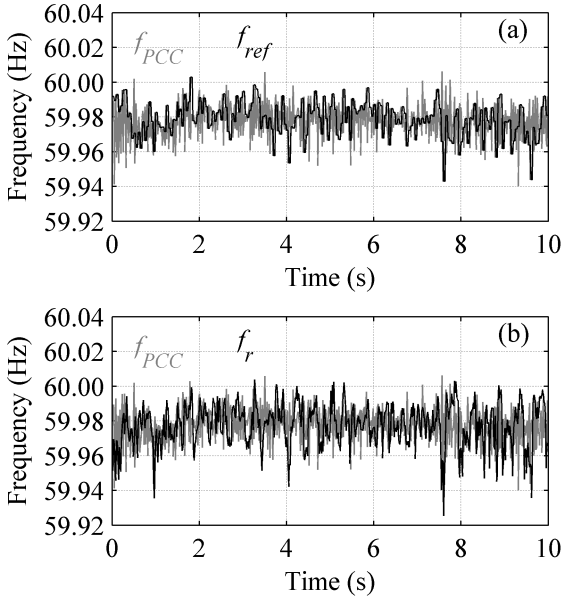

Fig. 8. Experimental result: measured frequencies PCC and (a) reference and (b) grid

Figure 12 presents the total dc bus voltage when the protection routine is enabled. The total voltage has 13 V step and returns to nominal voltage in around 1 second.

When the total dc bus controller is rejecting the continuous grid frequency variations, some of its compensating capability is compromised. Even so, the total dc bus controller successfully regulates the total dc bus voltage under a sudden load change, as seen in Figure 13.

The compensating angle, Figure 14, has a similar behavior as depicted in Figure 9, excluding the angle step at the load change instant.

V. CONCLUSION

This work proposes a simple method to enhance the autonomy of a voltage-controlled DSTATCOM in a low voltage distribution grid without any kind of grid voltage information. The frequency loop updates the reference

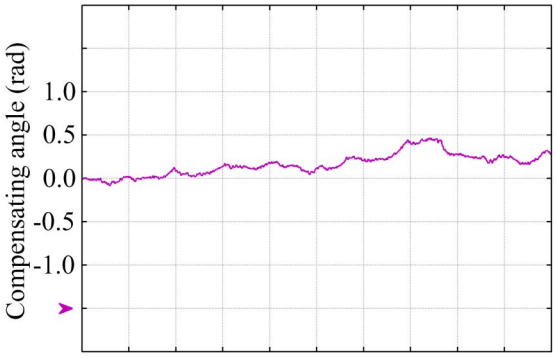

Fig. 9. Experimental result: compensating angle (500 mV/div, 10 s/div) in radians

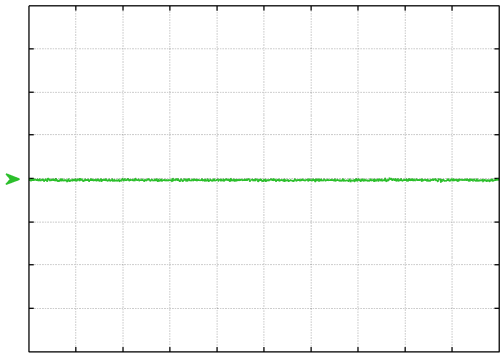

Fig.10. Experimental result: total dc bus voltage (50 V/div, 10 s/div) with the frequency compensation

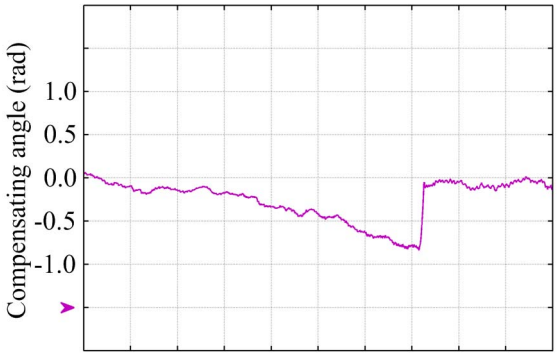

Fig.11. Experimental result: compensating angle (500 mV/div, 10 s/div) in radians under the protection routine

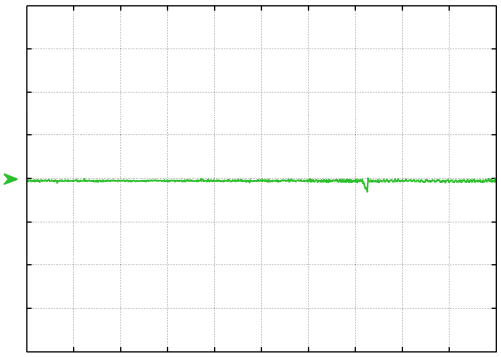

Fig.12. Experimental result: total dc bus voltage (50 V/div, 10 s/div) under the protection routine

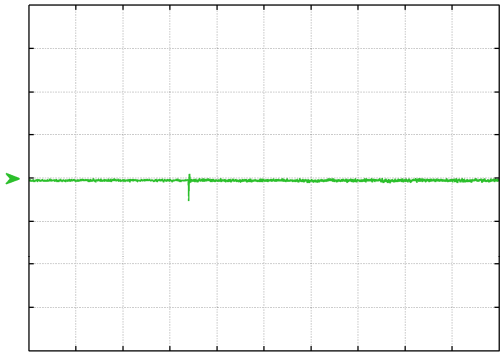

Fig.13. Experimental result: total dc bus voltage (50 V/div, 10 s/div) under a sudden load change with the frequency compensation

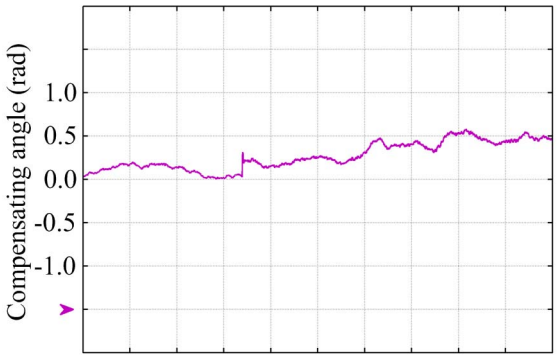

Fig.14. Experimental result: compensating angle (500 mV/div, 2 s/div) in radians under a sudden load change

analog limits and the dc bus voltage regulated at nominal value.

The proposed DSTATCOM is connected in parallel to the PCC, providing easy and fast installation and also maintain the grid reliability. Along with the conventional loops, the DSTATCOM composes a complete solution for voltage-controlled regulators.

ACKNOLEDGEMENTS

The authors would like to thank “Centrais Elétricas de Santa Catarina – CELESC” for the funding, Santa Catarina State University – UDESC, “Fundação Instituto Tecnológico de Joinville – FITEJ” and “Fundação de Amparo à Pesquisa e Inovação do Estado de Santa Catarina – FAPESC” for supporting this project.

REFERENCES

[1] ANEEL, *Procedimentos de Distribuição de Energia Elétrica no Sistema Elétrico Nacional – PRODIST* (in Portuguese), *Módulo 8 – Qualidade da Energia Elétrica,* 2001.

[2] R. T. Hock, Y. R. De Novaes and A. L. Batschauer, “A voltage regulator based in a voltage-controlled DSTATCOM with minimum power point tracker,” in *IEEE Energy Conversion Congress and Exposition (ECCE) 2014*, 2014.

[3] B. Singh, R. Saha, A. Chandra and K. Al-Haddad, "Static synchronous compensators (STATCOM): a review," *IET Power Electronics,* vol. 2, n. 4, pp. 297-324, July 2009.

[4] G. Ledwich and A. Ghosh, "A flexible DSTATCOM operating in voltage or current control mode," *IEE Proceedings-Generation, Transmission and Distribution,* vol. 149, n. 2, pp. 215-224, 2002.

[5] S.-H. Ko, S. Lee, H. Dehbonei and C. Nayar, "Application of voltage- and current-controlled voltage source inverters for distributed generation systems," *IEEE Transactions on Energy Conversion,* vol. 21, n. 3, pp. 782-792, Sept 2006.

[6] C. Kumar and M. Mishra, "A Multifunctional DSTATCOM Operating Under Stiff Source," *IEEE Transactions on Industrial Electronics,* vol. 61, n. 7, pp. 3131-3136, July 2014.

[7] C. Kumar and M. Mishra, "A Voltage-Controlled DSTATCOM for Power-Quality Improvement," *IEEE Transactions on Power Delivery,* vol. 29, n. 3, pp. 1499-1507, June 2014.

[8] "Centrais Elétricas de Santa Catarina - CELESC". Technical Report, 2013.

[9] T. P. Enderle, "Análise, Projeto e Implementação de um D-STATCOM para Redes de Distribuição Monofásica", Master Thesis, Federal University of Santa Maria, Santa Maria, RS, 2012.