A DC-DC ZVS PHASE-SHIFT PWM FULL-BRIDGE CURRENT-MODE CONTROLLED CONVERTER WITH MULTIPLES OUTPUTS FOR PHOTOVOLTAIC APPLICATIONS

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***Abstract* – This work proposes a new application of a DC-DC zero-voltage switching (ZVS) full-bridge converter in a photovoltaic (PV) energy system. On its input is connected a photovoltaic array, mostly parallel connected, resulting in a low voltage input. The control applied to the converter is a peak current-mode control, controlling its input current and performing the maximum power point (MPP) tracking (MPPT). The DC-DC converter provides three current outputs isolated by a high frequency transformer for a three-phase line-commutated 18-pulse inverter. Results of a 2.3kW converter simulation and preliminary experimental results are presented.**

***Keywords* – DC-DC power converter, High-gain converter, Peak current-mode control, PV array, ZVS.**

INTRODUCTION

With the use of photovoltaic energy growing in the last decade, plenty of works have been published showing its positive points, negative and better ways of using this clean energy. To use photovoltaic energy as alternative to the electric grid, or to consume it as alternate current, the use of an inverter and PV modules is necessary. A recent published study showed the use of line-commutated inverters connected to an autotransformer, resulting in an 18-pulse inverter as alternative to the usual PWM inverters, which are widely used to inject electric energy in the power grid. Despite being a low-cost and robust structure [1-2], there are a few features that need to be mitigated. They can be listed as the lack of galvanic isolation between the power grid and the PV array, resulting in high common-mode currents, the requirement of three isolated current sources, originally formed by series connected PV array, and the unusual maximum power point tracker, which is made changing the firing angles of the SCRs and consequently changing the power factor of the energy delivered to the power grid.

In this work, the addition of a DC-DC converter between the PV array and the line-commutated inverter is proposed, as showed in Figure 1. The use of a high-frequency converter allows a better and refined process of the PV power, draining low ripple current, and operating at MPP with low oscillation. The DC-DC converter can operate in a large range of input voltage, achieving high efficiency draining the PV array generated energy.

The PV array can be rearranged to a better configuration allowing a better fill-factor array association, improving the system performance in the occurrence of shading. The proposed converter steps-up the PV voltage to the required levels of the 18-pulse inverter through a high-frequency transformer. The MPPT applied on the proposed converter keeps the power factor of the line-commutated inverter fixed. The high-frequency transformer provides the isolation between the PV array and with its multiple outputs isolates each input of the inverter. The outputs of the converter have current source characteristics, providing a low ripple current and simplifying the connection with the inverter.

A fill-factor based search is made among the most usual PV arrays structures to find the best performance in shading conditions. Shading can cause a significant reduction in the power of the array [3-5], and by-pass diodes are usually employed to reduce shading influences in some configurations [6].

A peak current-mode control (PCMC) in the primary-side of the transformer is proposed. The current is controlled in the input of the converter, where the peak current of all semiconductors of primary side can be measured. This control also protects the semiconductors from overcurrents. Another benefit of using this control technique is the absence of DC removal capacitors in series with the primary of the power transformer [7].

A MPPT technique is applied to control the MPP of the PV array through the input current of the converter. The PV array current is measured by the same sensor that acquires the instantaneous current for the PCMC. After the signal passes a low-pass filter, the amplitude of the signal is equivalent to the mean value of the PV array current.

The algorithm used in the MPPT is an incremental conductance, which tracks the MPP and maintains it with no oscillation.

In Table I the electrical characteristics of the input and output of the proposed converter are described.

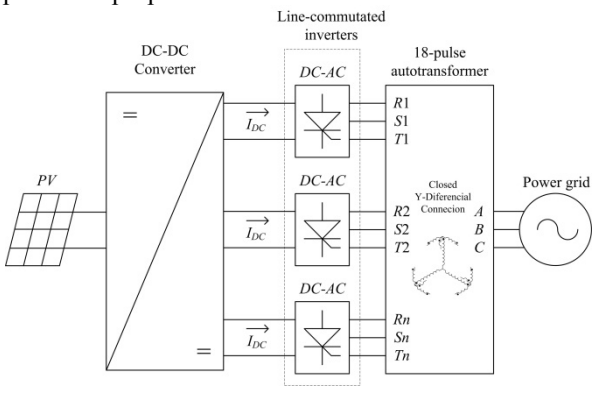

Fig. 1 Proposed system connection.

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TABLE I
Electric specification of the power converter

Characteristic	Value	minimum	Nomenclature
Power Input	2340W	302.4W	P_{in}
Input Voltage	52V	36V	V_{in}
Output Voltage	261.2V	-	V_o
Input Current	44.94A	8.4A	I_{in}
Switching Frequency	70kHz	-	f_s
Effective duty-cycle	0.855	-	D_{eff}

II. PHOTOVOLTAIC ARRAY CHARACTERISTICS

This section discusses how the structure of the PV array was chosen. The criterion of evaluation was the Fill-Factor and its robustness towards PV shading.

A. Fill-Factor

Fill-Factor (FF) is a figure of merit of a PV cell [8-10] that can be extended to PV module and arrays as well. It measures how close to ideal is the V *vs* I PV curve, relating its maximum power to the theoretical total power, i.e. the product of short-circuit current with the open-circuit voltage. Its mathematical expression is shown in equation (1). This value may vary depending on the used technology and on the modules array configuration.

$$FF = \frac{P_{MAX}}{P_{TOT}} = \frac{I_{MPP} \cdot V_{MPP}}{I_{SC} \cdot V_{OC}} \quad (1)$$

In Figure 2 is shown a graphical representation of the fill-factor for a clear understanding. Depending on the technology of the PV module and the array configuration different fill-factor can be achieved. In this study the fill-factor will be used to compare the performance of different PV arrays structures, because all the PV modules have the same technology and manufacturer.

B. The array configuration

This work was firstly intended to have a low voltage on PV side with the maximum possible parallel PV array. Analysis and simulations of different high-gain converters have shown that the current stress in semiconductors was not viable, and an increase in the input voltage was necessary through series association of PV modules. Therefore, the array configuration must have at least three PV modules in series connection to reduce the current stress maintaining the same initial power.

The total-cross-tied (TCT) array configuration is a variation of series-parallel (SP) configuration and is widely used because of its better characteristics towards others configurations. This configuration is recommended to reduce shading interferences [10], reduce mismatch losses in arrays [8], and results in a higher fill-factor compared to other arrays configuration [9-10].

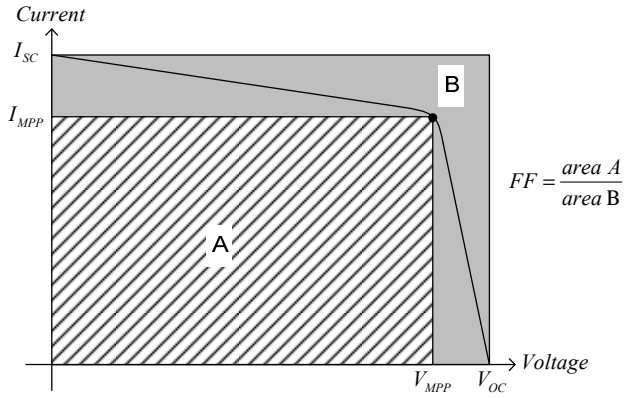

Fig. 2 Graphical explanation of Fill-Factor.

To choose this configuration it's been simulated various scenarios with PV shading, with and without by-pass diode in each PV module and compared to each other their FF.

The simulation was made in PSIM software with SolarWord SW130 PV module data. Three configurations of 18 PV modules were set and two of them were 50% shaded. The simple series (SS) configuration was made of 18 series PV modules, and SP and TCT configuration was made of 6 parallel sets of 3 series PV modules. Sweeping the array terminals and measuring its current the V *vs* I relation was acquired and the fill-factor calculated. The resumed results of the calculated FF can be seen in Figure 3.

Because of its high fill-factor and other advantages to the others configurations the TCT configuration was chosen to be used in this work.

III. PROPOSED CONVERTER

The proposed converter is a DC-DC ZVS Phase-Shift PWM Full-Bridge, based on the topology presented in [11-12]. This power structure is widely used for power supply circuits and others applications [13-16]

This converter was chosen due to its robustness, high efficiency, low EMI, current-characteristic output and galvanic isolation.

A. Proposed power circuit

The proposed power circuit of the converter is exhibited in Figure 4.

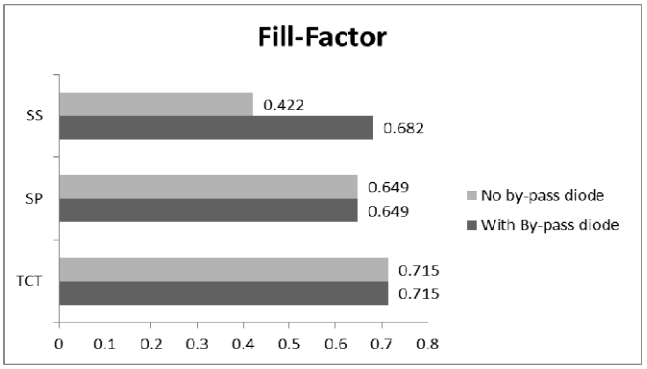

Fig. 3 Comparison of different arrays configurations under shading conditions.

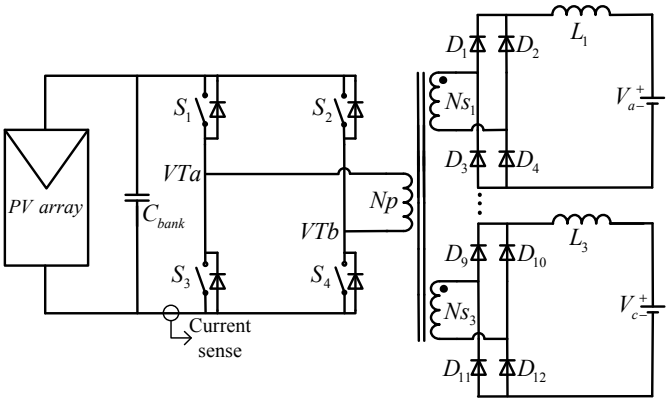

Fig. 4 Power circuit of the proposed converter. Output B is suppressed.

Due to the voltage fed characteristic of the converter and the current source characteristic of the PV array, a capacitor bank is necessary on its input. The output of the converter is connected to the 18-pulse inverter. Each input of the 18-pulse inverter has the rectified voltage of the power grid, and its mean value only depends on the power grid voltage, and then, the 18-pulse inverter is considered as three voltage sources in the output of the proposed converter.

In its primary side the leakage inductance of the transformer will be used as the resonant inductor. The resonant inductance necessary to store necessary energy to make the zero-voltage-switching in full input range is calculated with the equation (2) [12].

$$Lleak_{\min} = \frac{2}{Iin_{\min}^{\ 2}}\left(\frac{4}{3}C_{oss}\cdot Vin_{\min}^{\ 2}\right) \quad (2)$$

The minimum dead-time between the switches commands of the same lag can be determined by equation (3), based on [11].

$$t_{dead\,\min} = \sqrt{Lleak\cdot C_{oss}}\cdot\arcsin\left(\frac{Vin_{\min}}{Iin_{\min}}\sqrt{\frac{C_{oss}}{Lleak}}\right) \quad (3)$$

The resonant frequency is determined by equation (4) [14].

$$\omega_0 = \sqrt{\frac{1}{L_R\cdot 2C_{oss}}} \quad (4)$$

Because of its high current stress in the semiconductors, the capacitance in the input link must be able to handle this current stress. Polypropylene capacitors are chosen to compose the input capacitor bank. They have good electric characteristics such as low ESL, low ESR, high current handling and long life.

The minimum capacitance for the input capacitor bank is calculated by the equation (5) concerning the maximum ripple admitted.

$$C_{bank} = \frac{P_{in}}{2\cdot f_s\cdot V_{in}\cdot\Delta V_{in}} \quad (5)$$

Other design specifications were based on those presented in [11-12], [14].

IV. PEAK CURRENT MODE CONTROL

The PCMC is well known to be a fast control technique, with various highlights such as programmable current turn-off, that prevents semiconductor from driving an overcurrent, automatically balances the volt-second ratio in the primary side of the power transformer, allowing to remove DC blocking circuits and avoid core saturation [7], [17-19].

Differently from other applications of this kind of control, where to control of the output voltage is the principal objective [18-19], in this converter only the input current is controlled. The output current balance relies on the magnetic coupling of the power transformers [7], [20-21] and on the output voltage which is dependent of the power grid [1]. The 18-pulse inverter is designed to work properly under currents imbalance in its inputs, slightly affecting the current injected into the power grid [1].

The peak current-mode control is performed by the phase-shift controller UCC3895 from Texas Instruments. The block diagram is shown in Figure 5. In it is included the MPPT block which is responsible to define the current reference for the PCMC. Starting at the current sense, the sensed current must pass through a half-wave rectifier to eliminate all resonant currents that flows back to the input capacitor bank regenerating energy. After rectification, a low-pass (LP) filter removes switching noises that can compromise the signal, and then, the sensed current reaches the UCC3895, which compares the instant value to the reference. If the sensed value is higher than the reference, the command sent to the leg B of the bridge is reset. Leg B is composed of switches S2 and S4, while leg A is composed of switches S1 and S3. The commands of leg A are always complementary and 50% duty-cycle each. The commands of leg B are always complementary and 50% duty-cycle in steady-state. During transitory situations the commands of leg B can be of different duty-cycle, but it not compromises the converter.

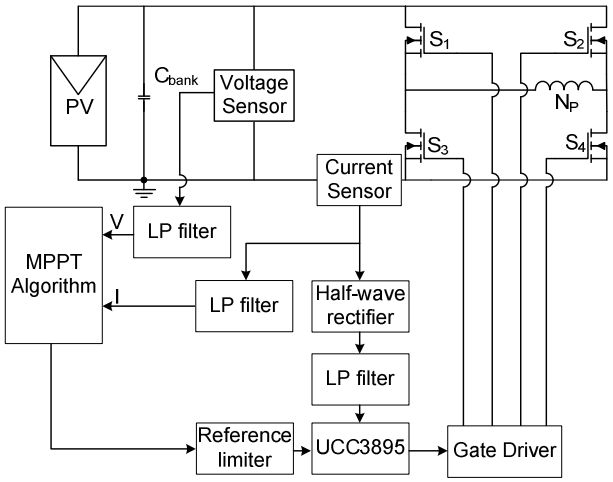

Fig. 5 Block diagram for the PCMC. Secondary side are suppressed.

V. DESIGN CONSIDERATIONS

Others electrics characteristics regarding the power converter design are resumed in Table II.

TABLE II
Electric specification of the power converter

Characteristic	Value	Nomenclature
Duty-cycle loss	0.095	ΔD
Primary-side rms current	85.1A	Ip_{rms}
Primary side turns	3	N_P
Secondary side turns	30	N_S

The value of leakage inductance required for the minimum energy to occur ZVS in full input range is calculated by equation (2). The MOSFETs switches used in this prototype are two parallel connected IRFB4110, resulting in 1.6nF of C_{oss}. The minimum leakage inductance value calculated is 78nH. Other parameter take in account in the commutating inductance is the effective duty-cycle, which is directly influenced by the commutating inductance. To maintain the duty-cycle loss (ΔD) of 0.095 in nominal condition, the maximum commutating inductance is calculated by the equation (6).

$$Lleak_{\max} = \frac{\Delta D \cdot V_{in}}{4 \cdot fs \cdot Ip_{rms}} \quad (6)$$

Using the values presented in Tables I and II, the result of equation (6) is 208 nH.

After proper design and implementation, the measured primary side leakage inductance is 189 nH, which provides ZVS in entire input range, and a duty-cycle loss lower than the specified, causing no harm to the converter.

The dead-time required for ZVS in minimum input aspects is 7ns according to equation (3). The leg dead-time was set to 250ns to prevent leg short-circuit and massive loss.

The calculated RMS current in the capacitor is above 74A. Each capacitor can handle a pulse of 100A peak. The minimum calculated capacitance for a 10% ripple of the maximum input voltage is 62µF. To reduce the voltage ripple and the current stress in each capacitor, ten 10µF capacitors were associated to form the input capacitor bank.

In secondary side, power elements were designed to achieve robustness and low current ripple as demanded from the 18-pulse inverter. The output rectifier is formed by HFA06TB120 diodes, and 2.1mH inductor for current filtering.

VI. SIMULATION RESULTS

Simulation results are provided to evaluate the converter performance, complementing the experimental results. The simulations were made in PSIM software, including the PV-array model and the line-commutated 18-pulse inverter.

Figure 6 presents the voltage and current of the proposed converter at maximum power point of the PV array. A small ripple value can be observed at low frequency, 360Hz, that is reflected from the output currents. The output current is shown in Figure 7. The low frequency ripple is predominant due the input voltage of the 18-pulse inverter. This occurs since the current in the output inductors is not controlled and depends on its applied voltage. According to Figure 8, each input voltage of the 18-pulse inverter has a 120Hz pulsed voltage, which determines the output current shape of the converter.

The 18-pulse delivered current to the power grid is shown in Figure 9. The injected current has harmonics components higher than the accepted, according to [22], the THD limit is 5%, and the measured value is 12%. A small passive harmonic filter is able to reduce the THD to the limits imposed by [22].

VII. EXPERIMENTAL RESULTS

All experimental results obtained are exclusively from the DC-DC converter and are preliminary results but ensure the proper design of the converter.

Zero-voltage-switching can be seen in each switch through its gate-source and drain-source voltages. If the gate-source command is applied when the drain-source voltage is zero, the switching is soft, otherwise, is a hard-switching.

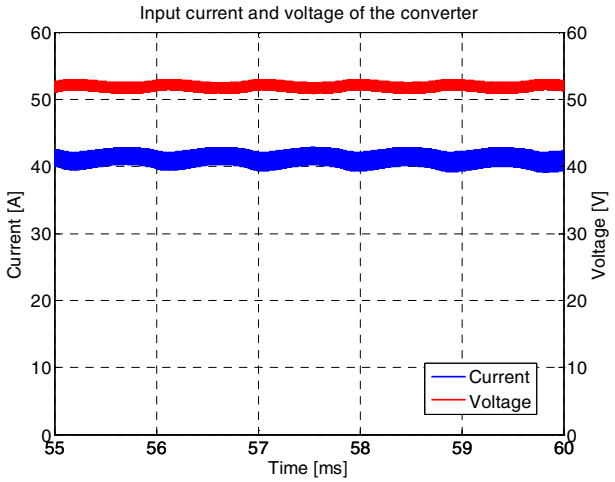

Fig. 6 Input voltage and current at PV array MPP.

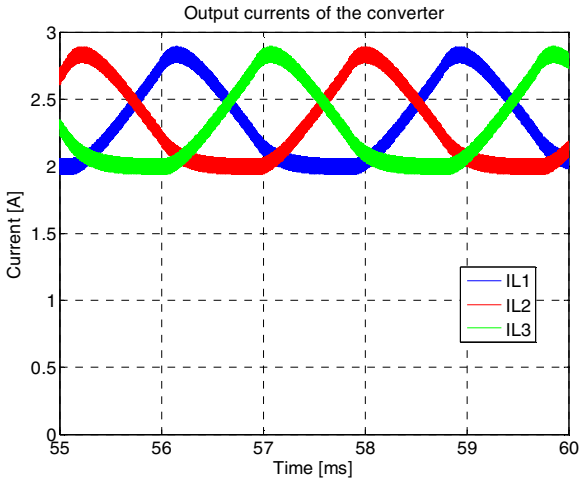

Fig. 7 Output current of the proposed converter, connected to the 18-pulse inverter.

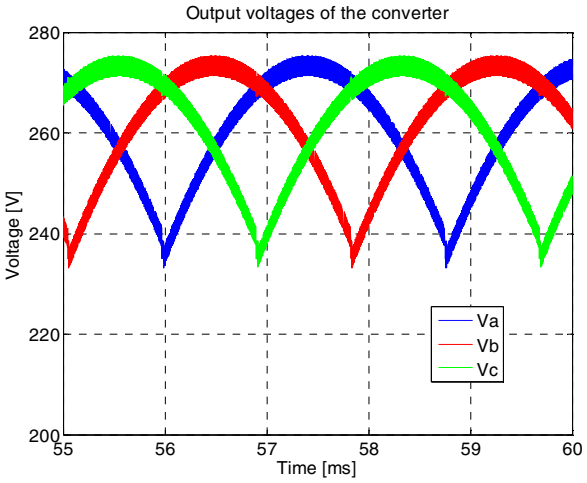

Fig. 8 Input voltages of the 18-pulse inverter.

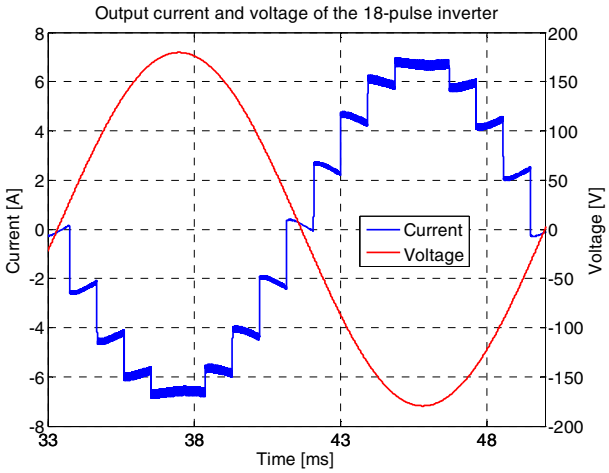

Fig. 9 Output current and voltage of the 18-pulse inverter.

A DC power source was used instead of the PV array and a resistive load was used in place of the 18-pulse inverter.

Due to power limitations of the used DC power source, the following results were obtained at reduced input voltage, 29V and input current value close to the nominal, 40A. Figure 10 shows the gate-source voltage (VGS) and the drain-source voltage (VDS) of S1, that is one of the two switches of the critical leg. It can be seen that a ZVS occurs because the gate command is sent when the VDS value is low. The ZVS can be seen in all others switches at this condition.

At the minimum input specifications, a minimum load was set at the output to evaluate the performance of the converter. Figure 11 shows the VGS and VDS of S1 with an input of 36V and 15A. A hard-switch is occurring in this leg due its critical condition. A smaller dead-time could turn this switching into soft-switching, but the loss in these switches is negligible. The non-critical leg remains ZVS at the same condition, grating low loss at minimum input specification.

The input and output currents can be seen at Figure 12. They present no low-frequency ripple as simulated results because the used load at experimental setup is resistive instead the 18-pulse inverter. All three output currents have approximately the same mean value as it should.

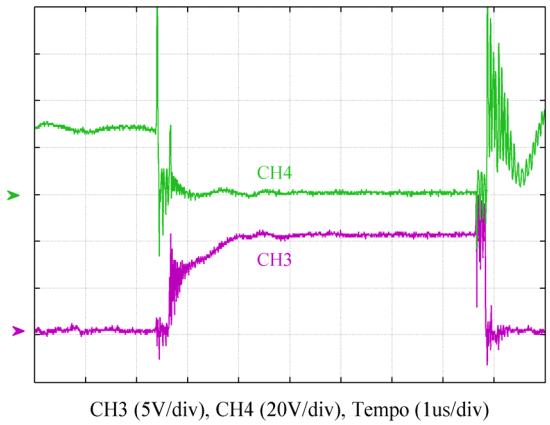

Fig. 10 VGS (CH3) and VDS (CH4) of one switch of crictical leg.

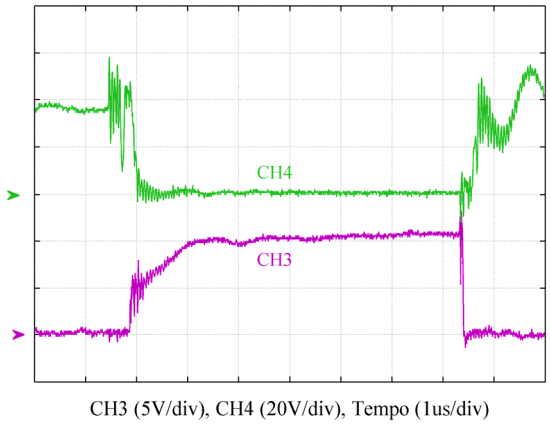

Fig. 11 VGS and VDS of S1 at minimum input specification.

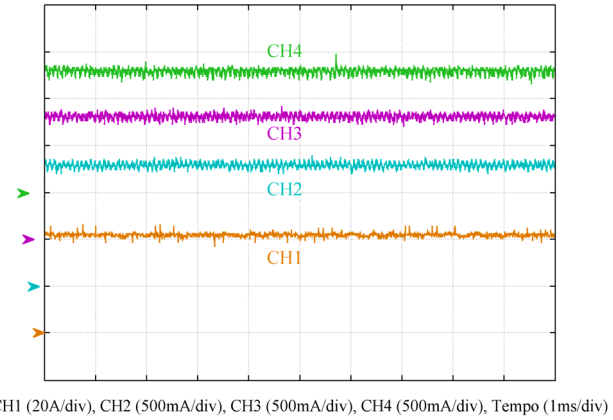

Fig. 12 Input current, and three output currents.

VIII. CONCLUSIONS

In this paper was proposed an application of a DC-DC full-bridge converter with ZVS for photovoltaic applications. The design of the converter allows a low-voltage PV array connection, improving shading robustness and reducing mismatches loss. A current-mode control is implemented in primary-side of the transformer offering overcurrent protection and removing DC-blocking circuit. The DC

current source required by the 18-pulse inverter is provided by the current characteristic of the proposed converter.

Preliminary experimental results show the proper functioning of the converter, with ZVS as proposed. Improvements in secondary-side of the power circuit are required to provide better performance of the converter and proper circuit control in primary-side. Simulation results complement the experimental results with the expected behavior and the connection to the 18-pulse inverter.

The proposed system has potential, with high-efficiency and robustness, presenting some faults, as the injected current THD, which can be mitigated with an external circuit as passive harmonic filters.

For future works, is proposed some adjustments in the DC-DC secondary-side converter and full system experimental results.

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