

A Voltage Regulator for Power Quality Improvement in Low-Voltage Distribution Grids

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Abstract—This paper presents a voltage-controlled distribution static synchronous compensator (DSTATCOM)-based voltage regulator for low-voltage distribution grids. The voltage regulator is designed to temporarily meet the grid code, postponing unplanned investments while a definitive solution could be planned to solve regulation issues. The power stage is composed of a three-phase four-wire voltage-source inverter and a second-order low-pass filter. The control strategy has three output voltage loops with active damping and two dc bus voltage loops. In addition, two loops are included to the proposed control strategy: the concept of minimum power point tracking (mPPT) and the frequency loop. The mPPT allows the voltage regulator to operate at the minimum power point, avoiding the circulation of unnecessary reactive compensation. The frequency loop allows the voltage regulator to be independent of the grid voltage information, especially the grid angle, using only the information available at the point-of-common coupling. Experimental results show the regulation capacity, the features of the mPPT algorithm for linear and nonlinear loads, and the frequency stability.

Index Terms—DSTATCOM, frequency compensation, minimum power point (mPP) tracker, power quality, static VAR compensators, voltage control, voltage regulation.

I. INTRODUCTION

CUSTOMERS connected at the end of low-voltage distribution grids may experience poor voltage regulation. According to Brazilian grid code [1], power companies have constrained deadlines (15 to 90 days) to restore the voltage levels at the point-of-common coupling (PCC) if the voltages are outside the admissible levels. The time needed for permanent solutions, like grid restructuring or capacitor banks installation, to be operational may exceed the deadlines. In the case of failure to meet the deadlines, the power company has to refund every customer in the distribution grid during the time that the poor voltage regulation persisted [1].

Aiming to prevent refunds, a voltage regulator can be utilized as a temporary solution. The voltage regulator must have fast voltage regulation, reduced weight, and easy installation [2], [3].

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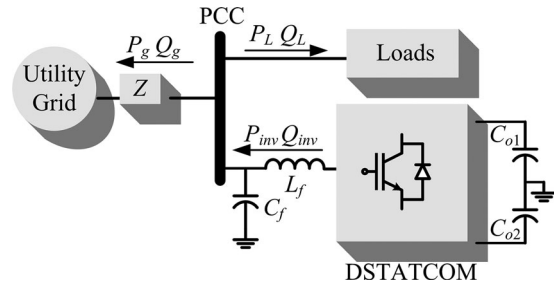


Fig. 1. Low-voltage distribution grid under analysis with the voltage regulator.

Using the proposed solution, the grid power quality is reestablished and the PCC voltage is restored in a short period of time. In the meantime, the permanent solution can be planned and installed in an appropriate time frame. Once the definite solution is implemented, the voltage regulator can be disconnected from the grid and connected to another grid with similar problems.

In real applications, poor voltage regulation occurs when the PCC is far from the main grid transformer and the distance between the PCC and the transformer can easily be further than 100 m. Access to grid voltage information can be difficult to obtain.

To meet the voltage regulation requirement, a voltage-controlled DSTATCOM-based voltage regulator is proposed with shunt connection to PCC [2]–[9], as shown in Fig. 1. The shunt connection avoids power supply interruption while the voltage regulator is installed or disconnected. The proposed DSTATCOM allows the power company to postpone investments and enhances the flexibility of grid management.

Voltage-controlled DSTATCOM can maintain the PCC voltages balanced even under grid or load unbalances. The PCC voltage is directly controlled by the DSTATCOM and sudden load changes have no significant impact in the PCC voltage waveforms. Moreover, the voltage-controlled DSTATCOM decouples the grid and the loads, serving as a low-impedance path for harmonic distortions due the voltage-source behavior. Current harmonic distortions from the loads have small impact in the grid and vice versa. The grid current quality, therefore, is exclusively given by the grid voltage quality.

According to [3], angular position reference is required for the voltage-controlled DSTATCOM to work properly. Before the DSTATCOM starts its operation, synchronization circuits generate the angular position to the voltage regulator [8]–[10]. Once the operation begins, the voltage-controlled voltage

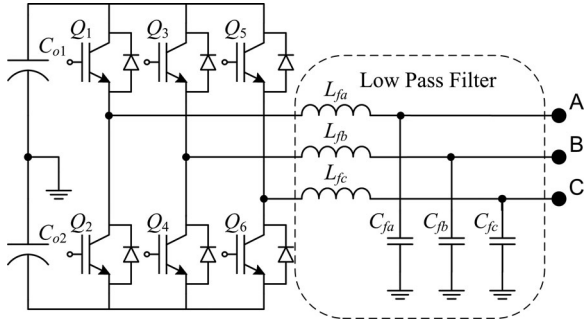


Fig. 2. Three-phase four-wire VSI with LC low-pass filter.

regulator replaces the PCC voltage and the grid voltage frequency and angle are no longer available. PCC voltage frequency and angle are then determined by the voltage regulator. For a real application, due to the distance between the transformer and the PCC, only the PCC voltage should be measured to compose the voltage reference of the DSTATCOM.

In past years, the PCC voltage amplitude (V_{PCC}) for reactive compensation methods was usually adopted as the nominal grid voltage [2], [5], i.e., 1.00 p.u. However, Brazilian grid code determines a maximum (1.05 p.u.) and a minimum (0.92 p.u.) voltage amplitude for low-voltage distribution grids [1]. The PCC amplitude can be viewed as a degree of freedom and the processed power can be reduced with a suitable control loop.

In this effort, Kumar and Mishra [8] propose a new method to determine the suitable PCC terminal voltage for reduction of the DSTATCOM power rating. The method is formulated according to the desired source current, aiming to achieve the unity power factor at the grid. However, this method requires information about the source current, grid resistance, and reactance. In [9], Kumar and Mishra propose another method to determine suitable V_{PCC} using the positive-sequence components of the load current to compute the PCC voltage. In both cases, additional information is required, increasing the process complexity, number of sensors, and the cost of the solution. To maintain the easy installation feature and reasonable costs, it is convenient to set the PCC voltage, in which the processed power is minimal, without monitoring any load or grid information and using only internal signals of the DSTATCOM, such as the PCC voltages and DSTATCOM output currents.

This paper presents a voltage-controlled DSTATCOM-based voltage regulator for low-voltage distribution grids, using a three-phase four-wire voltage-source inverter (VSI) with an LC low-pass output filter, as shown in Fig. 2. Operation principles of the voltage-controlled DSTATCOM and the control strategy are presented. Additionally, two loops are included to the proposed control strategy: the concept of minimum power point tracking (mPPT) [6] and the frequency loop [11]. The mPPT avoids unnecessary reactive compensation, increasing the compensation capability. The frequency loop overcomes the practical difficulty of synchronization by correcting the frequency of the voltage reference.

This paper proposes the combination of both loops, providing to the power company a solution for the poor voltage regulation in real distribution grids with superior PCC voltage quality. Experimental results confirm the effectiveness of the voltage regulator and the features of both loops, separately and simultaneously.

II. POWER FLOW ANALYSIS OF THE VOLTAGE-CONTROLLED DSTATCOM CONNECTED TO THE GRID

Voltage-controlled DSTATCOMs replace the PCC with three balanced voltage waveforms, adjusting their phase as the load and the dc bus require [2].

The active and reactive power flow between two bus bars can be expressed by

$$P_g = \frac{V_g^2}{Z} \cos(\phi) - \frac{V_g V_{PCC}}{Z} \cos(\phi) \cos(\theta) + \frac{V_g V_{PCC}}{Z} \sin(\phi) \sin(\theta) \quad (1)$$

$$Q_g = \frac{V_g^2}{Z} \sin(\phi) - \frac{V_g V_{PCC}}{Z} \sin(\phi) \cos(\theta) - \frac{V_g V_{PCC}}{Z} \cos(\phi) \sin(\theta) \quad (2)$$

where P_g and Q_g are, respectively, the grid active and reactive power, V_{PCC} is the PCC rms voltage, V_g is the grid rms voltage, Z and ϕ represent the grid impedance modulus and angle, respectively, and θ represents the displacement angle of the PCC voltage.

An ideal DSTATCOM processes only reactive power. Therefore, the active power balance can be written as

$$P_g + P_L = 0 \quad (3)$$

where P_L is the load active power. Replacing (3) in (1)

$$\frac{V_g^2}{Z} \cos(\phi) - \frac{V_g V_{PCC}}{Z} \cos(\phi) \cos(\theta) + \frac{V_g V_{PCC}}{Z} \sin(\phi) \sin(\theta) + P_L = 0 \quad (4)$$

the relationship between θ and P_L is obtained. On the other hand, the reactive power balance can be written as

$$Q_{inv} = Q_L + Q_g \quad (5)$$

where Q_{inv} is the DSTATCOM processed reactive power and Q_L is the load reactive power. Replacing (5) in (2), one can get

$$Q_{inv} = Q_L + \frac{V_g^2}{Z} \sin(\phi) - \frac{V_g V_{PCC}}{Z} \sin(\phi) \cos(\theta) - \frac{V_g V_{PCC}}{Z} \cos(\phi) \sin(\theta). \quad (6)$$

The apparent power can be derived as

$$S_{inv} = \sqrt{P_{inv}^2 + Q_{inv}^2}. \quad (7)$$

From (7), it is derived that S_{inv} is a function of V_{PCC} . To verify the impact of V_{PCC} in S_{inv} , θ must be computed first. Fig. 3 presents the numerical solution of (4) for a 0.8 lagging power

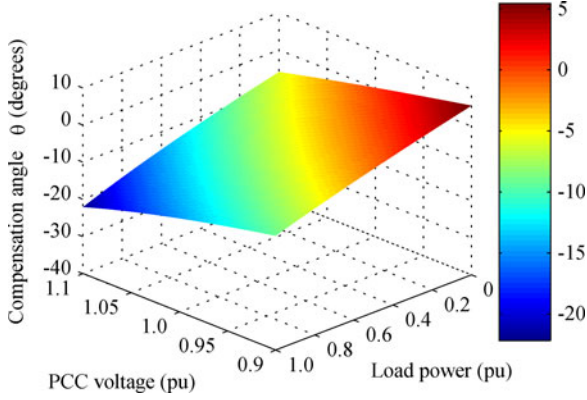


Fig. 3. Compensation angle θ as a function of PCC voltage and load power ($Z = 0.2$ p.u., $\phi = 45^\circ$, and $V_g = 1$ p.u.).

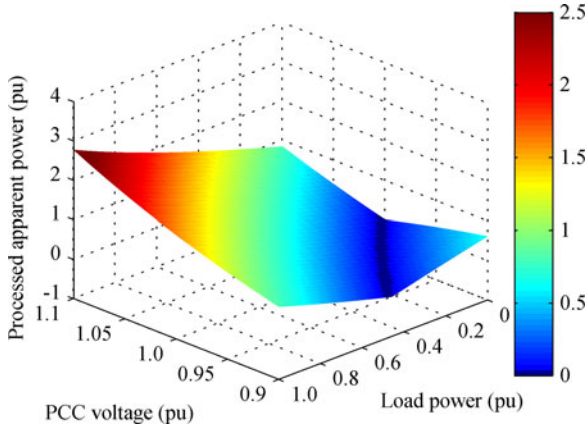


Fig. 4. Processed apparent power as a function of PCC voltage and load power ($Z = 0.2$ p.u., $\phi = 45^\circ$, and $V_g = 1$ p.u.).

factor load and for a given grid impedance and voltage (considered as $Z = 0.2$ p.u.; $\phi = 45^\circ$; $V_g = 1$ p.u.). The values of θ are replaced in (7) and the numerical solution is presented in Fig. 4. The operating points in which the apparent power is zero are shaded in Fig. 4.

For each combination of Z , ϕ , V_g , and load, (7) produces null solutions at different values of V_{PCC} . Therefore, V_{PCC} must be determined by a control system that does not need grid and load information, which is one proposal of this study.

The numerical solution of (7) helps in the power rating design of the voltage regulator. For this paper, the DSTATCOM power rating was chosen as 1.0 p.u., the nominal load power. Taking into account the PCC voltage reduction performed by the mPPT algorithm, Fig. 4 shows the DSTATCOM is able to compensate 1.0-p.u. load power with PCC voltage equal to 0.93 p.u.

III. MINIMUM POWER POINT (MPP) TRACKER

The voltage amplitude to be regulated at PCC changes the power flow between the grid, load, and DSTATCOM, as demonstrated in Section II. Suitable V_{PCC} makes the processed apparent power be minimal.

When the V_{PCC} is between the desired voltage limits, the mPPT minimizes the converter apparent power and no reactive

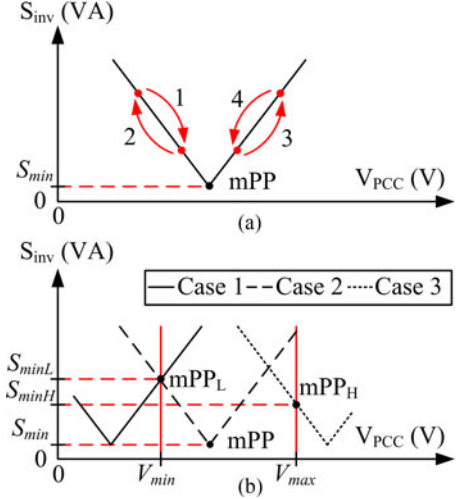


Fig. 5. (a) P&O-based mPPT derivation. (b) Example of the mPPT algorithm with voltage constraints.

power at the grid frequency is processed. Apparent power minimization means current minimization, which lowers the losses and extends the equipment life cycle.

For the mPPT analysis, apparent power is chosen to be minimized instead of reactive power due to: 1) active power in DSTATCOMs is a small fraction of the apparent power; 2) the harmonic currents from the grid and load are also processed; 3) the converter power rating and the losses are given by the apparent power; and 4) apparent power is easier to calculate in comparison to extract the reactive power at the grid frequency from distorted current waveforms.

A. Perturb-and-Observe (P&O)-Based mPPT Algorithm

The reduction of voltage regulator apparent power can be performed by tracking algorithms. An example of tracking algorithm is the maximum power point tracker (MPPT), which is widely used in photovoltaic (PV) systems.

Among several MPPT algorithms, the P&O method was chosen to compose the mPPT algorithm due to its simplicity, low computational effort, and a small number of sensors, although it has slow transient response and operates around a maximum power point (MPP) [12]–[19], which can be a local or a global MPP [20], [21].

Two parameters must be set to the P&O algorithm: perturbation amplitude and sample time. The perturbation amplitude defines the convergence time to reach the MPP and the amplitude of the oscillations in steady state [14]. The sample period must be greater than the response time of the system to avoid instabilities [12].

One interesting feature of the P&O method is its independence of PV arrays parameters [14], [18]. This feature makes the P&O not restricted to PV systems.

The P&O-based mPPT algorithm presents the same features of the P&O algorithm applied to MPPT, but is designed to achieve the mPP instead of MPP [6].

TABLE I
SUMMARY OF THE FEATURES OF THE MPPT ALGORITHM

Apparent Power	Voltage Amplitude	Marker	mPTT Action
increasing	increasing	3	decrease
	decreasing	2	increase
decreasing	increasing	1	increase
	decreasing	4	decrease

The mPPT can be derived analyzing Fig. 5(a). The marker 1 represents an increase of V_{PCC} and the marker 4 represents a decrease of V_{PCC} which leads to reduction of the S_{inv} . In these cases, the next perturbation will conserve the perturbation signal (positive for marker 1 and negative for marker 4) and the mPPT will converge to the mPP. On the other hand, the marker 2 represents a decrease of V_{PCC} and the marker 3 represents an increase of V_{PCC} diverging from mPP. Therefore, the direction of the next perturbation must be positive for marker 2 and negative for marker 3.

The mPPT algorithm is summarized in Table I. Comparing the perturbation logic of the P&O mPPT with the conventional P&O MPPT algorithm, one can conclude that the P&O-based mPPT can be obtained by simply changing the perturbation signal of the conventional P&O MPPT.

The processed power at the mPP was intentionally considered as S_{min} , the minimal power to be processed. DSTATCOM losses and harmonic distortions contributions to the apparent power cannot be minimized to zero.

B. Amplitude Loop

The amplitude loop is composed of the P&O-based mPPT algorithm and has voltage constraints to meet, which are imposed by the Brazilian grid code [1]. The voltage constraints are not considered in [6] and directly affect the apparent processed power.

There are three different cases when voltage constraints are present as depicted in Fig. 5(b). In case 1, S_{min} requires a V_{PCC} below the minimum allowable PCC voltage (V_{min}). The mPPT goes toward the mPP, but V_{PCC} cannot be lower than V_{min} . V_{PCC} is kept at V_{min} and the voltage regulator supplies reactive power to maintain the V_{PCC} regulated. Therefore, the mPP in case 1 will be at mPP_L and the processed power is represented by S_{minL} . The case 3 shows a similar outcome to case 1 with V_{PCC} kept at the maximum allowable PCC voltage (V_{max}). The converter operates at mPP_H and process reactive power equal to S_{minH} .

In case 2, the mPP occurs with V_{PCC} between V_{max} and V_{min} . The mPPT tracks the mPP and the converter process S_{min} , the active power to compensate the losses and the harmonic distortion from the grid and load.

IV. FREQUENCY LOOP

The grid frequency has small frequencies deviations around the nominal value and many loads can operate under such deviations. However, voltage-controlled DSTATCOM

synthesizes the PCC voltage with a constant frequency. Large differences between the grid and PCC frequencies, associated with long frequency deviations, may lead to disconnection of the DSTATCOM.

A. Grid Frequency Variation and the Total DC Bus Controller

The PCC voltage reference can be written as

$$v_{ref} = V_{PCC} \sin \left(2\pi f_{ref} t - \theta - \frac{2\pi}{3} x \right) + V_{PCC,dc}, x = 0, 1, 2 \quad (8)$$

with $x = 0, 1, 2$ representing a -, b - and c - phases, respectively. For a given constant grid frequency (f_g), one can assume that the reference frequency (f_{ref}) is equal to the PCC frequency (f_{PCC}) and θ is also constant. As f_g varies, the total dc bus voltage controller ensures f_{PCC} is equal to f_g , through a time-variant control output. The compensation angle can be decomposed in a constant (Θ) and a time-variant ($\theta(t)$) component, according to

$$\theta = \Theta + \theta(t). \quad (9)$$

Replacing (9) in (8), the voltage reference is rewritten as

$$v_{ref} = V_{PCC} \sin \left(2\pi f_{ref} t - \theta(t) - \Theta - \frac{2\pi}{3} x \right) + V_{PCC,dc}. \quad (10)$$

The PCC frequency is the time-variant term in (10):

$$f_{PCC} = f_{ref} - \frac{\theta(t)}{2\pi}. \quad (11)$$

B. Grid Frequency Variation Impacts

Differences between f_g and f_{PCC} have two impacts on the voltage regulator: dc bus voltage steady-state error and nonconstant total dc bus voltage controller output [22].

The steady-state error depends on the total dc bus controller design and frequency perturbation magnitude. If the steady-state error is positive, dc bus overvoltage can be higher than the capacitors' rated voltage. If negative, the modulation index can be close to the unity, reducing the PCC voltage quality.

When the controller is implemented in analog circuits, the nonconstant control output must be constrained to the analog voltage limits. Once the compensation angle (θ) reaches the constraints, the angle is kept to the limit value. Therefore, the total dc bus voltage controller is no longer able to regulate the total dc bus voltage. The voltage regulator shuts down, leading to severe consequences to PCC customers and power company.

C. Grid Frequency Variation Impacts

The proposed method is based on a feature of the total dc bus controller: f_{PCC} is equal to f_g due the nonconstant output of the total dc bus controller. By measuring f_{PCC} , f_g can be obtained. Periodically updating f_{ref} with f_{PCC} , the frequency loop brings $\theta(t)$ to zero in (11) at each sampling time. Counting the time between each PCC voltage zero cross, the f_{PCC} is fed into the reference generator.

To verify the frequency loop features, f_g is changed by a 0.1 Hz step at 0.2 s. in Fig. 6. The f_{PCC} is equal to f_g , regardless

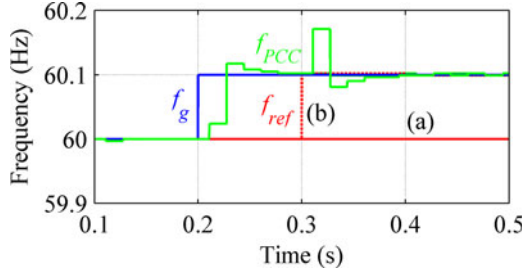


Fig. 6. Relationship between the grid, PCC, and reference frequencies: (a) Without and (b) with the frequency compensation.

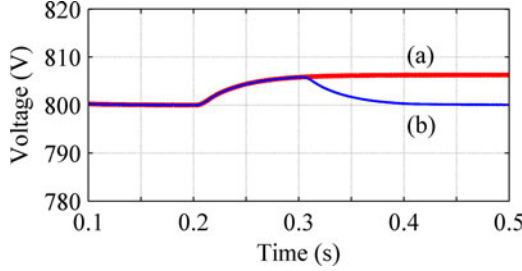


Fig. 7. Total dc bus voltage during the grid frequency variation: (a) Without and (b) with the frequency compensation.

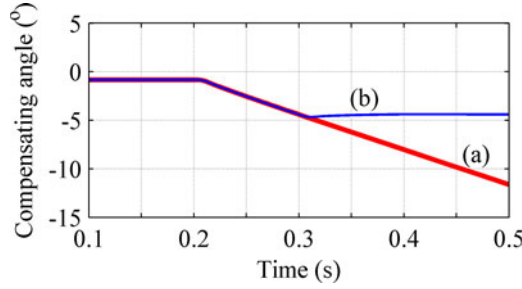


Fig. 8. Compensation angle during the grid frequency variation: (a) Without and (b) with the frequency compensation.

of the f_{ref} . The frequency loop updates f_{ref} with f_{PCC} at 0.3 s and the three frequencies have the same value, as shown in Fig. 6(b).

The effect of the grid frequency step on the total dc bus voltage can be seen in Fig. 7(a). The dc bus voltage has low steady-state error (around 6 V) because of a large total dc bus voltage controller bandwidth. With the f_{ref} update, Fig. 7(b), the total voltage returns to nominal voltage.

After the frequency step, the total voltage controller has a slope output. Without f_{ref} update, Fig. 8(a), the compensation angle decreases indefinitely, whereas with the frequency loop, the compensation angle is constant, as shown in Fig. 8(b). However, the compensation angle does not return to the previous value. Errors between f_{ref} and f_{PCC} are accumulated in the compensation angle and the controller output may reach its limits. If imminent, a protective routine is activated, which adds a constant factor to f_{ref} , bringing the compensation angle back to 0 radians. After that the frequency loop returns to normal operation.

TABLE II
VOLTAGE REGULATOR PARAMETERS

Nominal Power	S_o	30 kVA
Nominal dc bus voltage	V_o	800 V
Grid voltage	V_g	220 V
Grid frequency	f_g	60 Hz
Switching frequency	f_s	20 kHz
DC bus capacitance	C_{oeq}	3,500 μ F
Output filter inductance	L_f	560 μ H
Output filter capacitance	C_f	47 μ F
Grid resistance	R_g	0.685 Ω
Grid inductance	L_g	1.82 mH

V. CONTROL STRATEGY

The control strategy aims to synthesize three balanced voltage waveforms at PCC with adequate amplitude, low total harmonic distortion (THD), and also regulate the voltage of the dc bus capacitors. Therefore, the control strategy has three output voltage loops, one total and one differential dc bus voltage loop. The aforementioned controllers were designed with the parameters presented in Table II and evaluated for a range of the grid impedance (0.1 to 10 of R_g and L_g) through frequency response analysis. In this range, the designed controllers work properly.

Additionally, this paper includes two loops: a loop responsible for the PCC voltage amplitude and another one responsible for mitigating the grid frequency effect on the voltage regulator. Fig. 9 shows the complete control block diagram with the amplitude and frequency loops.

A. Output Voltage Loop

The inputs of the output voltage loop are three voltage references (v_{ref}). The voltage references are composed of the dc bus controllers output, the mPPT, and the frequency loop, as depicted in Fig. 9. To achieve adequate synthesis of the voltage references, the output voltage loop must have fast dynamic response. The output controller is a PID controller.

The simplified output voltage loop block diagram can be seen in Fig. 10. The output voltage loop has active damping controllers to enhance the stability of the voltage regulator against grid impedance variations [6].

B. Grid Frequency Variation and the Total DC Bus Controller

The DSTATCOM operation causes power losses in the power converter as a result of semiconductor switching. The losses diminish the total dc bus voltage (v_o). As seen in Section II, the displacement angle θ determines the active power flow at the PCC. Therefore, the total dc bus loop compares v_o to the reference v_o^* and, through a PI plus pole controller, set a suitable θ to drain active power from the grid and reestablish the power balance between the grid, the loads and the DSTATCOM.

The DSTATCOM is composed of three-phase four-wire VSI and the voltage balance at the split capacitors is required. The difference between the split capacitor voltages (v_d) is compared to the reference (v_d^*) and a PI plus pole contributes to the reference generator with a small dc component ($V_{PCC,dc}$). This dc

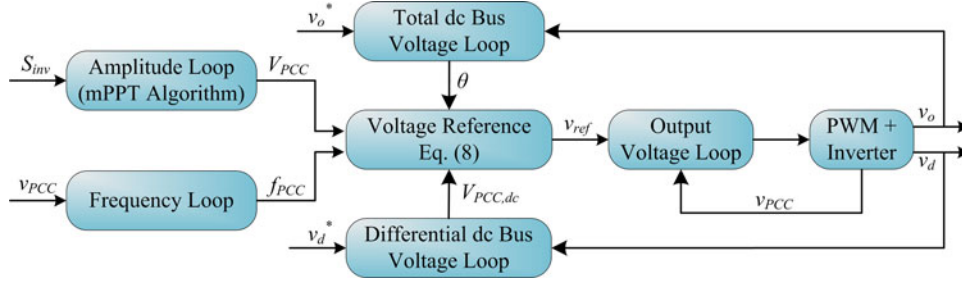


Fig. 9. Proposed control strategy including amplitude and frequency loops.

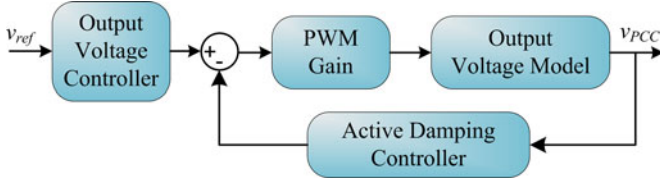


Fig. 10. Output voltage loop block diagram.

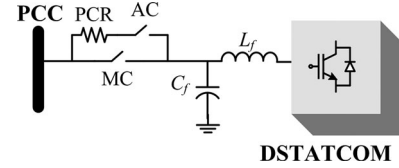


Fig. 12. Single-phase representation of the voltage regulator initialization circuits.

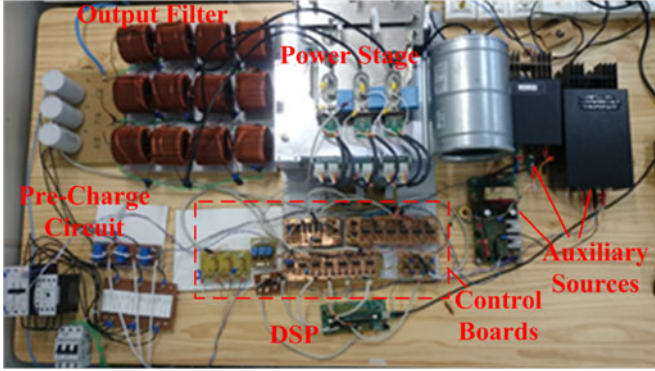


Fig. 11. Voltage regulator experimental setup.

component charges one capacitor more than the other and the voltage balance can be achieved.

VI. EXPERIMENTAL RESULTS

In order to verify the voltage regulation capability, the mPPT, and the frequency loop, a prototype was implemented, depicted in Fig. 11, using the parameters given in Table II. At first, this paper presents experimental results for the mPPT, which were not presented in [6], and the frequency loop separately. At the end of this section, the simultaneous operation of both proposed loops is presented, enhancing the results obtained in [6] and [11].

A. Prototype Implementation and Initialization

The prototype uses analog control to compose the output and the dc bus voltage loops. The controllers are based on PI and PID controllers and designed via frequency response [6]. The θ and $V_{PCC,dc}$ are sampled by the digital signal processor (DSP) at f_s via analog-to-digital converters. On the other hand, the mPPT algorithm and the frequency loop are implemented in the DSP TMS320F28335.

The apparent power is calculated using moving average filters (MAF) to obtain the rms current of the DSTATCOM. The MAFs have 80 samples for each period of the grid. The PCC voltage amplitude (V_{PCC}) is intrinsic to the DSP and is set by the mPPT. The apparent power is given by the product of V_{PCC} and the calculated rms current. The sum of the three apparent powers is applied to the mPPT. The voltage step of mPPT was set to 0.2 V with a period of 0.1667 s.

For the f_{PCC} measurement, the PCC voltage waveform is compared to zero and the signal period is counted with the enhanced capture module of the DSP every 500 ms. Multiple zero crossings are filtered in order to improve the measure accuracy.

After the update of V_{PCC} and f_{ref} , the DSP generates the voltage references, according to Fig. 9. The output voltage loop receives the voltage references through digital-to-analog circuits.

The DSP also protects the DSTATCOM against dc bus over-voltage and overload, and performs routines as precharging and synchronization.

The initialization procedure is depicted in Fig. 12. At the time t_0 the auxiliary contactor (AC) closes and inserts the precharge resistors (PCR) in series with the DSTATCOM while the pulse width modulation (PWM) is maintained disabled. The dc bus charges through the switches diodes, as shown in Fig. 13. Meanwhile, the phase-locked loop circuit synchronizes the voltage references with the PCC voltages.

At the time t_1 , the main contactor short circuits the PCR and the PWM is enabled. The dc bus voltage reference rises with a slow slope to avoid overshoot. At the time t_2 , AC is opened.

B. Linear Loads

The linear loads are composed of 10.4-kW three-phase resistive loads. The PCC voltage amplitude without compensation is 212 V according to Fig. 14. One can see that the PCC voltages

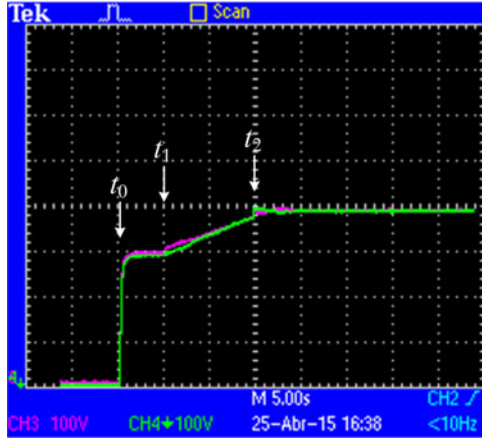


Fig. 13. DC bus voltages during the DSTATCOM initialization.

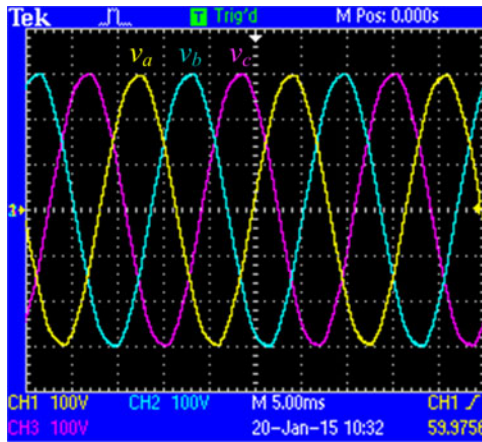


Fig. 14. PCC voltages without compensation for linear loads.

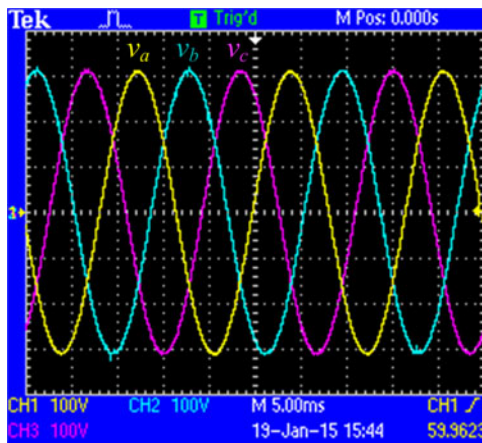


Fig. 15. PCC voltages with compensation for linear loads.

contain some harmonic distortion inherent to low-voltage distribution grids. The compensated PCC voltage was arbitrarily chosen as 220 V. The PCC voltages are regulated with low THD (0.2%), as shown in Fig. 15.

The compensation currents have different rms values for each phase, highlighting the natural unbalance of the low-voltage grids. The harmonic distortion present in the grid voltage is

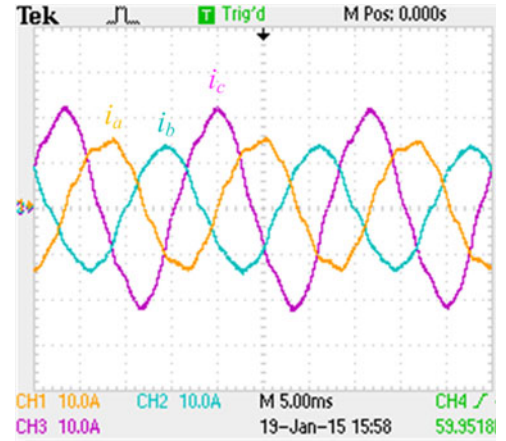


Fig. 16. Voltage regulator currents for linear loads.

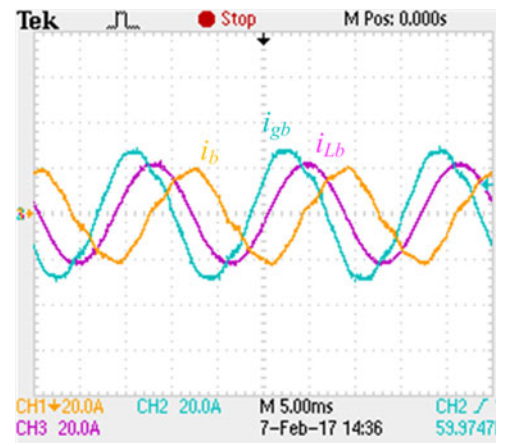


Fig. 17. Grid, load, and voltage regulator currents for linear loads.

compensated by the regulator. Fig. 16 presents the compensation current waveforms.

The quality of the b -phase grid current (i_{gb}) for linear loads is shown in Fig. 17. The voltage regulator supplies the load with low-THD voltages, as seen by the load current (i_{Lb}). The harmonic content in i_{gb} is given by the grid voltage distortions.

C. Nonlinear Loads

The considered nonlinear loads are three 2-kVA single-phase rectifiers with a capacitive filter, one in each phase added to 5.2-kW three-phase resistive loads. The PCC voltage amplitude without compensation is 203 V with 6.4% THD, as shown in Fig. 18. The compensated PCC voltage is depicted in Fig. 19, having three regulated and sinusoidal waveforms with 0.6% THD.

The compensation currents contain the fundamental frequency for the reactive compensation and all the harmonic distortion from the nonlinear loads, as seen in Fig. 20.

The b -phase grid current (i_{gb}) waveform for nonlinear load is shown in Fig. 21. The voltage regulator absorbs the harmonic content from the load current (i_{Lb}) leaving i_{gb} free of load harmonic distortions. Comparing i_{gb} from Figs. 17 and 21, one

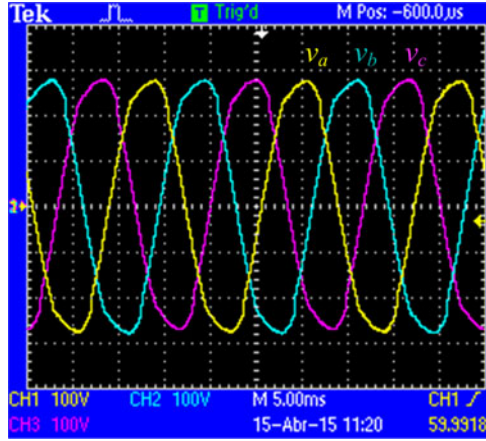


Fig. 18. PCC voltages without compensation for nonlinear loads.

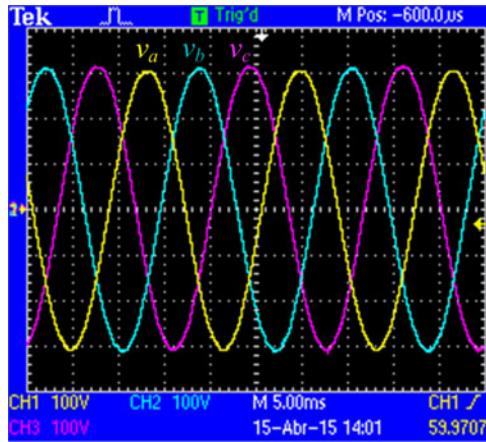


Fig. 19. PCC voltages with compensation for nonlinear loads.

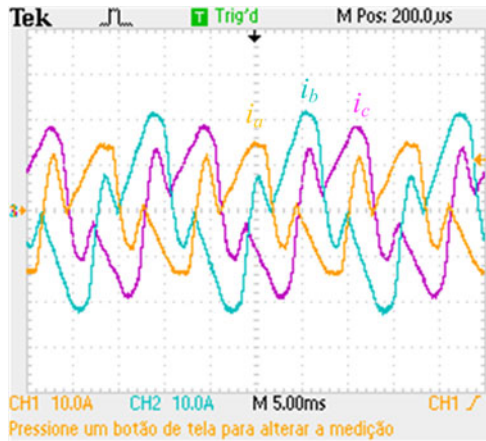


Fig. 20. Voltage regulator currents for nonlinear loads.

can notice the grid current waveforms present similar distortions from the grid voltage.

D. Minimum Power Point Tracking

The behavior of the voltage amplitude loop for linear loads is depicted in Fig. 22. The initial value for the voltage amplitude is 1.00 p.u. (220 V) and decreases to 0.9545 p.u. (210 V).

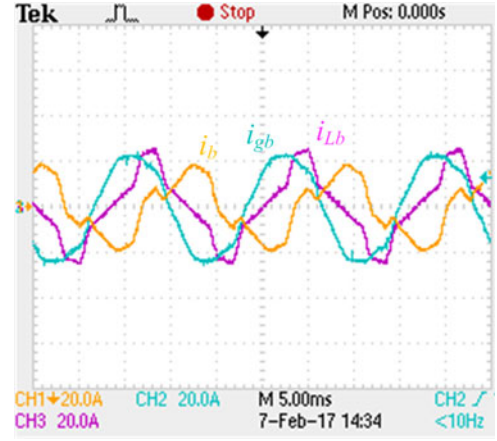


Fig. 21. Grid, load, and voltage regulator currents for nonlinear loads.

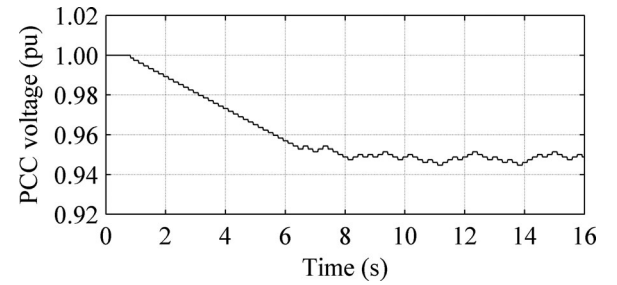


Fig. 22. PCC rms value with linear loads.

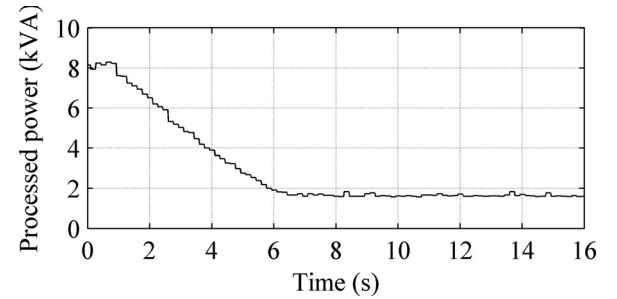


Fig. 23. Processed apparent power with linear loads.

As the mPPT gets close to the minimum power, the current amplitudes are small and the measurement precision becomes relevant. In the present case, the mPPT algorithm has large oscillations around the mPP. The processed power depicted in Fig. 23 decreases from 8 to 1.6 kVA, a reduction of around 80%. The remaining 1.6 kVA is S_{min} , the minimal necessary power for DSTATCOM operation, composed of active power (converter losses) and grid voltage harmonic distortions. The processed currents, as expected, are near zero in steady state, according to Fig. 24.

The mPPT algorithm was also evaluated with nonlinear loads. The initial value for the voltage amplitude is 1.00 p.u. and decreased to 0.9609 p.u. (211 V), as shown in Fig. 25. The apparent power reduction is lower than the linear case, of around 51%, from 7.6 to 3.7 kVA, according to Fig. 26. The harmonic currents from the nonlinear loads contribute significantly to the increase of S_{min} .

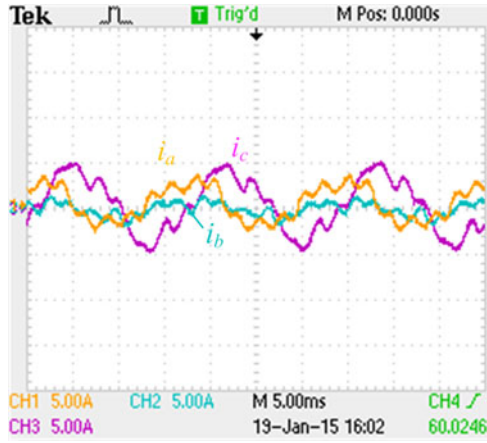


Fig. 24. Voltage regulator currents with mPPT enabled for linear loads.

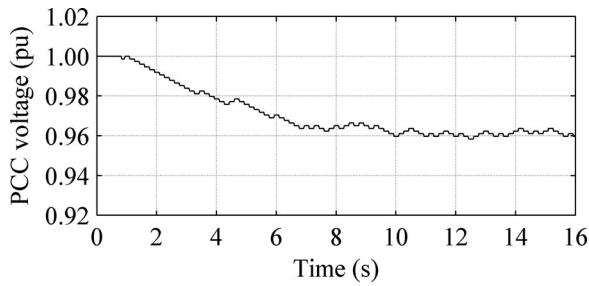


Fig. 25. PCC rms value with nonlinear loads.

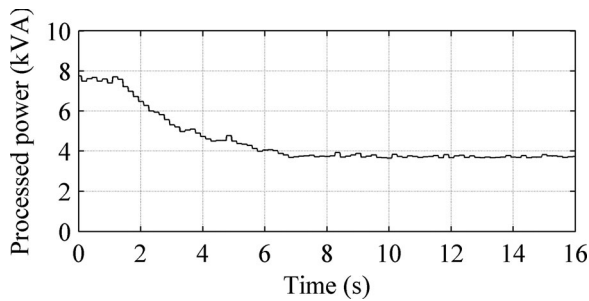


Fig. 26. Processed apparent power with nonlinear loads.

In the nonlinear load case, the processed currents are mostly composed of the harmonic distortion of the load, as seen in Fig. 27.

E. mPPT Dynamic Under Grid Voltage Variation

To evaluate the mPPT dynamic under grid voltage variations, the grid voltage was increased by steps from 1.0 to 1.079 p.u., simulating a voltage swell. The voltage regulator starts with the mPPT in steady state. Fig. 28 depicts a -phase waveforms of total dc bus voltage (v_o), PCC voltage (v_a), grid voltage (v_{ga}), and compensation current (i_a) under the increasing of the grid voltage. After each step, i_a increases to keep v_a in the previous value. The mPPT goes toward the new mPP, but reaches V_{max} first. The PCC voltage is regulated at V_{max} (1.04 p.u.) and the voltage regulator process 1.43 kVA.

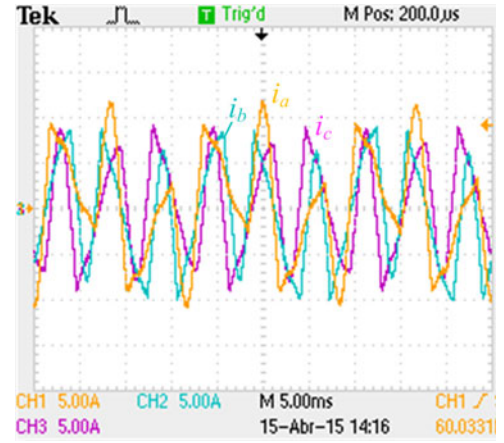
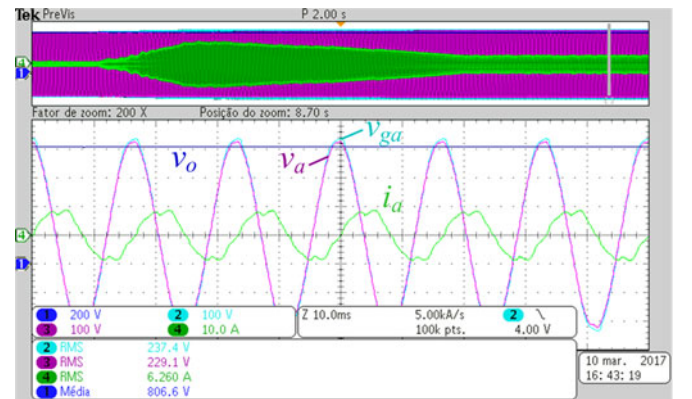


Fig. 27. Voltage regulator currents with mPPT enabled for nonlinear loads.

Fig. 28. Total dc bus voltage, PCC voltage, grid voltage, and voltage regulator current waveforms of a -phase with mPPT enabled with grid swell.

To simulate sag, the grid voltage was decreased by steps from 1.0 to 0.866 p.u. After each step, the amplitude of i_a increases and the mPPT constantly seeks the new mPP. However, the mPPT reaches V_{min} and the voltage regulator must inject reactive power in the PCC. PCC voltages are regulated at V_{min} (0.934 p.u.) with low THD, as shown in Fig. 29(a). The processed power is 4.88 kVA. The total dc bus voltage performance under the grid voltage steps is presented in Fig. 29(b), which deviates around 1.25% from the mean value.

With the PCC voltages between V_{min} and V_{max} , the voltage regulator meets the grid code and provides adequate voltage to customers.

F. Frequency Loop

The DSTATCOM is connected to a low-voltage grid and is subject to frequency variations around f_g . An example of the sampled f_{PCC} and the updated f_{ref} during the experimentations is shown in Fig. 30.

The compensation angle (θ) and the total dc bus voltage (v_o) during 100 s are presented in Fig. 31. The compensation angle varies without a defined pattern in opposition to grid frequency variations. The total dc bus voltage is kept regulated at the nominal value and the ripples are caused by the frequency updates.

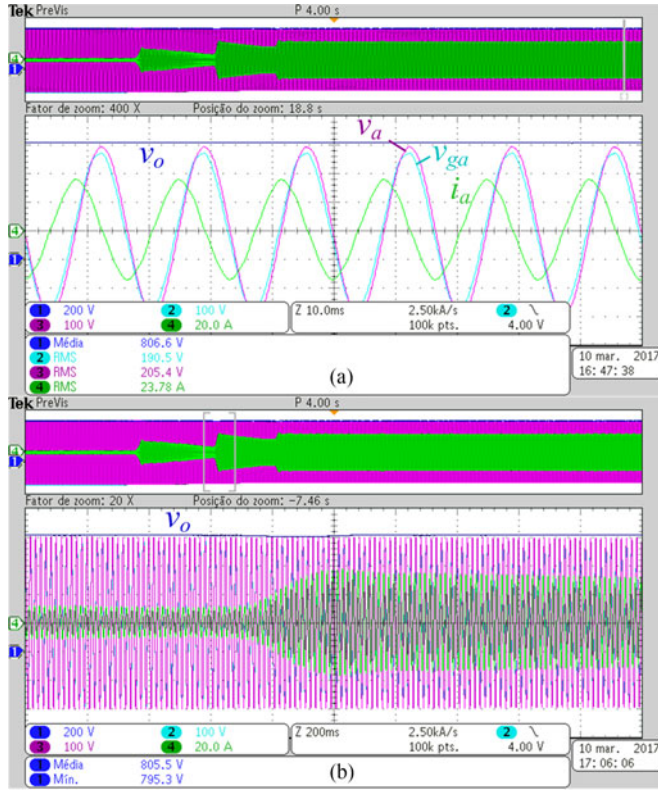


Fig. 29. (a) Total dc bus voltage, PCC voltage, grid voltage, and voltage regulator current waveforms of a -phase and (b) detail of total dc bus voltage performance with mPPT enabled with grid sag.

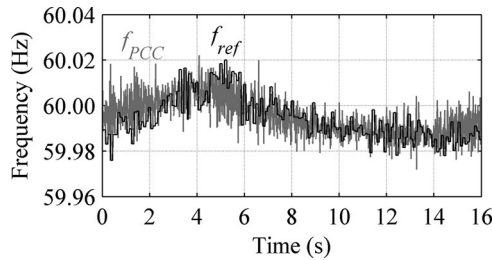


Fig. 30. PCC frequency and the reference frequency.

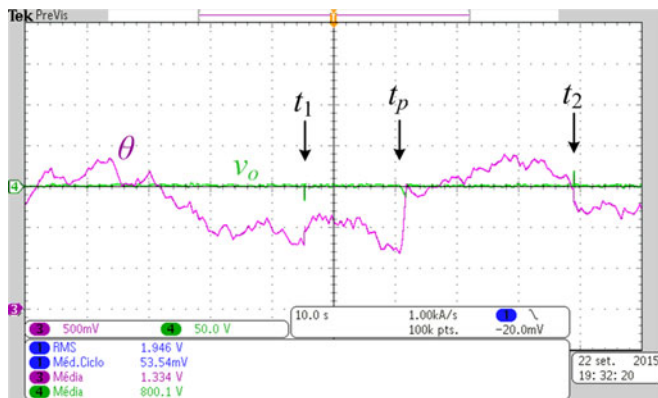


Fig. 31. Compensation angle and total dc bus voltage with the frequency compensation.

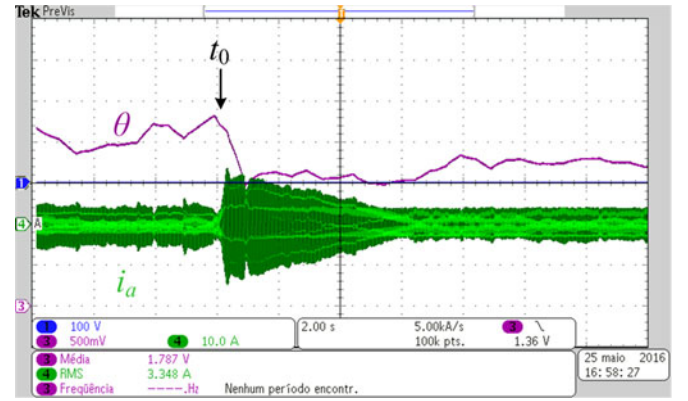


Fig. 32. Compensation angle and voltage regulator current of a -phase with mPPT and frequency loop enabled.

As cited in Section IV, the reference frequency update cannot maintain a safe operation under any kind of disturbances, or indefinitely. In this case, a frequency protection routine was implemented by adding a constant frequency to f_{PCC} , leading the compensation angle back to zero. Fig. 31 presents an example of the protection routine, where the arrow indicates the activation of the protective routine at t_p . The total dc bus voltage has a -12 -V step perturbation and returns to nominal voltage.

To verify the total dc bus voltage controller performance under the frequency loop, load perturbations are applied to the voltage regulator. Fig. 31 shows that the total dc bus voltage remains regulated under sudden load changes, from 5.2 to 10.4 kW at t_1 and backward at t_2 .

G. mPPT and Frequency Loop

The simultaneous operation of the proposed loops to compose the DSTATCOM is also evaluated. In Fig. 32, the compensation angle and the a -phase current are presented. The a -phase current is near zero as the mPPT is in steady state. At t_0 , the grid voltage is slightly perturbed in order to move the operating point from the mPP. The a -phase current decreases with the time due to actions of the mPPT and reaches a new mPP. During the mPPT perturbations, the compensation angle changes as the grid frequency varies due to the frequency loop.

VII. CONCLUSION

This paper presents a three-phase DSTATCOM as a voltage regulator and its control strategy, composed of the conventional loops, output voltage, and dc bus regulation loops, including the voltage amplitude and the frequency loops.

Experimental results demonstrate the voltage regulation capability, supplying three balanced voltages at the PCC, even under nonlinear loads.

The proposed amplitude loop was able to reduce the voltage regulator processed apparent power about 51% with nonlinear load and even more with linear load (80%). The mPPT algorithm tracked the mPP within the allowable voltage range when reactive power compensation is not necessary. With grid voltage sag and swell, the amplitude loop meets the grid code. The mPPT

can also be implemented in current-controlled DSTATCOMs, achieving similar results.

The frequency loop kept the compensation angle within the analog limits, increasing the autonomy of the voltage regulator, and the dc bus voltage regulated at nominal value, thus minimizing the dc bus voltage steady-state error. Simultaneous operation of the MPPT and the frequency loop was verified.

The proposed voltage regulator is a shunt-connected solution, which is tied to low-voltage distribution grids without any power interruption to the loads, without any grid voltage and impedance information, and provides balanced and low-THD voltages to the customers.

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