

Comprehensive Analysis of Single-Phase Full-Bridge Asymmetrical Flying Capacitor Inverters

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Abstract—This paper presents a comprehensive analysis of single-phase full-bridge asymmetrical flying capacitor inverters under distinct capacitor voltage values. The asymmetrical operation is explored in order to increase the number of output levels for the same number of semiconductors. A formation law for the flying capacitors' voltages is proposed according to the desired number of output levels. The voltage regulation of the flying capacitors is carried out using the charge regulation analysis. The modulation strategy is also verified to overcome the inverter unbalance problem. Simulation and experimental results are included to demonstrate the performance of the proposed structures.

Index Terms—Asymmetrical inverter, flying capacitor, multilevel converter, space vector modulation (SVM), voltage regulation.

I. INTRODUCTION

MULTILEVEL converters have been used in many applications in the last years due to their capacity to operate with high voltage levels employing low-voltage semiconductors [1]–[3]. Additionally, multilevel converters are able to synthesize waveforms with a higher number of output levels, reducing significantly their harmonic content and size of passive filters. Classical topologies include neutral point clamped, flying capacitor, cascaded multilevel and modular multilevel converters [4]–[7], which require a higher number of semiconductors to increase the number of levels.

An alternative to synthesize a higher number of output voltage levels, without increasing the number of semiconductors, is to use asymmetrical multilevel converters, which employ distinct values for the dc voltage sources and/or capacitor voltages

[8]–[10]. Although the synthesized waveforms present reduced distortion, power devices of asymmetrical multilevel converters are submitted to distinct voltage levels, which usually lead to hybrid multilevel converters with different semiconductor technologies and/or modulation strategies [11]–[13]. The cascaded multilevel converters can easily operate as an asymmetrical multilevel converter by employing distinct dc bus voltage sources for the converters cells [14], [15]. Flying capacitor converters are also suitable for asymmetrical operation, since they have redundant states that can be used to generate additional levels. Furthermore, flying capacitor converters do not require the use of isolated dc sources as in the cascaded multilevel topologies.

Some papers addressed the operation of asymmetrical flying capacitor converters [16]–[20]. In [16], a full-binary combination scheme was considered to increase the number of output levels for a flying capacitor leg. However, fixed voltage sources were used rather than flying capacitors. A three-phase version of a three-cell flying capacitor was presented in [17], exploring the redundant states that exists to synthesize the line-to-line voltages for the flying capacitors' voltage regulation. However, the operation with the maximum number of levels is achieved only for low-power factors. In [18], a complex finite-state model predictive control is applied to a three-cell flying capacitor leg, but some undesired switch combinations are employed to keep the capacitor voltages controlled. Although an active capacitor voltage regulating method for asymmetrical flying capacitor inverters is proposed in [19], the authors did not explore the determination of the flying capacitor voltages. A hybrid inverter topology is presented in [20], made by a three-level flying capacitor cell and a half-bridge two-level converter. In contrast to the conventional five-level inverters, the number of switches is reduced for the proposed structure, but there is no flexibility for the determination of the flying capacitor voltage. In this sense, one can observe that there are several works that use flying capacitor-based topologies, including asymmetrical ones. However, a general analysis for all the flying capacitors' voltages possibilities and for the capacitors' voltage regulation is not fully explored.

Although the number of output levels is increased for the same number of semiconductors in asymmetrical flying capacitor inverters, some redundant states are sacrificed. Therefore, a voltage regulation technique is required. Some papers addressed self-balancing or open-loop methods for the flying capacitors' inverters [21]–[24]. However, these methods did not ensure the voltage regulation for asymmetrical inverters [19].

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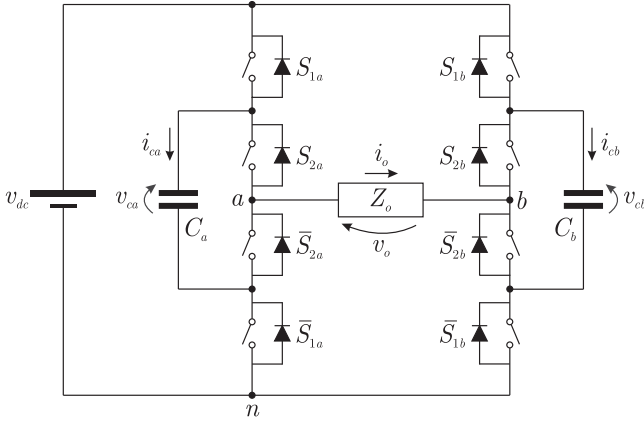


Fig. 1. Single-phase full-bridge flying capacitor inverter.

Consequently, a closed-loop strategy is required to perform the voltage regulation in asymmetrical flying capacitor inverters. For example, in [25], a proportional-integral (PI) controller was employed to obtain the voltage regulation for an asymmetric flying capacitor inverter. However, only a nine-level configuration was explored, and a formation law for the flying capacitors' voltages was not presented.

Therefore, this paper presents a comprehensive analysis for asymmetrical operation of single-phase full-bridge flying capacitor converters under distinct flying capacitors' voltages. All possible voltage configurations for the flying capacitors are explored to maximize the number of equally spaced output levels with the same number of semiconductors. The regulation problem of the flying capacitors is also addressed and an alternative space vector modulation (SVM) strategy is proposed to extend the inverter operating region.

This paper is organized as follows. Section II describes the asymmetrical multilevel topology under study and a formation law is achieved for the flying capacitors' voltages according to the desired number of output levels. Section III performs an analysis regarding the voltage regulation of the flying capacitors. A method to overcome the flying capacitor voltage regulation problem is proposed in Section IV. Finally, some simulation and experimental results are included in Section V to verify the operation of the asymmetrical flying capacitor inverter.

II. TOPOLOGY DESCRIPTION

The multilevel converter under study is shown in Fig. 1. It consists of a single-phase full-bridge inverter where each leg is composed of one flying capacitor cell with four active switches. Each leg of the inverter (leg a and leg b) is able to generate up to four distinct levels, depending on the flying capacitors' voltages.

To simplify the analysis, all voltages in the converter were normalized with respect to the dc bus voltage, i.e., $v_{dc} = 1$ p.u. Therefore, the leg voltages v_{an} and v_{bn} can present the following levels, for legs a and b , respectively:

$$v_{xn} = \{0, v_{cx}, 1 - v_{cx}, 1\}, \quad x = a, b \quad (1)$$

where v_{ca} and v_{cb} are the normalized voltages of the flying capacitors C_a and C_b , respectively. The classical symmetrical configuration is obtained by adopting $v_{ca} = v_{cb} = 1/2$ p.u. In this case, the inverter redundant states can be used for the voltage regulation of the flying capacitors and the output voltage presents up to five levels [26].

On the other hand, it is possible to increase the number of output voltage levels if the flying capacitor voltages are set to another values. The output voltage v_o is given by the difference between the leg voltages v_{an} and v_{bn} as follows:

$$v_o = v_{an} - v_{bn}. \quad (2)$$

Thus, by changing the capacitors' voltage ratio, the leg voltages can be controlled, and more combinations can be generated in the inverter output voltage v_o , according to (2). Note that, for each capacitor voltage v_{cx} there is always an equivalent capacitor voltage v_{cx}^* that can produce the same output voltage levels, defined by

$$v_{cx} + v_{cx}^* = 1, \quad x = a, b. \quad (3)$$

For example, adopting $v_{ca} = 2/5$ p.u., the leg voltage v_{an} can assume four different levels: 0, 2/5, 3/5, and 1. Equivalently, for $v_{cb} = 1/5$ p.u., the leg voltage v_{bn} is able to synthesize the following levels: 0, 1/5, 4/5, and 1. Using this capacitor voltage combination, the number of output voltage levels is increased to 11, as there are more values obtained from the combinations of the leg voltages. Moreover, by applying (3), a similar 11-level structure is obtained by using the capacitor voltage combination $v_{ca} = 3/5$ p.u. and $v_{cb} = 1/5$ p.u. However, the following restriction must be satisfied to allow the use of unidirectional voltage switches:

$$v_{cx} \leq 1 \text{ p.u.}, \quad x = a, b. \quad (4)$$

Considering these assumptions, it is possible to define three different situations for the flying capacitors' voltages, which are described in the following sections: $v_{ca} = 2v_{cb}$ (situation I), $v_{ca} = v_{cb}$ (situation II), and the equivalent voltage configurations (situation III).

A. Situation I: $v_{ca} = 2v_{cb}$

In this case, the voltage on flying capacitor C_a is greater than the voltage on flying capacitor C_b , and the following restriction must be satisfied to obtain an output waveform v_o with equally spaced output voltage levels:

$$v_{ca} = 2v_{cb}. \quad (5)$$

In addition, the voltage v_{cb} can be obtained from the desired number of output voltage levels (m) as follows:

$$v_{cb} = \frac{2}{m-1}, \quad m = 7, 9, 11, 13. \quad (6)$$

The maximum number of levels is 13, while the minimum is 7. The set of values for the output voltage v_o is obtained for a given number of levels using the following expression:

$$v_o = \left\{ \frac{2}{m-1} l - 1 \right\}, \quad l = 0, 1, 2, \dots, m-1. \quad (7)$$

TABLE I
BASE CAPACITOR VOLTAGES CONFIGURATIONS, OBTAINED FROM
SITUATION I AND SITUATION II

m	v_{ca} (pu)	v_{cb} (pu)
5	1/2	1/2
7	1/3	1/3
	2/3	1/3
9	1/4	1/4
	1/2	1/4
11	2/5	1/5
13	1/3	1/6

One can observe that there is a significant increase in the number of voltage levels compared with the conventional symmetrical configuration.

B. Situation II: $v_{ca} = v_{cb}$

The nominal voltages on flying capacitors are considered equal in this case. Similarly to situation I, the voltage v_{cb} is obtained from

$$v_{cb} = \frac{2}{m-1}, \quad m = 5, 7, 9. \quad (8)$$

However, the maximum number of levels in this situation is nine, while the minimum is five. Note that the classical symmetrical configuration is obtained for $m = 5$, so that $v_{ca} = v_{cb} = 1/2$ p.u. The set of output voltages is also given by (7). The possible flying capacitor voltage combinations, obtained from situation I and from situation II, addressed hereinafter as base configurations, are summarized in Table I.

C. Situation III: Equivalent Voltage Configurations

Although Table I presents some capacitors' voltage combinations for equally spaced output voltage levels, more configurations can be obtained by using (3). By changing the capacitors' voltages to its equivalent pairs, it is possible to synthesize the same set of output voltages for each of the converter legs. As mentioned before, considering $v_{ca} = 2/5$ p.u., the leg voltage v_{an} can assume four different levels, namely: 0, 2/5, 3/5, and 1. The same set of values are obtained considering the equivalent capacitor voltage $v_{ca} = 3/5$ p.u. Therefore, the output voltage values synthesized at the inverter output are equivalent for $v_{ca} = 2/5$ p.u. and for $v_{ca} = 3/5$ p.u. Applying this concept on both of the inverter legs for the configurations presented in Table I, the equivalent configurations are obtained, as stated in Table II. All possible capacitor voltage combinations, for equally spaced output voltage levels, are presented in Tables I and II.

III. VOLTAGE REGULATION OF THE FLYING CAPACITORS

It is imperious that the flying capacitors' voltages remain regulated around their nominal values for the correct operation of the inverter. However, for asymmetrical flying capacitor inverters, these voltages may diverge depending on the

TABLE II
EQUIVALENT CAPACITOR VOLTAGE CONFIGURATIONS,
OBTAINED FROM SITUATION III

m	v_{ca} (pu)	v_{cb} (pu)
7	2/3	2/3
9	3/4	3/4
	3/4	1/4
	1/2	3/4
11	2/5	4/5
	3/5	1/5
	3/5	4/5
13	1/3	5/6
	2/3	1/6
	2/3	5/6

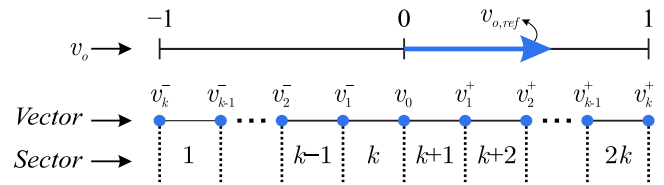


Fig. 2. Output voltage space for a m -level inverter.

amplitude modulation index and load angle. In this case, a regulating technique must be employed to restore the voltages to nominal values. An alternative is to use redundant states of the inverter, which synthesize the same output voltage but with different contributions to the flying capacitors' currents. Nevertheless, regarding asymmetrical flying capacitor inverters, the increase in the number of output levels reduces the number of redundant states, which can impair the voltage regulating technique.

Therefore, a careful analysis must be made to ensure the voltage regulation of the flying capacitors. The SVM is especially interesting for this goal, since it is easy to evaluate the impact of each switching state on the output voltage and capacitors' voltage regulation.

The space vector diagram for an m -level single-phase flying capacitor inverter is illustrated in Fig. 2. One can observe positive ($v_1^+, v_2^+, \dots, v_k^+$), negative ($v_1^-, v_2^-, \dots, v_k^-$), and one zero (v_0) vectors, originating $2k$ different sectors, where $k = (m-1)/2$. Although the voltage levels in Fig. 2 are presented as scalars, they can be referred as vectors in a one dimensional space ($\mathbb{R}^1$). The output voltage is $v_{o,ref}$, and it is given by

$$v_{o,ref}(\theta) = m_a \sin(\theta) \quad (9)$$

where θ is the fundamental angle, and m_a is the amplitude modulation index, which varies from zero to unity in the linear operating region. Note that the desired average value of the output voltage ($\bar{v}_o$) can be synthesized using the two nearest vectors to the reference during a switching period, as given by

$$\bar{v}_o = d_y v_y + d_z v_z \quad (10)$$

where d_y and d_z are the duty cycles of the two nearest vectors to the reference voltage v_y and v_z , respectively. Therefore, the

TABLE III
NUMBER OF SWITCHING STATES FOR EACH POSITIVE VECTOR

m	v_{ca} (pu)	v_{cb} (pu)	v_0	v_1^+	v_2^+	v_3^+	v_4^+	v_5^+	v_6^+
5	1/2	1/2	6	4	1	-	-	-	-
7	1/3	1/3	4	3	2	1	-	-	-
	2/3	1/3	4	3	2	1	-	-	-
9	1/4	1/4	4	2	1	2	1	-	-
	1/2	1/4	2	3	2	1	1	-	-
11	2/5	1/5	2	2	2	1	1	1	-
13	1/3	1/6	2	2	1	1	1	1	1

duty cycle associated to each vector can be obtained using the following relationship for any sector of the output voltage space:

$$\begin{bmatrix} d_y \\ d_z \end{bmatrix} = \begin{bmatrix} v_y & v_z \\ 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} v_{o,ref} \\ 1 \end{bmatrix}. \quad (11)$$

Without loss of generality, only the configurations presented in Table I are analyzed in the voltage regulation, since the current contribution of the vectors from the base configurations and their respective equivalent configurations is the same (in module). Similarly, the current contribution of positive and negative vectors is also the same (in module). Based on these statements, Table III shows the number of switching states for each positive vector of the base configurations presented in Table I.

From Table III, it is observed that the number of redundant states decreases for a higher number of levels, and the voltage regulation of the flying capacitors becomes rather challenging. For higher level configurations, the main source of unbalance is the use of uncontrollable vectors, which affect the flying capacitors' currents but do not have redundancies for the capacitors' voltage regulation. On the other hand, the average value of the capacitors' currents can be controlled using the redundant states of controllable vectors. Thus, to obtain the operation region (load angle and amplitude modulation index), where it is possible to regulate the voltage on the flying capacitors, the following restriction must be met:

$$|Q_{c,x}(m_a, \varphi)| \geq |Q_{u,x}(m_a, \varphi)|, \quad x = a, b \quad (12)$$

where $Q_{c,a}$ and $Q_{c,b}$ are the maximum attainable charge of controllable vectors that can control the flying capacitors C_a and C_b average currents, respectively. Contrarily, $Q_{u,a}$ and $Q_{u,b}$ are the charge of uncontrollable vectors that do not have redundancies for the voltage regulation of capacitors C_a and C_b , respectively. If restriction (12) is met, then it implies that there is a feasible solution that allows the voltage regulation of the flying capacitors.

Therefore, the voltage regulation of the flying capacitors is closely related to the inverter switching redundancies. Clearly, the controllable vectors must be able to compensate the uncontrollable vectors to obtain the inverter operating region. Therefore, the operating region for each configuration shown in Table III will be analyzed in the following sections.

A. Nine-Level Configuration

Among the asymmetrical configurations given in Table III, the nine-level structure with $v_{ca} = 1/2$ p.u. and $v_{cb} = 1/4$ p.u. is specially interesting, since the number of levels is increased

TABLE IV
IMPACT OF POSITIVE VECTORS ON THE FLYING CAPACITORS' VOLTAGES
CONSIDERING $m = 9$, $v_{ca} = 1/2$ P.U. AND $v_{cb} = 1/4$ P.U.

Vector	State	S_{1a}	S_{2a}	S_{1b}	S_{2b}	C_a	C_b	v_o (pu)
v_0	$v_{0,1}$	0	0	0	0	-	-	0
	$v_{0,2}$	1	1	1	1	-	-	
v_1^+	$v_{1,1}^+$	1	0	0	1	↑	↑	1/4
	$v_{1,2}^+$	0	1	0	1	↓	↑	
	$v_{1,3}^+$	1	1	1	0	-	↓	
v_2^+	$v_{2,1}^+$	1	0	0	0	↑	-	1/2
	$v_{2,2}^+$	0	1	0	0	↓	-	
v_3^+		1	1	0	1	-	↑	3/4
v_4^+		1	1	0	0	-	-	1

↑ (charging), ↓ (discharging), - (unchanged)

to nine, and one of the inverter legs maintains the symmetrical feature. Thus, the analysis presented hereinafter addresses the voltage regulation issue for this nine-level inverter and can be extended to its equivalent configuration with $v_{ca} = 1/2$ p.u. and $v_{cb} = 3/4$ p.u., since the contribution of the vectors on the flying capacitors' currents, for both structures, is the same (in module).

The positive vectors and their contribution to the flying capacitors' voltages are summarized in Table IV, considering a positive load current, as defined in Fig. 1. Although vector v_0 has two redundant states ($v_{0,1}$ and $v_{0,2}$), it does not affect the average current in the flying capacitors. On the other hand, vector v_1^+ has three redundant states ($v_{1,1}^+$, $v_{1,2}^+$, and $v_{1,3}^+$) and vector v_2^+ has two redundant states ($v_{2,1}^+$ and $v_{2,2}^+$). Vector v_3^+ does not have redundant states and it affects the average current in capacitor C_b . Finally, vector v_4^+ does not affect the average currents in both flying capacitors.

One can verify from Table IV that the flying capacitor C_a does not have problems with the voltage regulation, since it is possible to even eliminate its low-frequency ripple. This can be made by adjusting the distribution rate of redundant states of v_1^+ and v_2^+ over a switching period, since these redundant states have distinct impacts on the currents across C_a . For example, when it is necessary to apply the vector v_2^+ , the effective duty cycle d_2 can be equally distributed between $v_{2,1}^+$ and $v_{2,2}^+$. As a result, the contribution of the vector v_2^+ in the average current of the flying capacitor C_a , in a switching period is zero. Regarding the vector v_1^+ , there are three possible states to generate the same output voltage. If the state $v_{1,3}^+$ is used, the contribution to the average current in capacitor C_a is null. However, if it is necessary to charge the capacitor C_b , the states $v_{1,1}^+$ or $v_{1,2}^+$ should be used. Therefore, the duty cycles associated to these states must be equal to keep the contribution in the average current of the capacitor C_a equal to zero. Consequently, using this strategy, the voltage of the flying capacitor C_a remains regulated for all load angles and amplitude modulation index values. In other words, even if the inverter operation point changes, the average capacitor current in a switching period is always kept at zero.

On the other hand, the voltage regulation of the flying capacitor C_b presents some peculiarities. The main source of unbalance for capacitor C_b is the use of the vector v_3^+ , since it affects the

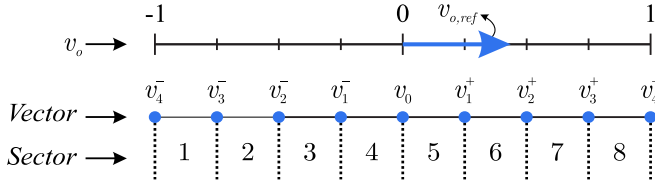
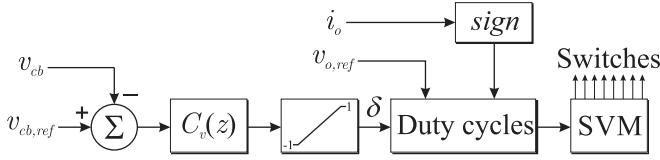
Fig. 3. Output voltage space for $m = 9$.

Fig. 4. Block diagram of the inverter control system.

capacitor current and does not have redundant states. Thus, the total uncontrollable charge of the capacitor C_b is determined by

$$Q_{u,b}(m_a, \varphi) = \int_0^\pi i_o(\theta, \varphi) d_3(\theta, m_a) d\theta. \quad (13)$$

The load current is defined here as

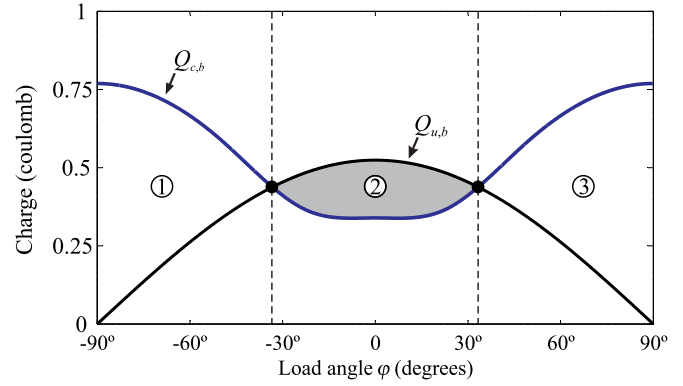
$$i_o(\theta, \varphi) = I \sin(\theta + \varphi) \quad (14)$$

where I is the peak value of the load current and φ is the load angle that represents the output power factor.

The output voltage space for the nine-level inverter is presented in Fig. 3. The vector v_3^+ is used if the reference voltage is located in sectors five and six. For these sectors, there is a degree of freedom for the voltage regulation of the capacitor C_b , since there are three redundant states associated to v_1^+ . Thus, the average value of the capacitor current can be controlled in this sector using these redundant states, so that

$$\bar{i}_{cb} = |i_o| d_1 \delta, \quad -1 \leq \delta \leq 1. \quad (15)$$

The variable δ is the current modulation index, which is the variable used for the voltage control into a switching period. For example, if $\delta = -1$, during the entire period that the reference is located into the sectors five and six the capacitor C_b will be discharged, since only the state $v_{1,3}^+$ is employed, considering a positive load current. Similarly, if $\delta = 0$, during half of the switching period, the state $v_{1,3}^+$ is used while in the remaining time the states $v_{1,1}^+$ and/or $v_{1,2}^+$ are used. Therefore, the voltage regulation for the capacitor C_b depends on amplitude modulation index m_a , output current i_o (load angle), and current modulation index δ . The block diagram of the capacitor voltage control system is shown in Fig. 4. A digital PI controller $C_v(z)$ is employed to obtain the variable δ . Only the voltage of the capacitor C_b is measured, since capacitor C_a does not have problems of voltage regulation. This routine is executed at every sampling period, and it is valid if condition (12) is satisfied. Note that the sign of the load current and the output voltage reference $v_{o,ref}$ are used to compute the duty cycles. This is necessary to ensure that the charge and discharge of C_b are controlled only by δ , independently of the sign of i_o . Therefore, the duty cycles

Fig. 5. Charge in C_b as a function of the load angle, for $m_a = 0.65$ and $I = 1$ A.

of the vector v_1^+ redundant states are determined by

$$d_{1,1} = d_{1,2} = (1 + \text{sign}(i_o)\delta) d_1 / 4 \quad (16)$$

$$d_{1,3} = (1 - \text{sign}(i_o)\delta) d_1 / 2 \quad (17)$$

where $\text{sign}(i_o) = -1$ for $i_o < 0$ and $\text{sign}(i_o) = 1$ for $i_o \geq 0$. $d_{1,1}$, $d_{1,2}$, and $d_{1,3}$ are the duty cycles of the redundant vectors $v_{1,1}^+$, $v_{1,2}^+$, and $v_{1,3}^+$, respectively. These values are used to implement the SVM.

Thus, if restriction (12) is met, then it implies there is a feasible solution for the variable δ within the interval $[-1, 1]$ that allows the capacitors' voltage regulation. The maximum capacitor charge associated to sectors five and six (controllable portion) is obtained by the integral of the capacitor current considering $\delta = 1$. So that

$$Q_{c,b}(m_a, \varphi) = \int_0^\pi |i_o(\theta, \varphi)| d_1(\theta, m_a) d\theta. \quad (18)$$

To exemplify the application of restriction (12), the charges $Q_{c,b}$ and $Q_{u,b}$, as a function of the load angle and considering $m_a = 0.65$ and $I = 1$ A, are shown in Fig. 5. It is possible to verify that $Q_{c,b} > Q_{u,b}$ in the regions 1 and 3, indicating that the voltage regulation is feasible. On the other hand, $Q_{c,b} < Q_{u,b}$ in the region 2, which means that voltage regulation is not possible. Thus, one can see from Fig. 5 that the voltage regulation of the capacitor C_b can be obtained only for a load angle below -34° or above 34° when $m_a = 0.65$.

Extending the results shown in Fig. 5 for the whole range of modulation index, the solution space for the voltage regulation of the inverter is shown in Fig. 6. These results were obtained considering the inverter operation in the steady state. The regions B and C represent the operational points (load angle, amplitude modulation index) where the voltage regulation is possible (stable region), i.e., the restriction (12) is satisfied. In the region C, the low-frequency voltage ripple on capacitor C_b can also be eliminated, since only the controllable vectors v_0 , v_1^+ , and v_2^+ are used for $m_a \leq 0.5$, according to Fig. 3 and considering only positive vectors. Thus, the voltage regulation is feasible in a switching period. On the other hand, for region B, the voltage regulation is obtained in half of the fundamental period for the capacitor C_b . However, the voltage regulation is

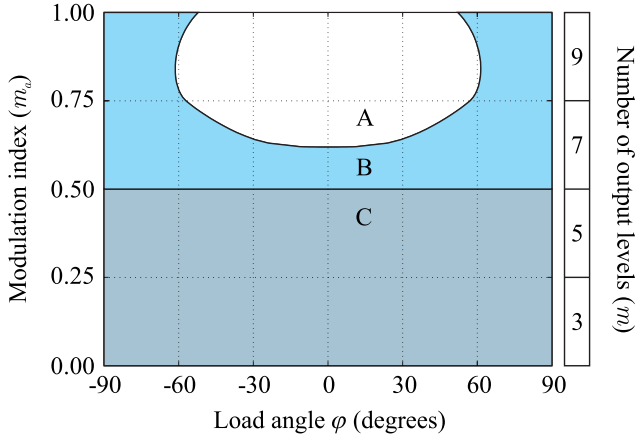


Fig. 6. Solution space where it is possible to make the voltage regulation for $m = 9$, $v_{ca} = 1/2$ p.u., and $v_{cb} = 1/4$ p.u. Region A: Non-operable region. Region B: Low-frequency voltage ripple region. Region C: Normal operating region.

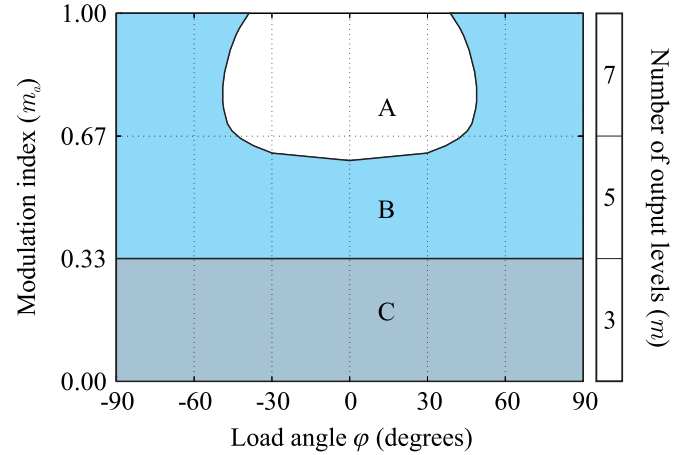


Fig. 7. Solution space where it is possible to make the voltage regulation for $m = 7$. Region A: Non-operable region. Region B: Low-frequency voltage ripple region. Region C: Normal operating region.

TABLE V
IMPACT OF POSITIVE VECTORS ON THE FLYING CAPACITORS' VOLTAGES
CONSIDERING $m = 13$, $v_{ca} = 1/3$ p.u. AND $v_{cb} = 1/6$ p.u.

Vector	State	S_{1a}	S_{2a}	S_{1b}	S_{2b}	C_a	C_b	v_o (pu)
v_0	$v_{0,1}$	0	0	0	0	-	-	0
	$v_{0,2}$	1	1	1	1	-	-	
v_1^+	$v_{1,1}^+$	0	1	0	1	↓	↑	1/6
	$v_{1,2}^+$	1	1	1	0	-	↓	
v_2^+		0	1	0	0	↓	-	1/3
v_3^+		1	0	0	1	↑	↑	1/2
v_4^+		1	0	0	0	↑	-	2/3
v_5^+		1	1	0	1	-	↑	5/6
v_6^+		1	1	0	0	-	-	1

↑ (charging), ↓ (discharging), - (unchanged)

not achieved in the region A and the voltage on the capacitor C_b will diverge from its nominal value. The reason for this is that for loads with the power factor angle above 60° and for $m_a \geq 0.62$, the vector v_3^+ is applied when the load current is near to its maximum value (in module) making that voltage on capacitor deviates from its nominal value. Similarly, the voltage on capacitor C_b also diverges for load angles below -60° and $m_a \geq 0.62$. Consequently, the application of the redundant states related to the controllable part of the current is not enough to compensate it. In contrast, for region B, the application of the vector v_3^+ occurs when the load current is small, and the compensation can be made through redundant states of the vector v_1^+ , ensuring the voltage regulation.

B. Thirteen-Level Configuration

The maximum number of output levels for the single-phase flying capacitor inverter is obtained by adopting $v_{ca} = 1/3$ p.u. and $v_{cb} = 1/6$ p.u., considering the structures presented in Table III. The positive vectors and their contribution to the flying capacitors' currents are presented in Table V, for the positive load current, as defined in Fig. 1.

One can observe that the 13-level configuration presents a limited number of redundant states. Vector v_0 has two redundant states and does not affect the flying capacitors' currents. Similarly, vector v_1^+ also has two redundant states, but it directly affects the capacitors' voltage regulation. Vectors v_2^+ , v_3^+ , v_4^+ , and v_5^+ do not have redundant states and affect at least one of the flying capacitors' currents. Finally, vector v_6^+ does not affect the current in both flying capacitors. The voltage regulation for capacitor C_b can be achieved for a limited range of amplitude modulation index and load angles, in half of the fundamental period, by adjusting the duty cycles of the vector v_1^+ redundant states. However, there are no redundant states for the current control of the flying capacitor C_a . Therefore, there is no controllability for the inverter voltage, and the 13-level configuration does not present a feasible operating region.

C. Operating Region Comparison

In this section, the operating region of the configurations under study will be discussed to select the proper structure for a given application. The analysis presented hereinafter only addresses the base configurations, since their respective equivalent configurations presents the same regulating region, as the current contribution of the vectors from both configurations is the same (in module).

There are three possible capacitors' voltages combinations, which results in a seven-level inverter. This configuration has the main advantage that a larger number of redundant states greatly simplifies the voltage regulation process. Using a similar analysis to that presented for the nine-level configuration, one can obtain the operating region for all the seven-level topologies, presented in Fig. 7. Unlike the aforementioned nine-level inverter, region A represent the unstable region, where the flying capacitors' voltages diverge from their nominal values. The voltage regulation is achieved in regions B and C. In region C, as there are no uncontrollable vectors, the low-frequency voltage ripple can also be eliminated from both flying capacitors.

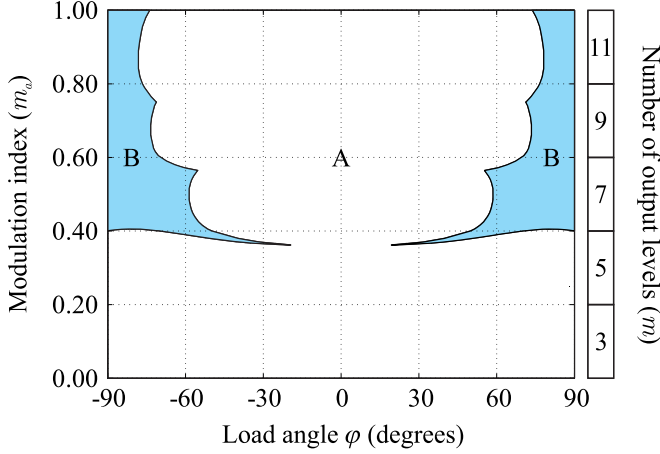


Fig. 8. Solution space, where it is possible to make the voltage regulation for $m = 11$. Region A: Non-operable region. Region B: Low-frequency voltage ripple region.

Regarding the nine-level topology, there are two possible base configurations that produce equally spaced output voltage levels. The operating region of the nine-level inverter is presented in Fig. 6, considering $v_{ca} = 1/2$ p.u. and $v_{cb} = 1/4$ p.u. Note that there is a significant decrease in the inverter operating region compared to the seven-level configuration, as there are fewer redundant states for the average current control of the flying capacitors.

In addition, a nine-level inverter is also obtained by adopting $v_{ca} = v_{cb} = 1/4$ p.u. However, this configuration presents no controllable vectors for the voltage regulation. Therefore, this configuration does not present a feasible operating region.

The operating region for the 11-level inverter is presented in Fig. 8. The complete control over the flying capacitors' voltages is achieved only in region B. Additionally, the flying capacitors' voltages, in the inverter stable region, always present low-frequency ripple, as the voltage regulation is only achieved in half of the fundamental period.

IV. EXTENSION OF THE CONVERTER OPERATING REGION

As can be observed, the operating region of each asymmetrical configuration is limited. An alternative to expand the inverter stable region is to use the virtual vectors concept [27]. However, the output voltage distortion will be increased and the output voltage will present unequally spaced output voltage levels.

The uncontrollable vectors are the main source of unbalance for the operation of the converter. This occurs because these vectors affect the current on the flying capacitors but have no redundant states for the voltage regulation. Since it is possible to synthesize the average value of the uncontrollable vectors using controllable vectors, it is possible to decrease or even eliminate the duty cycle associated to the uncontrollable vectors to extend the operating region of the full-bridge asymmetrical flying capacitor inverter. For example, Fig. 9 presents a new space solution for the nine-level configuration operating region presented in Fig. 6, successively reducing the duty cycle associated to the vector v_3^+ . In this case, vectors v_2^+ and v_4^+ were used to

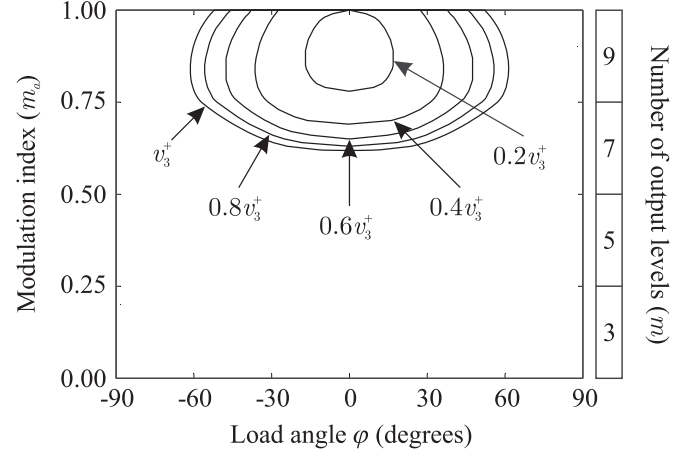


Fig. 9. New solution space for the nine-level configuration by successively reducing the duty cycle of the vector v_3^+ .

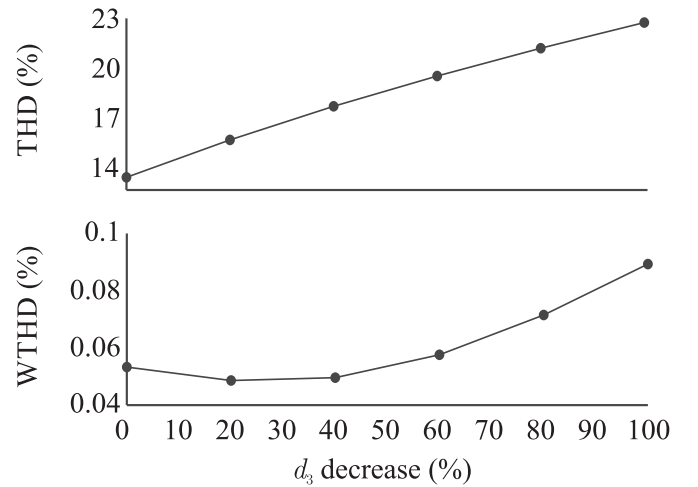


Fig. 10. Impact of the vector v_3^+ reduction in the converter THD and in the WTHD, for $m_a = 0.98$, $C_a = 1$ mF, and $C_b = 4.7$ mF.

synthesize the average value of the vector v_3^+ , in a switching period. It is possible to notice that, for each decrease in the use of this vector, the functional area of the inverter increases, until the case $d_3 = 0$, where the inverter can operate for any load angle and amplitude modulation index. On the other hand, by decreasing the application time of the vector v_3^+ , the output voltage tends to distort, and the total harmonic distortion (THD) and the weighted total harmonic distortion (WTHD) [28] increase, as illustrated in Fig. 10.

V. RESULTS

Simulation and experimental results were obtained to verify the operation of the proposed regulation strategy. The parameters adopted are described in Table VI, where the nine-level inverter was considered. The modulation and the control law for the voltage regulation of the capacitor C_b was implemented in a digital signal processor. Only the voltage of the capacitor C_b is measured, since the capacitor C_a does not have problems

TABLE VI
INVERTER PARAMETERS

Parameter	Value
dc bus voltage (v_{dc})	200 V
Voltage on capacitor C_a	100 V
Voltage on capacitor C_b	50 V
Capacitor C_a	1 mF
Capacitor C_b	4.7 mF
Fundamental frequency (f_1)	50 Hz
Switching frequency (f_{sw})	2.6 kHz
Load 1	$1.8 + 14.13j \Omega$
Load 2	$31.4 + 14.13j \Omega$

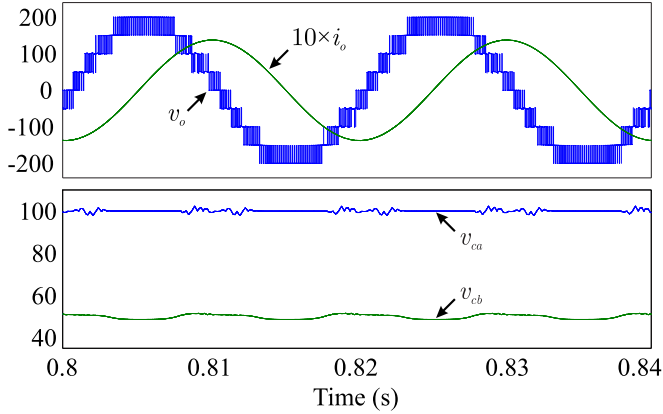


Fig. 11. Simulation results for load 1 and $m_a = 0.98$. Top: Output voltage and current. Bottom: Flying capacitors' voltages.

with the voltage regulation. Two resistive–inductive loads were considered to validate the inverter operation region: low power factor (load 1) and high power factor (load 2), as presented in Table VI.

The design of the flying capacitors can be made using distinct criteria. As the capacitor C_a has only high-frequency voltage ripple, a capacitance of 1 mF can be used with acceptable results. On the other hand, the capacitor C_b presents a low-frequency voltage ripple if the inverter operates in region B of Fig. 6. Therefore, a capacitance of 4.7 mF was chosen for capacitor C_b , maintaining its voltage ripple on acceptable levels.

A. Simulation Results

A simulation result for the converter operating with $m_a = 0.98$ and using load 1 is presented in Fig. 11. One can verify the nine levels generated at the inverter output and the voltage on the flying capacitors. As expected, the voltage on capacitor C_b presents some low-frequency ripple in this operation point (region B in Fig. 6). Moreover, the voltage regulation of the capacitor C_a is also achieved with the proposed modulation strategy.

The flying capacitors' currents are shown in Fig. 12. For each switching period, the average current of the capacitor C_a is equal to zero, resulting in only a high-frequency voltage ripple in this capacitor. On the other hand, the flying capacitor C_b

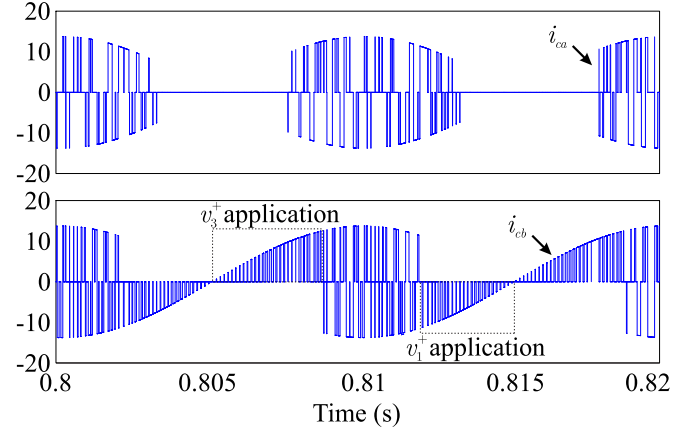


Fig. 12. Simulation results for the flying capacitors' currents for load 1 and $m_a = 0.98$. Top: Current in capacitor C_a . Bottom: Current in capacitor C_b .

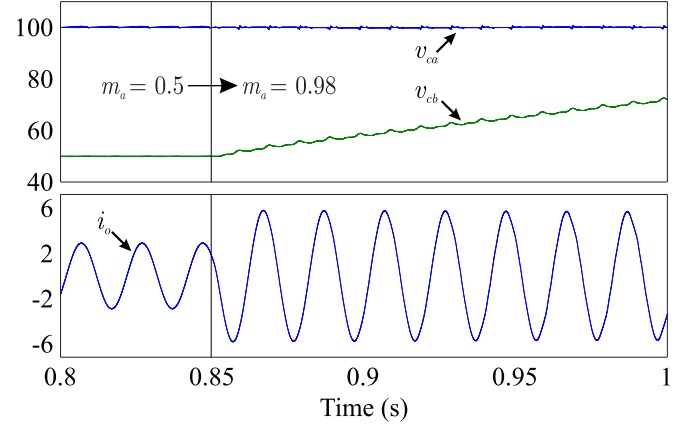


Fig. 13. Simulation result for an amplitude modulation index step. Top: Flying capacitors' voltages. Bottom: Output current.

current is always positive during the application of the vector v_3^+ in the inverter output. Therefore, the controllable vector v_1^+ must be used to maintain the average current equal to zero for the capacitor C_b , in half of the fundamental period.

On the other hand, considering the load 2, the voltage regulation of the flying capacitor C_b is achieved for lower values of the modulation index, as described in Fig. 13. In this result, an amplitude modulation index step is performed at 850 ms ($m_a = 0.5 \rightarrow m_a = 0.98$), where it is possible to verify that the voltage on capacitor C_b diverges from its nominal value, since this operation point is inside region A, shown in Fig. 6.

Fig. 14 presents the output voltage if the duty cycle set to vector v_3^+ is zero, for the load 2, for a high load power factor. Since there is no non-operational area for this case, the voltage in capacitor C_b remains regulated. Even so, a seven-level output voltage is still guaranteed.

The output voltage v_o spectrums for the nine-level waveform and for the seven-level waveform are shown in Fig. 15. The fundamental voltage for both configurations is equal to 196 V. While the fundamental voltage is not affected, there are some harmonic components that arise from the voltage regulation

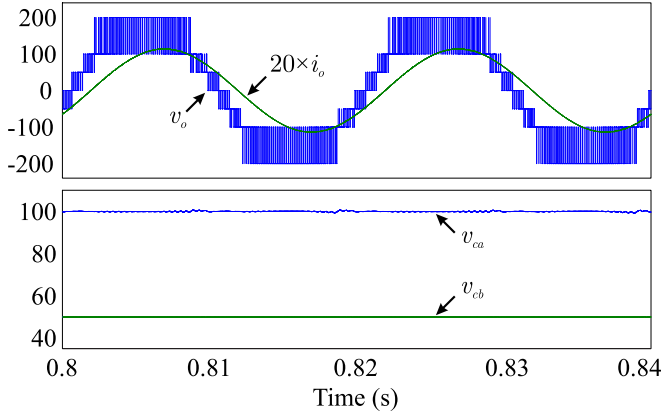


Fig. 14. Simulation result for $d_3 = 0$, $m_a = 0.98$ load 2. Top: Output voltage and current. Bottom: Flying capacitors' voltages.

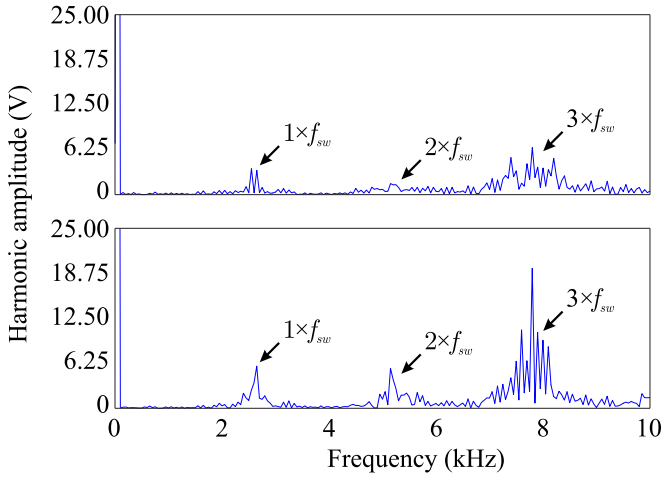


Fig. 15. Simulation results of the output voltage spectrum for $m_a = 0.98$. Top: Output voltage spectrum for the nine-level waveform. Bottom: Output voltage spectrum for the seven-level waveform with $d_3 = 0$.

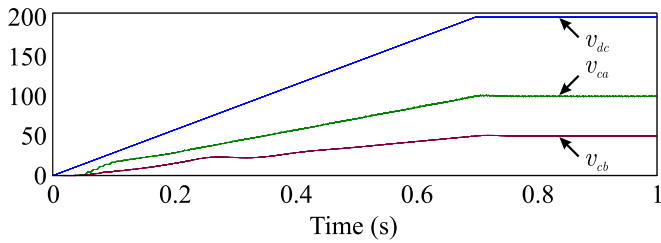


Fig. 16. Simulation results of the pre charging method for the flying capacitors' voltages.

method. Furthermore, it is clearly noticeable that some harmonic components of the seven-level waveform present greater amplitude compared to the nine-level waveform, resulting in a greater harmonic distortion for the output voltage.

Finally, the pre charging method used for the initialization of the inverter is illustrated in Fig. 16. A PI controller was implemented for the flying capacitor C_a voltage regulation only during this period. The flying capacitors' voltages are defined

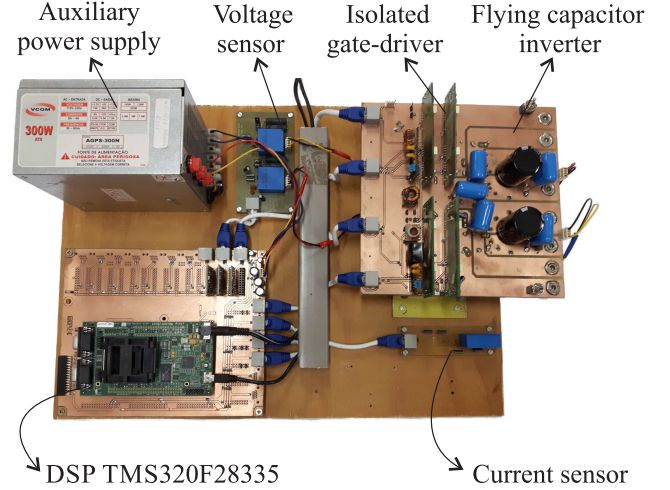


Fig. 17. Prototype of the flying capacitor inverter.

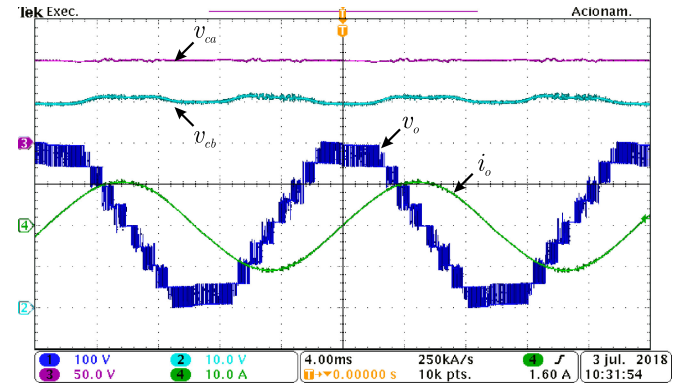


Fig. 18. Experimental results for load 1 and $m_a = 0.98$: Output voltage, output current, and flying capacitors' voltages.

based on the dc bus voltage v_{dc} , which rises linearly. Using this approach, the proportion between the dc bus voltage and the capacitors' voltages remains constant and the voltage is adequately shared between the semiconductors.

B. Experimental Results

Experimental results were obtained through the prototype shown in Fig. 17 and considering the parameters given in Table VI. Current and voltage sensors, LA 55-P and LV 20-P, respectively, were used for the capacitors' voltage regulation.

Experimental results for $m_a = 0.98$ and using the load 1 are shown in Fig. 18. It is possible to verify the nine-level voltage generated at inverter output as well as the balanced voltages on the flying capacitors C_a and C_b . The voltage v_{ca} is free of a low-frequency ripple while the voltage v_{cb} presents a low frequency originated by the voltage regulation strategy.

The flying capacitors' currents can be verified in Fig. 19. Note that the average value of the current can be controlled for each switching period in capacitor C_a . Furthermore, since the inverter is operating in region B of Fig. 6, the controllable vectors are used to maintain the average current contribution in

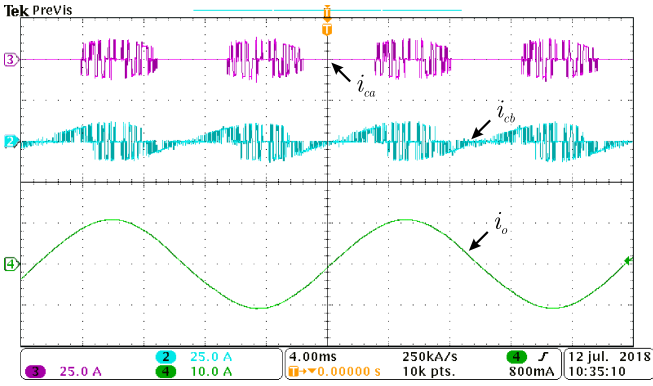


Fig. 19. Experimental results for the flying capacitors' currents for load 1 and $m_a = 0.98$: Current of the capacitor C_a , current of the capacitor C_b , and output current.

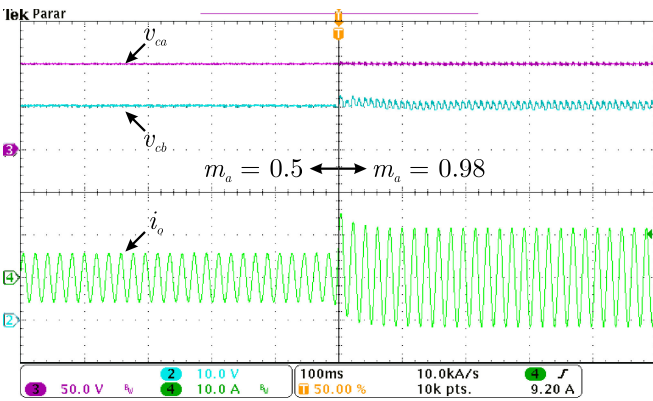


Fig. 20. Experimental result for modulation index step (load 1): Flying capacitors' voltages and output current.

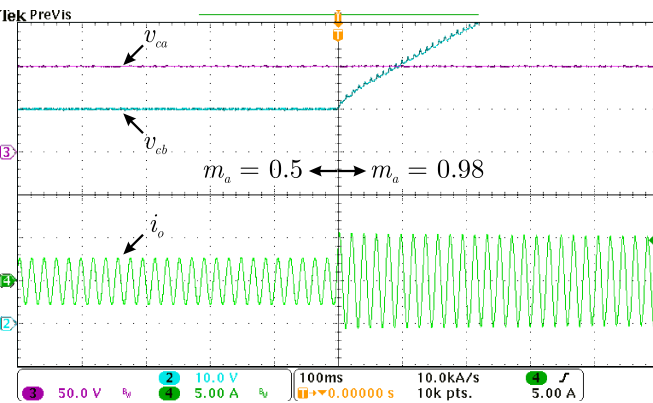


Fig. 21. Experimental result for modulation index step (load 2): Flying capacitors' voltages and output current.

the flying capacitor C_b equal to zero, in half of the fundamental period.

The inverter voltage regulation capability can be verified in Figs. 20 and 21, where an amplitude modulation index step was performed. The voltage on the flying capacitors remained regulated for load 1 in both cases, as shown in Fig. 20. This result shows that the proposed voltage regulation strategy can also

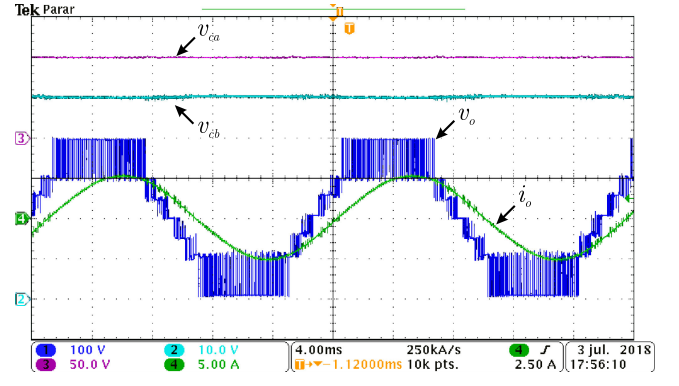


Fig. 22. Experimental results for $d_3 = 0$ and $m_a = 0.98$ (load 2): Output voltage, output current and flying capacitors' voltages.

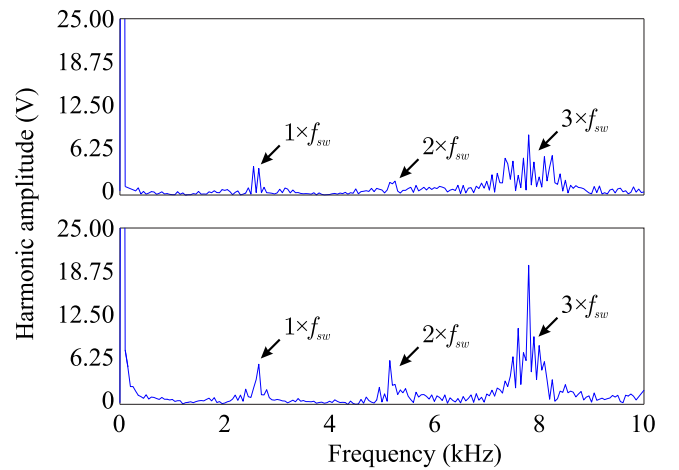


Fig. 23. Experimental results of the output voltage spectrum for $m_a = 0.98$. Top: Output voltage spectrum for the nine-level waveform. Bottom: Output voltage spectrum for the seven-level waveform with $d_3 = 0$.

recover from transients. Additionally, low-frequency components are present on voltage v_{cb} only for high values of the modulation index. Considering the load 2, the voltage regulation is achieved only for low values of the amplitude modulation index.

The Fig. 22 presents the output waveform setting $d_3 = 0$, for load 2. Note that the voltages of the flying capacitors remain regulated for any load condition for this configuration. The low-frequency ripple of capacitor C_b is also eliminated. However, the total harmonic distortion increases.

Fig. 23 presents the experimental results for the spectrum of the output voltage v_o of the inverter. The fundamental components are equal to 192 V and 188 V for the nine-level the seven-level waveforms, respectively. This occurs mainly because of the voltage drop in the diodes for a negative output current, as defined in Fig. 1, that directly affects the output voltage. Moreover, the seven-level waveform presents higher distortion, as its harmonic components have greater amplitude. This phenomenon has already been observed in Fig. 10.

The experimental results for the pre charging method of the flying capacitors are shown in Fig. 24. The flying capacitors' voltages references are calculated based on the dc bus voltage

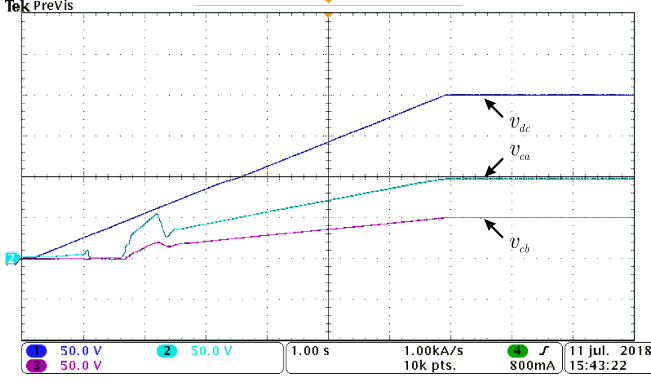


Fig. 24. Experimental results of the pre charging method for the flying capacitors' voltages.

value, which rises linearly. This process continues until the converter reaches its nominal voltage, i.e., $v_{dc} = 200$ V.

VI. CONCLUSION

This paper proposed a detailed analysis for single-phase asymmetrical flying capacitor inverters under distinct capacitor voltage values. One can verify that it is possible to increase the number of output voltage levels using the same number of semiconductors. This is achieved by adopting unconventional values for the capacitors voltages. Therefore, a formation law for the flying capacitors' voltages in function of the number of output levels was achieved. A general voltage regulation analysis of the flying capacitors was addressed for the different possible inverter configurations from the space vectors modulation concept. From an operation viewpoint, the voltage regulation of the flying capacitors is highly dependent of the inverter redundant states. The operating regions of the converter were obtained so that some configurations operate for a limited range of amplitude modulation indexes and load angles. Therefore, authors believe that this topology can be mainly used for applications that require low power factor, such as in reactive power compensation. An alternative SVM was presented in this paper in order to overcome the inverter unbalance issue for high power factors, by modifying the applications time of the uncontrollable vectors.

APPENDIX

This appendix aims to clarify the achievement of (5), (6), and (7), presented in Section II. Note that the maximum positive voltage is 1 p.u., while the adjacent level is $1 - v_{cb}$ p.u., since $v_{cb} < v_{ca}$. Therefore, the difference between these two levels gives the smaller output voltage step (Δv) as follows:

$$\Delta v = 1 - (1 - v_{cb}) = v_{cb}. \quad (19)$$

One can verify from (19) that the smaller output voltage step is equal to the voltage of the capacitor C_b . The next adjacent level is $1 - v_{ca}$ p.u. In this sense, the following relation must be satisfied to keep the same Δv for these levels:

$$\Delta v = (1 - v_{cb}) - (1 - v_{ca}) = v_{ca} - v_{cb}. \quad (20)$$

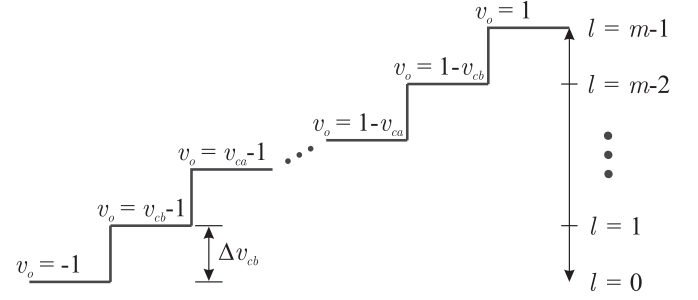


Fig. 25. Representation of the output voltage levels.

Thereby, substituting (19) into (20), it is possible to obtain the same expression described previously in (5). In order to obtain (6) and (7), it is necessary to consider Fig. 25. It is possible to notice that the overall excursion of the output voltage is 2 p.u., which is divided into $m - 1$ steps. Therefore, the smaller output voltage step Δv is given by

$$\Delta v = \frac{2}{m - 1} = v_{cb}. \quad (21)$$

As $\Delta v = v_{cb}$, (21) matches with (6). Finally, since the minimum negative value of the output voltage is -1 p.u., the output voltage step l is obtained by just adding this value to the next number of voltage steps as follows:

$$v_o = \Delta v l - 1 = \frac{2}{m - 1} l - 1, \quad l = 0, 1, 2, \dots, m - 1. \quad (22)$$

For example, if $l = m - 1$ results in $v_o = 1$, as described in Fig. 25, then each term of (7) is obtained using (22).

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