

Design of flying capacitors for n -level FC and n -level SMC

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ABSTRACT

This paper presents a methodology for the design of flying capacitors for multilevel inverters. It is based on the harmonic representation of the switching functions, so that it is possible to design the flying capacitors for different operation points. Experimental results are provided to verify the presented analysis. The proposed methodology is developed for the five-level Flying Capacitor Converter and for the five-level Stacked Multicell Converter, but it can be expanded for both types of converter with a higher number of output voltage levels or for other topologies.

1. Introduction

Power electronic devices are found in many industrial and energy sectors [1–3]. In some applications with dc-ac converters, the traditional voltage-source inverter (VSI) has been losing space to multilevel inverters, due to the semiconductor's lower blocking voltage, better output waveform quality and electromagnetic compatibility. However, increased complexity and development time are some disadvantages of the multilevel inverters [4,5]. To optimize the development time and to provide good support for the hardware designer, the design of multilevel inverters must be based on a well-known theoretical background.

In the field of multilevel inverters, some topologies deserve greater attention, such as the Neutral Point Converter (NPC), the Flying Capacitor Converter (FC), the Cascaded H-Bridge Converter (CHB) and the Modular Multilevel Converter (MMC).

The NPC is widely employed by the industry in power systems and motor drives applications, due to its design simplicity and robustness [6–8].

Another topology used in power conditioners and motor drive applications is the CHB. The CHB presents an interesting structure based on series-connected H-bridge converters, which can be extended by increasing the number of such converters, consequently, increasing the number of output voltage levels. Once the design of the CHB is based on the design of H-bridge converters, well known and explored, new challenges for the CHB are related to the control strategies, in particular the power flow control [8–10].

The MMC was presented in [11] and, it has been recently explored in many works [12–14]. Its modular structure presents a great advantage in high-voltage applications, where it is possible to increase the

number of output voltage levels by increasing the number of modules, without using isolated voltage sources even for applications with active power transfer. Such characteristic allows for the operation of the MMC with low-voltage semiconductors in high-voltage applications. Therefore, due to the many researches about the MMC in the last years, its structure is consolidated and new efforts are focused on the development of new applications and control strategies [15,16].

On the other hand, the FC was introduced in [17] and, recently, it has been the work subject in many papers [18–20]. Generally, the research topic has been about new techniques to control the flying capacitor voltages, in particular, using the PS-PWM (Phase-Shift Pulse Width Modulation). Although new control techniques for the flying capacitor voltages have been studied and developed, the capacitors' design is poorly explored, specially when the FC is employed as an inverter.

Some works have presented a method to evaluate the ripple current waveforms and the voltage balancing dynamics of the flying capacitors when they are employed as an inverter [21,22]. However, they did not support a design methodology for flying capacitors in multilevel inverters.

Others works [23–27] have used the methodology proposed in [28] to design the flying capacitors in dc-ac applications. In [28] the flying capacitors are designed for a dc-dc multilevel converter. Unlike in dc-dc applications, in dc-ac converters other aspects must be considered when designing the flying capacitors, such as: the modulation scheme, the amplitude modulation index and the output current phase angle.

The capacitors used in voltage-source inverters must withstand the high ripple currents and, commonly, operations in high ambient temperature. So, disregarding the current through the capacitors can

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yield, especially when electrolytic capacitors are used due to the high series resistance (ESR) [29], a drastic lifetime reduction due to self-heating [30].

Therefore, this paper proposes a new design methodology for flying capacitors in multilevel inverters, where, aspects as: the modulation scheme, the amplitude modulation index, the output current phase angle and the number of output voltage levels are considered. However, the proposed methodology to design the flying capacitors is developed for the nL-FC and the nL-SMC (Stacked Multilevel Converter) only using the PS-PWM and the PD-PS-PWM (Phase Disposition Phase-Shift Pulse Width Modulation), respectively, under constant output loads. This way, the hardware designer has a capacitor design procedure to make the best choice from the power capacitors available in the market, reducing cost and expanding the lifetime of power capacitors, and, consequently, the power converters.

This paper is organized as follows: the converters under study are analyzed in Section 2. Sections 3 and 4 show the proposed methodology and examples to design the flying capacitors for multilevel inverters. Section 5 includes some experimental results for a single-phase five-level converter composed of three-level flying capacitor legs.

2. FC and SMC converters

2.1. Flying capacitor converters

Flying Capacitor Converters are based on the series association of chopper cells to generate n -output voltage levels, as shown in Fig. 1[17].

The only difference between the chopper cells is the voltage rating in the flying capacitors, which obey the following distribution

$$V_{C_k} = \frac{k V_{dc}}{m}, \quad (1)$$

where $k \in [1, \dots, m-1]$, m is the number of chopper cells and V_{dc} is the dc-bus voltage source. This distribution ensures that the voltages across the switches are the same for all switches of the FC, once voltage across the switches are clamped by voltages of the nearest flying capacitors. Therefore, the voltages across the switches can be given by

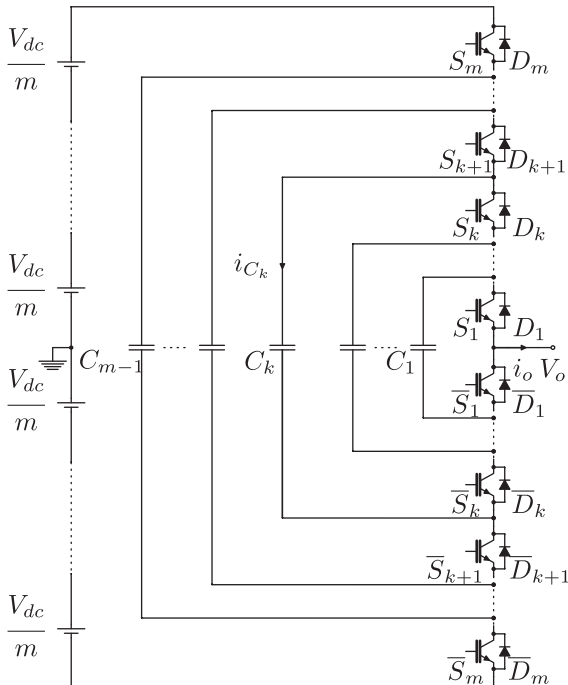


Fig. 1. nL-FC converter.

$$V_{S_k} = \frac{V_{dc}}{m}. \quad (2)$$

However, the flying capacitors are not supplied by external dc sources and, to keep their voltages stable, the average current through them must be equal to zero. The current i_{C_k} through the flying capacitor C_k is defined by the output current i_o and by the switching functions of the nearest switches, S_k and S_{k+1} , and it is given by

$$i_{C_k}(t) = [S_{k+1}(t) - S_k(t)] i_o(t). \quad (3)$$

Thus, considering that the switching period T_s is shorter than the output's fundamental period T_o , the output current can be considered constant in a switching period. Consequently, the stability condition for the FC inverter is obtained if the nearest switches have the same duty cycle D_{S_k} in a switching period. This condition can be naturally achieved by some modulation schemes, such as PS-PWM [21,31]. Due to this feature, the PS-PWM is commonly used in the FC.

2.2. Stacked multilevel converter

The SMC structure is similar to the FC structure and it can be seen as an association of the chopper converters. However, in this case, the association of chopper converters can be seen as a matrix association ($p \times q$), as shown in Fig. 2.

This new distribution of semiconductors and flying capacitors gives new characteristics to the SMC when compared to the FC, and the flying capacitor voltages can be given by:

$$V_{C_{l,k}} = \frac{k V_{dc}}{p q}, \quad (4)$$

where $k \in [1, \dots, q]$, $l \in [1, \dots, p]$, q is the number of series chopper converters and p is the number of stacked chopper converters ($p = 2$, in Fig. 2). Comparing the SMC and the FC for the same number of output voltage levels, the voltages and size of the flying capacitors are reduced in the SMC [32].

Similarly to the FC, the SMC needs to keep the flying capacitor voltages stable, ensuring the proper operation of the converter. This is possible with a suitable choice of switching states, so that the average current through the flying capacitors is maintained equal to zero. The current $i_{C_{l,k}}$ flowing through the flying capacitor $C_{l,k}$ of the SMC can be defined as:

$$i_{C_{l,k}}(t) = [S_{l,k+1}(t) - S_{l,k}(t)] i_o(t). \quad (5)$$

Fig. 3 shows the modulation scheme that maintains the flying capacitor voltages regulated, called PD-PS-PWM [33].

3. Design of the flying capacitors

One of the challenges for the hardware designer is to define the power capacitors employed in power converters, since many types and sizes are provided by different manufacturers. In addition, the application, cost and lifetime are other variables that should be considered in the project. Consequently, for the hardware designer to evaluate all those aspects and make a suitable choice, the flying capacitors' design should be based on a capacitor design procedure. For instance, the capacitor's lifetime is directly linked with the current rms value, while the correct estimation of the capacitors' capacitance and voltage operation ensures a safe and proper operation of the inverter. Another way to estimate a capacitors' capacitance and rms current is by simulation. However, sometimes, the simulation takes a lot of time to evaluate all critical operational points of the inverter, and even result in a wrong estimation such points and, consequently, of the capacitor's parameters.

In the next steps, a capacitor design procedure is developed to design the flying capacitors for multilevel inverters, considering aspects such as the amplitude modulation index and the output load. In most

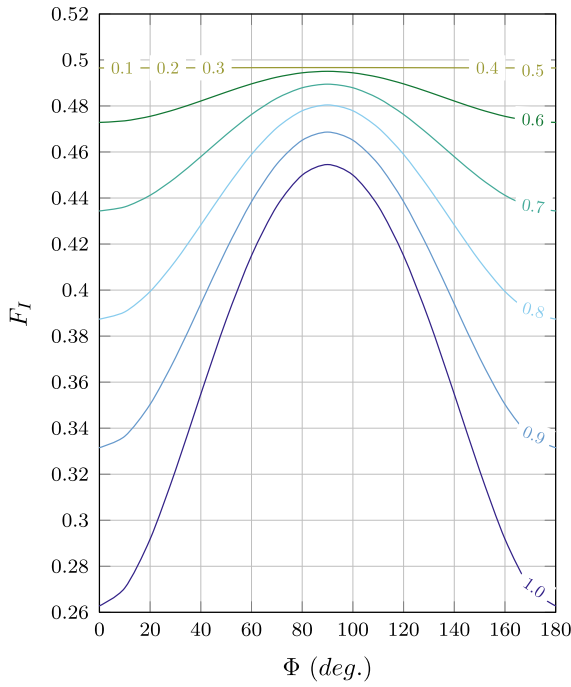
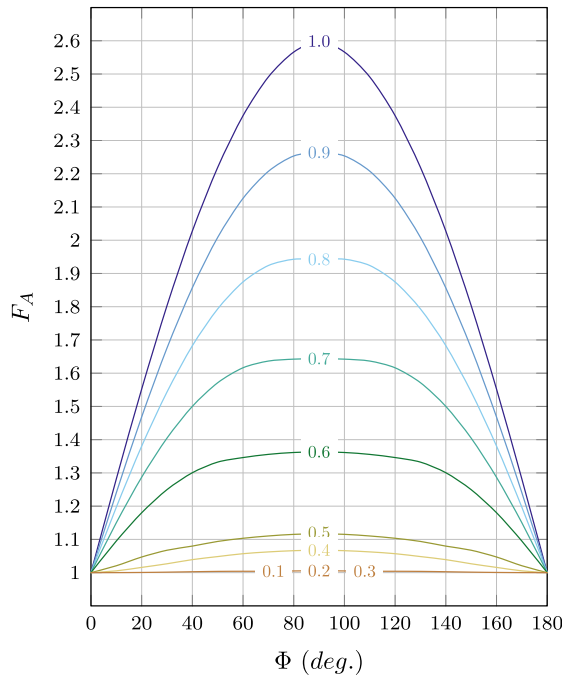


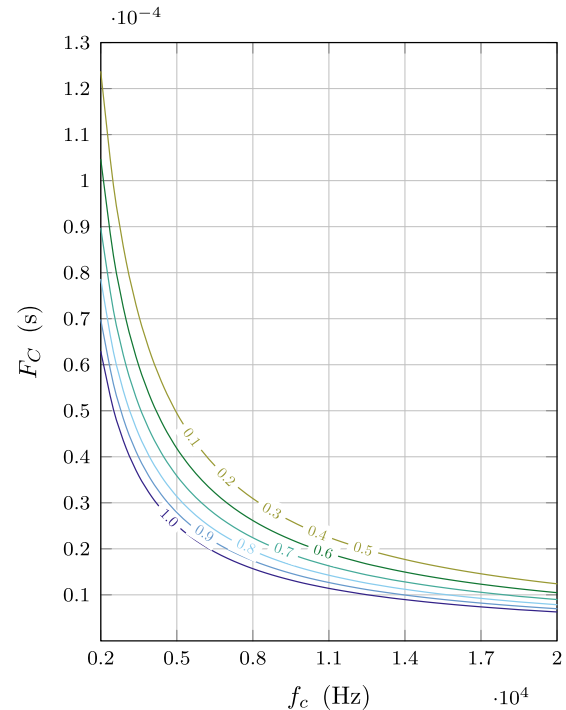
Fig. 4. Current factor correction of the flying capacitor as a function of the phase angle and amplitude modulation index.

where R_{ESR} is the equivalent series resistance of the capacitor, F_A is the phase angle factor correction, given in Fig. 5(a), and F_C is the carrier frequency factor correction, presented in Fig. 5(b).

Regarding the graphics presented in Fig. 4 and in Fig. 5 are restricted to five-level FC (5L-FC), and others graphics can be drawn from (12) and (14), allowing the design of flying capacitors to n -level FCs (n L-FC).



(a)



(b)

Fig. 5. (a) Phase angle factor correction as a function of the phase angle and amplitude modulation index and (b) Carrier frequency factor correction as a function of the carriers frequency and amplitude modulation index, for the FL-SMC.

3.2. Expanding the design of the flying capacitors for others converters

The same design methodology can be extended for others topologies employing flying capacitors, such as the SMC. This design methodology for the flying capacitors can be divided into three steps.

The **first step** is to define the equation that represents the behavior of the current through the flying capacitors. For the SMC, such behavior is given by (5).

The **second step** is to compute the harmonic representation of the switching functions using double Fourier series. For the SMC with PD-PS-PWM, the switching functions can be generalized, and are given by:

$$S_{l,k}(t) = \frac{C_{00}}{2} + C_{0h} \cos[h(\omega_o t + \theta_o)] + C_{g0} \cos[g(\omega_c t + \theta_{c,k})] + \sum_{g=1}^{\infty} \sum_{h=-\infty}^{\infty} C_{gh} \cos[g(\omega_c t + \theta_{c,k}) + h(\omega_o t + \theta_o)]. \quad (16)$$

Once the double Fourier integral is evaluated, one can observe that the harmonic magnitudes for the SMC are:

$$C_{00} = \frac{2M_a}{\pi}, \quad (17)$$

$$C_{0h} = M_a \left\{ \frac{1}{2} \Big|_{h=1} + \frac{1}{\pi} \left[\frac{\sin\left[\frac{(h+1)\pi}{2}\right]}{h+1} + \frac{\sin\left[\frac{(h-1)\pi}{2}\right]}{h-1} \right] \Big|_{h>1} \right\}, \quad (18)$$

$$C_{g0} = \frac{4}{g\pi^2} \sum_{u=1}^{\infty} \left[\frac{J_{2u-1}(M_a g \pi)}{2u-1} \right], \quad (19)$$

$$C_{gh} = \frac{2}{g \pi^2} \sum_{u=1}^{\infty} \left\{ \times \left\{ \frac{\sin\left[\frac{(u+h)\pi}{2}\right]}{u+h} \Big|_{\substack{h \neq -u, \\ h \neq u}} + \frac{\sin\left[\frac{(u-h)\pi}{2}\right]}{u-h} \Big|_{\substack{h \neq -u, \\ h \neq u}} + \frac{\pi}{2} \Big|_{h=\pm u} \right\} \right\} \quad (20)$$

The current flowing through the flying capacitors can be obtained by replacing (16) in (5), so that:

$$i_{C_{l,k}}(t) = I_p \sin(\omega_o t - \Phi) \times \left\{ C_{g0} \{ \cos[g(\omega_c t + \theta_{c,k+1})] - \cos[g(\omega_c t + \theta_{c,k})] \} + \sum_{g=1}^{\infty} \sum_{h=-\infty}^{\infty} C_{gh} \left\{ \cos[g(\omega_c t + \theta_{c,k+1}) + h(\omega_o t + \theta_o)] - \cos[g(\omega_c t + \theta_{c,k}) + h(\omega_o t + \theta_o)] \right\} \right\} \quad (21)$$

The capacitance of the flying capacitors is obtained by

$$i_{C_{l,k}}(t) = C_{l,k} \frac{dv_{C_{l,k}}(t)}{dt} \quad (22)$$

The **third step** is to build graphics for the design of the flying capacitors. The graphics are generated by numerical analyses, due to the complexity mathematical operations of the Eqs. (21) and (22). All this process is made by software and the flowchart is presented in the Fig. 6.

The process consists of the parameter sweep of the amplitude modulation index M_a , switching frequency f_c and phase angle Φ , while the parameters I_p and $\Delta V_{C_{l,k}}$ are normalized in unitary values. The data result of numeric analyses of either $I_{C_{l,k}rms}$ or $C_{l,k}$ results in graphics of the factor corrections.

Thus, by following the above steps the graphics for the 5L-SMC using the PD-PS-PWM are obtained.

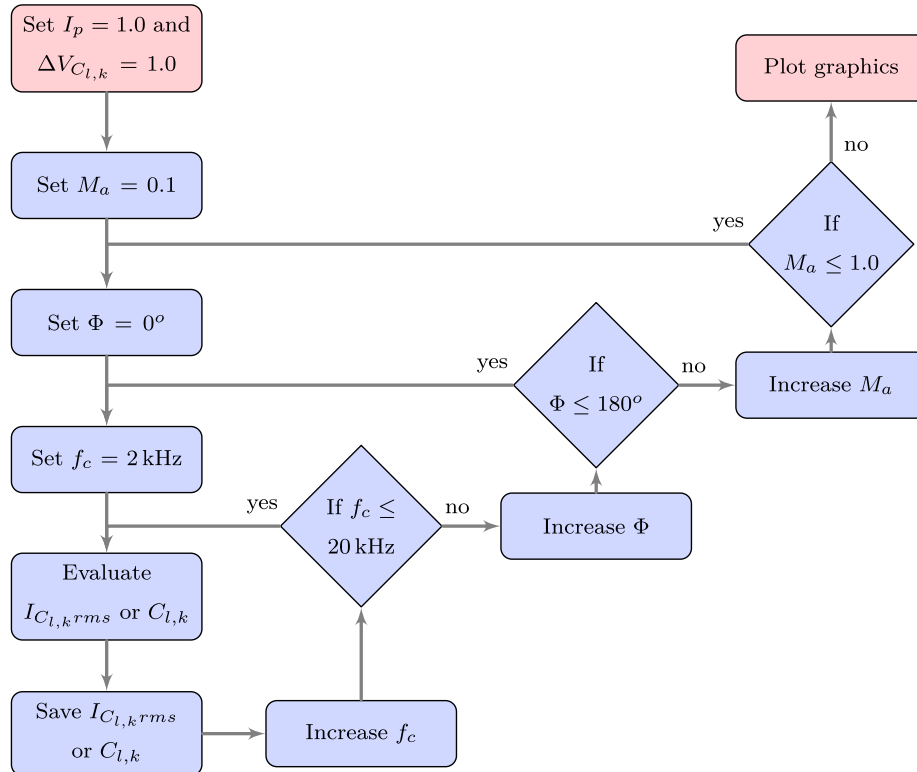


Fig. 6. Flowchart of the building process of the correction factors graphics.

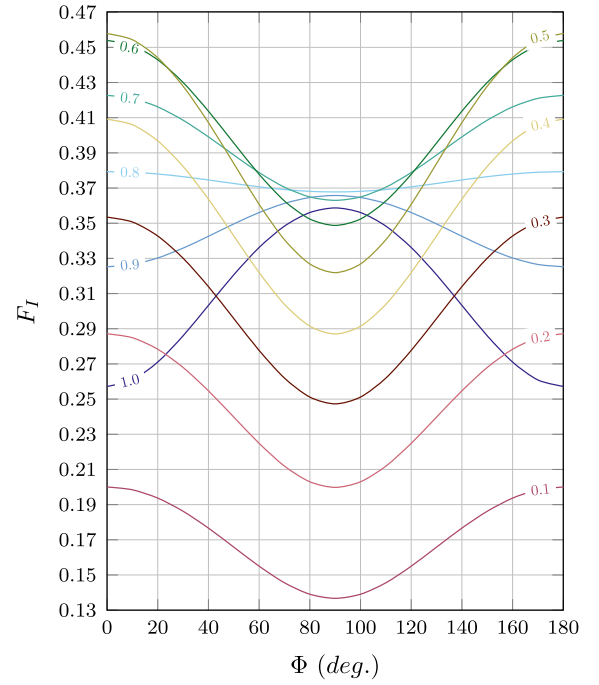


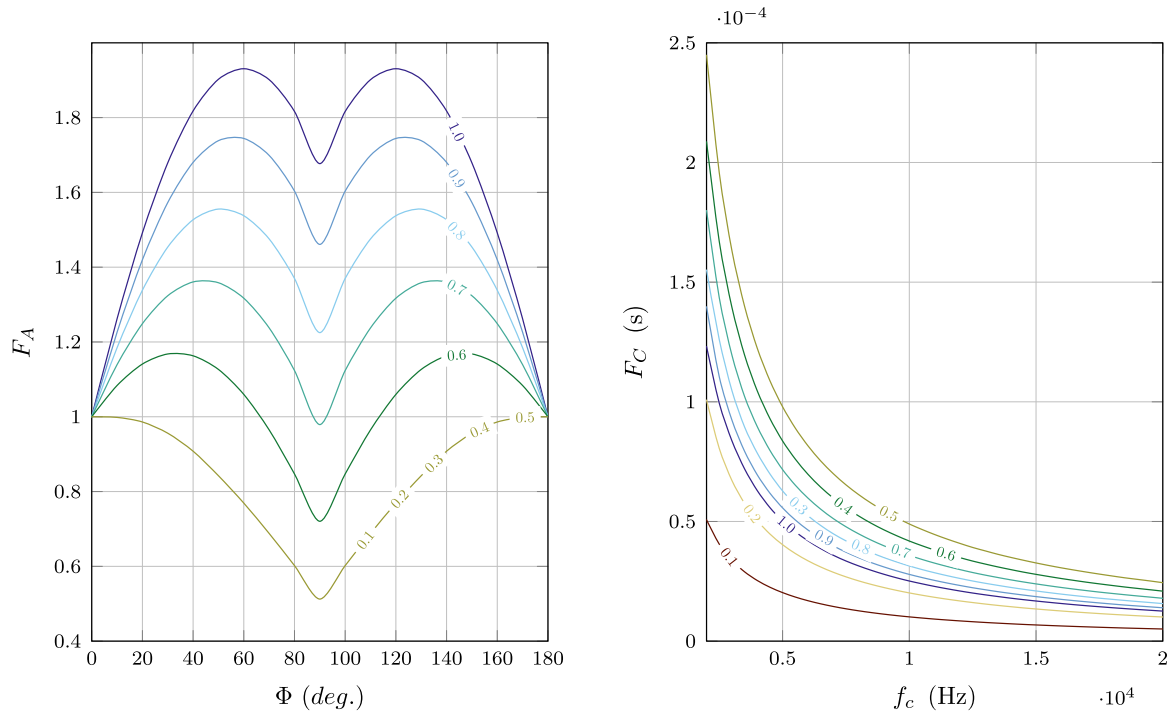
Fig. 7. Current factor correction of the flying capacitor as a function of the phase angle and amplitude index modulation, for the 5L-SMC 2×2 .

The current rms value in the flying capacitor is given by

$$I_{C_{l,k}rms} = I_p F_I. \quad (23)$$

where F_I is the current factor of the flying capacitor and it is shown in Fig. 7.

The capacitance value of the flying capacitors is defined by



(a) Phase angle factor correction as a function of the phase angle and amplitude modulation index. (b) Carrier frequency factor correction as a function of the carriers frequency and amplitude modulation index.

Fig. 8. Phase angle factor and carrier frequency factor correction for the 5L-SMC 2×2 .

$$C_{l,k} = \frac{I_p F_A F_C}{\Delta V_{C_k} - 2 I_p R_{ESR}}, \quad (24)$$

where the phase angle factor correction F_A and the carrier frequency factor correction F_{Ck} can be determined from Fig. 8 (a) and (b), respectively.

The presented graphics enable the design of the flying capacitors for the 5L-SMC. For SMCs with more output voltage levels, or for other converters, new graphics can be made following the steps above.

4. Design examples

In this section, the proposed methodology to design the flying capacitors is verified and compared with the methodology presented in [28]. The design examples are for the 5L-FC, utilizing the PS-PWM, for different operating points, as shown in Table 1.

For the classic design of the flying capacitors, some variables are considered, such as the voltage ripple of the flying capacitors ΔV_{C_k} , the

number of output voltage levels n , the maximum output current I_p and the carrier frequency f_c . Thus, for the Design 1 the capacitance value is given by

$$C_k = \frac{I_p}{(n-1)\Delta V_{C_k} f_c} = \frac{6.428}{4 \cdot 5 \cdot 2000} = 160.7 \mu\text{F}, \quad (25)$$

for others operating points the capacitance are presented in Table 1. Due to the simplicity of the design methodology presented in [28], some important variables are disregarded, such as the amplitude modulation index and the output phase angle, which can result in the oversizing or undersizing of the flying capacitors.

On the other hand, by using the proposed design methodology, the rms value of the capacitor currents can be obtained from (13) and Fig. 4. Considering the design parameters shown in Table 1, the rms value of the capacitor currents for the Design 1 is given by

$$I_{C_{k,rms}} = I_p F_I = 6.428 \cdot 0.435 = 2.8 \text{ A}, \quad (26)$$

Table 1
Design operation points for the 5L-FC.

Systems Parameters	Design 1	Design 2	Design 3	Design 4
dc voltage source	$V_{dc} = 400 \text{ V}$	$V_{dc} = 400 \text{ V}$	$V_{dc} = 400 \text{ V}$	$V_{dc} = 400 \text{ V}$
Flying cap. volt. ripple	$\Delta V_{C_k} = 5 \text{ V}$	$\Delta V_{C_k} = 5 \text{ V}$	$\Delta V_{C_k} = 10 \text{ V}$	$\Delta V_{C_k} = 10 \text{ V}$
Output peak current	$I_p = 6.428 \text{ A}$	$I_p = 6.428 \text{ A}$	$I_p = 6.428 \text{ A}$	$I_p = 6.428 \text{ A}$
Output frequency	$f_o = 50 \text{ Hz}$	$f_o = 50 \text{ Hz}$	$f_o = 50 \text{ Hz}$	$f_o = 50 \text{ Hz}$
Carrier frequency	$f_c = 2 \text{ kHz}$	$f_c = 2 \text{ kHz}$	$f_c = 2 \text{ kHz}$	$f_c = 2 \text{ kHz}$
Modulation index	$M_a = 0.7$	$M_a = 0.9$	$M_a = 0.7$	$M_a = 0.9$
Phase angle	$\Phi = 0^\circ$	$\Phi = 90^\circ$	$\Phi = 30^\circ$	$\Phi = 70^\circ$
Flying cap. ESR	$R_{ESR} = 0 \Omega$	$R_{ESR} = 120 \text{ m}\Omega$	$R_{ESR} = 120 \text{ m}\Omega$	$R_{ESR} = 120 \text{ m}\Omega$
Classic design	$C_k = 160.7 \mu\text{F}$	$C_k = 160.7 \mu\text{F}$	$C_k = 80.3 \mu\text{F}$	$C_k = 80.3 \mu\text{F}$
Proposed design	$C_k = 113.1 \mu\text{F}$	$C_k = 294.1 \mu\text{F}$	$C_k = 93.6 \mu\text{F}$	$C_k = 113.6 \mu\text{F}$

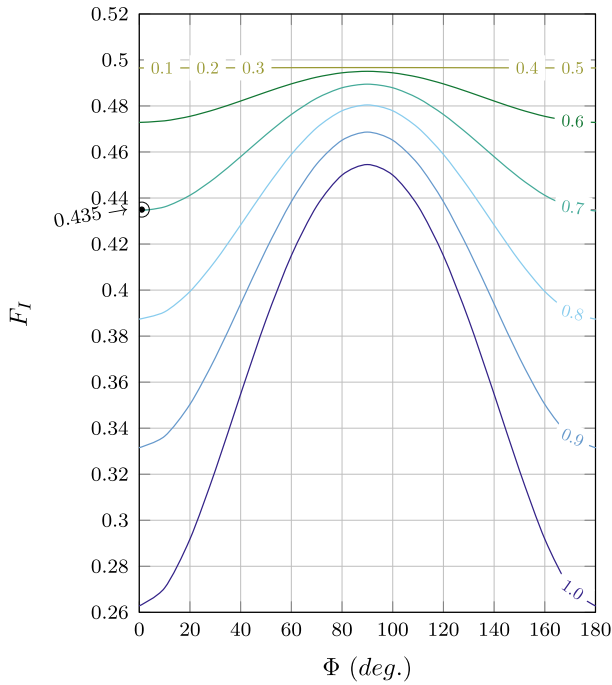


Fig. 9. Current factor correction of the flying capacitor for the design examples of the 5L-FC.

where FI is obtained as illustrated in Fig. 9.

Similarly, the capacitance value can be computed from (15) and Fig. 5 (a) and (b). Therefore, the capacitance value for the Design 1 is given by

$$C_k = \frac{I_p F_A F_C}{\Delta V_{C_k} - 2 I_p R_{ESR}} = \frac{6.428 \cdot 1.88 \times 10^{-5}}{5 - 2 \cdot 6.428 \cdot 0} = 113.1 \mu\text{F}. \quad (27)$$

As expected, the two design of the flying capacitors result in distinct capacitance values, as shown in Table 1. These different results evidence that the flying capacitors are oversizing or undersizing and used a wrong methodology of design of the flying capacitors. Thus, experimental results are obtained to clarify the differences of the two design methodology.

5. Experimental results

The theoretical analysis presented in this paper has been validated with experimental results that have been obtained from the 5L-FC-FC. The PS-PWM employed for the 5L-FC-FC is identical to the PS-PWM for the 5L-FC, enabling that the graphics obtained for the 5L-FC can be used for the 5L-FC-FC. The circuit of the 5L-FC-FC is presented in Fig. 10.

Table 2 presents the parameters of the 5L-FC-FC prototype.

The dc voltage supply and the flying capacitors of the prototype are composed of electrolytic capacitors. The capacitors of the dc voltage supply are manufactured by EPCOS, model B43503-S5477-M91.

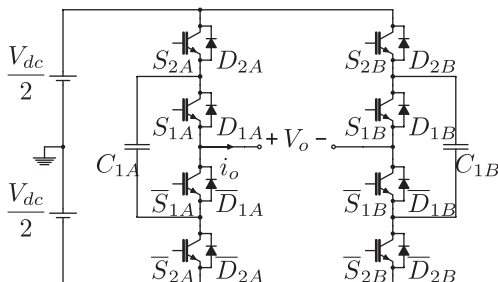


Fig. 10. Five-level full-bridge flying capacitor converter (5L-FC-FC).

Table 2

Parameters of the 5L-FC-FC prototype.

Prototype Parameters	
dc voltage source	$V_{dc} = 400 \text{ V}$
Output frequency	$f_o = 50 \text{ Hz}$
Carrier frequency	$f_c = 2 \text{ kHz}$
Flying capacitors rating	$C_k = 120 \mu\text{F}$
Flying capacitor voltages	$V_{C_k} = 200 \text{ V}$
Flying cap. ESR	$R_{ESR} = 120 \text{ m}\Omega$

Electrolytic capacitors manufactured by Nichicon, model LGW2W121MELZ35, are used for the flying capacitors. The electrolytic capacitors ensure the safe operation for voltages up to 450 V and rated capacitance is 470 μF for the model B43503-S5477-M91, and 120 μF for model LGW2W121MELZ35. The semiconductors employed in the prototype are developed by International Rectifier, model IRGP50B60PD1. The semiconductors are rated for 600 V and 33 A.

An active voltage balancing strategy to control the flying capacitors' voltages is used to keep them in the steady-state, ensuring the safe operation of the 5L-FC-FC. The active voltage balancing strategy was presented in [35], called *Modified M Method*. It is applied to avoid imbalances in the flying capacitor voltages that can be generated by the delay and dead-time switching commands and to improve the response at transient loads. Thus, this little variation in modulation signals are negligible when the inverter operates in steady-state conditions and it does not interfere in the proposed design methodology. The design of the active control is not the main focus of interest, therefore, it will not be introduced in this paper.

The active voltage balancing strategy was accomplished with a DSP, model TMS320F28379D, as well as the PS-PWM.

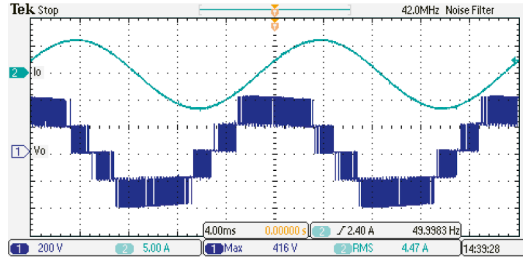
Fig. 11 shows the output voltage and current of the 5L-FC-FC operating with $M_a = 0.9$ and $\Phi = 67^\circ$ in steady-state conditions. A five-level voltage waveform can be observed, and the output current presents low ripple due to the high inductance at the output load. In steady-state conditions, the voltage ripple of the flying capacitors is 9.4 V and the average voltage is 200 V. The current rms value in the flying capacitors is 2.85 A and the current average value is negligible. The results ensure the correct operation of the 5L-FC-FC with the active voltage balancing strategy, keeping the capacitor voltages within the nominal ratings.

These operating conditions and the voltage ripple of the flying capacitors are similar of the "Design 4", in Table 1, where the design of the flying capacitor for the proposed methodology the capacitance value of the flying capacitors are the $C_k = 113.6 \mu\text{F}$ close to the capacitance value of $C_k = 120 \mu\text{F}$ in the prototype. This result shows the divergence of the two design methodologies, once the classic design methodology the capacitance value is the $C_k = 80.3 \mu\text{F}$.

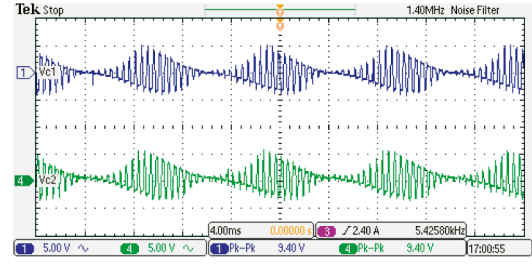
Thus, it is possible to get results for others operating points of the inverter evaluating all range of the proposed design methodology. Fig. 12 shows the experimental results for the current factor correction of the flying capacitor for different inverter operation parameters and output loads, which were obtained from measuring the output and the flying capacitor current, and through analysis by computer software.

The experimental results are in the agreement with current factor correction in the flying capacitors, for the entire range of the modulation index M_a , the output phase angle Φ and the carrier frequency f_c . Moreover, Fig. 13 shows the experimental results for the phase angle factor correction for different amplitude modulation indices, output loads and carrier frequencies. The experimental results were obtained from measuring the output current and the flying capacitors' voltages.

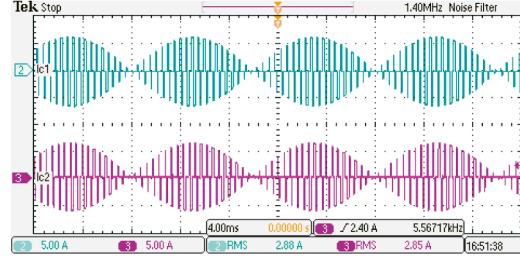
In Fig. 13, the results show small differences between the phase angle factor correction and the experimental results, which are explained by the measuring disturbances of the voltage ripple in the flying capacitors, which turn the measured noise into a source of imprecision.



(a) Output voltage $V_o(t)$ and output current $i_o(t)$.



(b) Flying capacitor voltages $V_{C_k}(t)$.



(c) Flying capacitor currents $i_{C_k}(t)$.

Fig. 11. Experimental results for the 5L-FC-FC, with $M_a = 0.9$ and $\Phi = 67^\circ$.

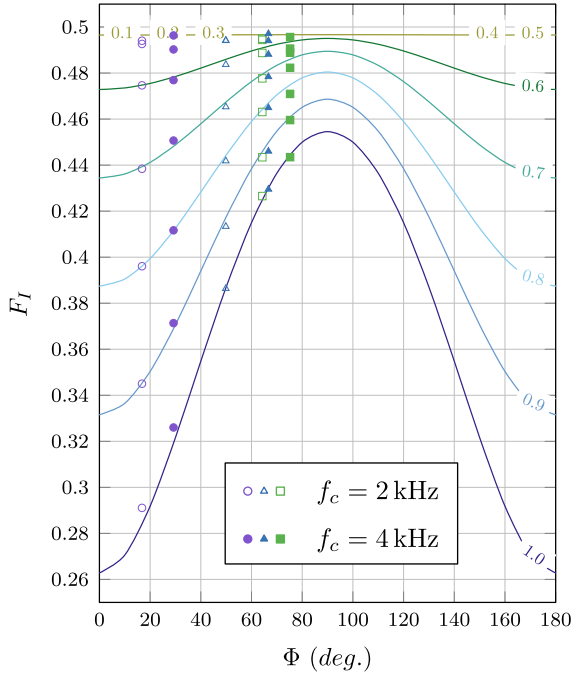


Fig. 12. Experimental results of the current factor correction of the flying capacitor as a function of the phase angle and amplitude modulation index using different loads.

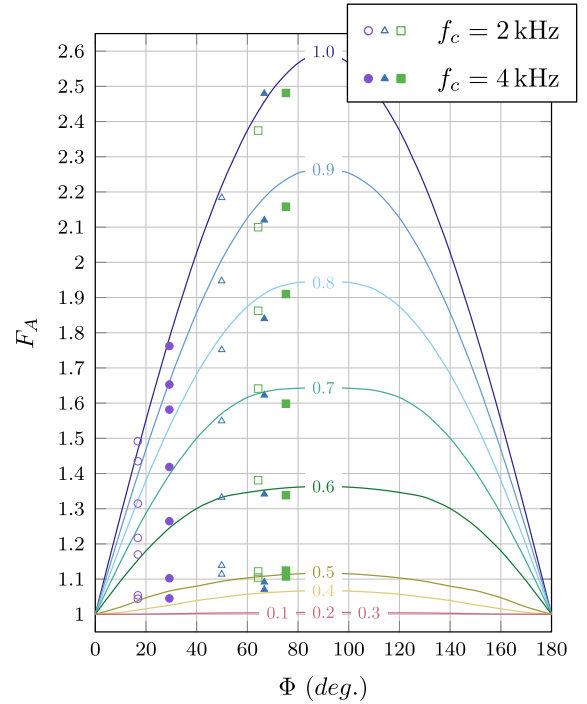


Fig. 13. Experimental results of the phase angle factor correction as a function of the output phase angle and amplitude modulation index using different loads.

6. Conclusion

This paper proposed a methodology to design flying capacitors for n-levels FC and SMC converters, using the double Fourier series representation of the inverter switching functions to describe the behavior of the near switches of the flying capacitors and, thereafter, the current through. This result allows the development of graphics for the design of flying capacitors. The methodology presented in this work can be expanded for all topologies employing flying capacitors in

structures.

The methodology was validated with experimental results for the 5L-FC-FC. Those good results confirm that the design of flying capacitors can be performed for different operation points of the multilevel inverter, e.g., the number of the output voltages levels, the output load and the amplitude index modulation.

The design of flying capacitors for the FC and the SMC using graphics has proven to be a good alternative, once other design

methodologies are limited and presents imprecise results due to they don't considered the output phase angle and amplitude index modulation. Therefore, the proposed methodology is only applied for the PS-PWM modulation and similar.

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Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at <https://doi.org/10.1016/j.jepes.2019.05.030>.

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