

A Control Strategy for a Series APF With Critical-Load-Bus Voltage Feedback That Avoids Injection Transformer Saturation

Guilherme da Silva Fischer¹, Alisson Mengatto², Luís Gustavo Kremer, and Marcello Mezaroba³, *Member, IEEE*

Abstract—Series active power filters (APF) are an important solution to deal with power quality issues in weak grids under the presence of non-linear loads. The use of voltage feedback from the critical-load-bus (cload-bus) in the series APF allows for a control strategy that has performance and processing power advantages, when compared to other strategies in literature, but can cause saturation of injection transformers. This paper presents a control strategy that uses cload-bus voltage feedback with an additional control loop of the dc current in the output of the series APF voltage source converter (VSC), to avoid injection transformer saturation. The controlled dc current is additionally used for balancing the split dc-bus capacitors voltage in the VSC. The series APF and the proposed control strategy are modeled using small signal analysis for allowing controller design. Experimental results from a 3 kVA prototype are presented, with cload-bus voltage total harmonic distortion improving from 9% to 3% in each phase, while achieving the objectives of improved cload voltage waveform, controlled transformer dc current, and balanced dc-bus capacitors voltage.

Index Terms—Control design, harmonic distortion, power conditioner, series active power filter (APF).

I. INTRODUCTION

DUE to increasing number of power electronic devices connected to the low voltage distribution network, non-linear currents with high harmonic content have become more present in the electrical grid. Consequently, if compensation techniques are not used, the point of common coupling (PCC) will supply distorted voltages affecting the operation of loads.

In developed countries, most of power electronics equipments have improved their input current quality and currently does not present serious problems related to harmonics. In other hand, in some less developed countries, the regulations about power factor and harmonics are less strict, so current and voltage harmonics still are present in the distribution grids, causing a lot of issues in loads operation.

Manuscript received May 10, 2018; revised September 20, 2018; accepted November 30, 2018. Date of publication December 14, 2018; date of current version April 20, 2019. Paper 2018-PSEC-0442.R1, presented at the 2017 Brazilian Power Electronics Conference (COBEP), Juiz de Fora, Brazil, Nov. 19–22, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Power Systems Engineering Committee of the IEEE Industry Applications Society. (Corresponding author: Marcello Mezaroba.)

The authors are with the Electric Power Processing Group, Santa Catarina State University, Joinville 89219710, Brazil (e-mail: guilherme.silva.fischer@gmail.com; alisson_mengatto@hotmail.com; lgkremer@hotmail.com; marcello.mezaroba@udesc.br).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TIA.2018.2886769

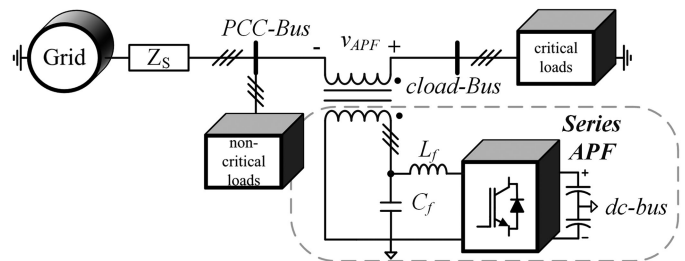


Fig. 1. Conventional series APF structure.

A power quality conditioner can be used to improve the voltage delivered to these loads. The conditioner is usually connected to the PCC, with other non-loads, and creates an additional bus, the cload-bus, with improved power quality.

Among the active power quality conditioners applied to mitigate voltage disturbances, the voltage controlled series active power filter (APF) [1], with an appropriate control scheme, ensures low voltage distortion at the cload-bus even when non-linear loads are connected or the supplied grid voltage is already distorted. The series APF can also be used to balance phase voltages in three-phase systems and to compensate sags and swells.

As illustrated in Fig. 1, the conventional series APF structure connects a voltage source converter (VSC), by means of an injection transformer, in series from the PCC-bus to the cload-bus. Compensation of the cload-bus voltage is realized by injecting harmonic voltage components in opposite phase with the distorted PCC-bus voltage. In steady state, there is only transfer of reactive power between the VSC and the load-bus, with a small parcel of active power being absorbed to compensate the VSC losses. Furthermore, if there is three phase voltage unbalance, the series APF can absorb power in one phase and deliver it to another, even during steady state, achieving voltage balance at the loads. To compensate sags and swells, other than an adequate control strategy, the series APF requires energy storage capacity, to either supply or absorb energy during the sag/swell without reaching the limits of dc-bus voltage required for its operation. Another alternative to improve load voltages are dynamic voltage restorers (DVR) [2] and unified power-quality conditioners (UPQC) [3]. DVR are not concerned with steady-state regulation and are attractive to handle voltage sags/swells. UPQC compensates both voltage and current harmonics in a cascaded shunt and series APF with a shared dc bus.

The conventional abc frame control strategy for the voltage controlled series APF provides pure sinusoidal voltage to the loads indirectly, by extracting the fundamental and harmonic components of the PCC-bus voltage to generate counter harmonics as references for the VSC output voltage [4]–[6]. However, additional low-or high-pass filters are necessary to separate the fundamental voltage component, which increases computational efforts and adds an extra time delay which may deteriorate the compensation performance [7]. Other control schemes use $\alpha\beta$ transformation to separate the negative and positive sequences [8] and dq0 reference frame [9] to transform sinusoidal to dc variables. However, additional filters are necessary and computational effort is increased by the reference frame transformation.

When using a coupling transformer with these control technique, if the feedback voltage is placed on converter side (henceforth referred as primary transformer side), it does not eliminate disturbances caused by the transformer, such as voltage drops in the leakage inductance, and there is no guarantee that the load voltage is well compensated. If the voltage is measured at the secondary of the transformer, an undesirable dc voltage at the VSC output would not be seen due to the dc blocking nature of transformers, and could destabilize the voltage controller. Few works are proposed in the literature treating the transformer dc current control for APFs [10]. Transformerless applications [5] are much more costly in three-phase applications as they require three single-phase converters with three independent dc sources.

The control strategy presented in this paper acts in the clod-bus voltage directly as in [3] and [11], ensuring that the voltage is regulated by placing the feedback voltage sensor at load side, but an additional primary side dc current control loop is integrated to provide system stability with respect to injection transformer saturation. To design the controller for the proposed strategy, the dynamics of the injection transformer are considered in the development of the small signal models. The controlled dc current is also used to achieve balanced dc-bus capacitors voltage in split capacitor VSC. Experimental results verify the functionality of the control scheme, as the 3 kVA prototype is capable of providing balanced sinusoidal clod-bus voltages with low total harmonic distortion (THD) when supplying linear and non-linear loads, while keeping dc currents to a minimum and the dc-bus voltages balanced. This strategy for avoiding transformer saturation is also applicable to other converters with series injection and clod side feedback, such as DVR and UPQC. Furthermore, the controlled primary side dc current can also be used for balancing the voltage of the dc bus in series APF that uses split dc-bus capacitor. This control strategy was first introduced in the work presented in [12] but only validated with simulation results.

In addition to controlling the clod-bus voltage, series APF requires control of the dc-bus voltage to achieve good performance. Schemes to create the dc-bus voltage using the load itself in applications with rectifiers [13] or using a separate low power diode bridge rectifier [14] are reported in literature; however, added hardware costs are a drawback of these solutions. Several different dc-bus voltage control schemes exist for power conditioners. In UPQCs [3], [15], the dc-bus voltage is controlled by

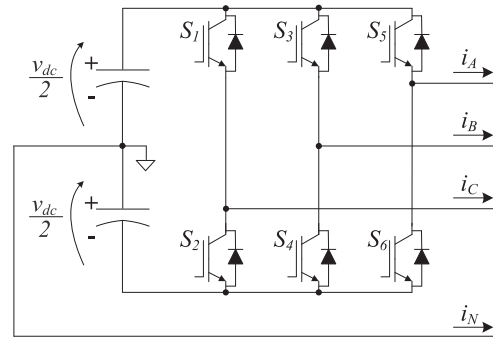


Fig. 2. Three-phase, four wire, split capacitor VSC.

the shunt APF. Using the “pq” theory, the active power absorbed by the series APF can be directly controlled without utilizing other power electronics equipment or dc sources [16]. In [4], the dc-bus voltage control strategy for a series APF is established as a voltage drop in the fundamental frequency in phase with the source voltage, and its model is proposed by average instantaneous values at the switching frequency. Another possibility is to create a voltage drop synchronized with the load current in the fundamental frequency so that the series APF is seen as a resistor in series with the load. It is also possible to control the dc-bus voltage while injecting reactive power at the fundamental frequency, regulating the load voltage within limits that are imposed by the load power factor, similarly to DVR [2]. The solution proposed in [4], and extended in [17] to consider the influence of the system load, is used in this paper for its simplicity.

II. DISTRIBUTION SYSTEM AND COMPENSATOR TOPOLOGY

The typical low-voltage power distribution in Brazil is composed by a three-phase Δ -Y transformer providing a grounded neutral conductor. Typical loads connected to this three-phase, four wire (3P4W) power system are adjustable speed drives, electric furnaces, lighting ballasts, office equipment, and other facilities with power electronics. These loads can have input current with high harmonic content, which causes voltage distortion at the PCC, and may be either single-phase or three-phase, causing voltage unbalance (different fundamental amplitude) across the three phases. This configuration of distribution line constitutes a non-symmetrical system where three independent variables exist, that is, the sum of the instantaneous value of phase voltages can be different than zero.

To compensate each voltage independently, the series APF requires a three-phase inverter with a neutral connection. The three-phase two-level VSC topology with split dc-bus capacitor, in Fig. 2, is the simplest converter to compensate voltages independently in each phase. This topology can be seen as three independent half-bridge converters with a shared dc bus. The neutral conductor forms a return path and flows current through the midpoint of the two capacitors so each phase can generate fully independent compensation voltages. The shared dc bus allows power transfer between phases, which allows for compensation of unbalances in the phase voltages.

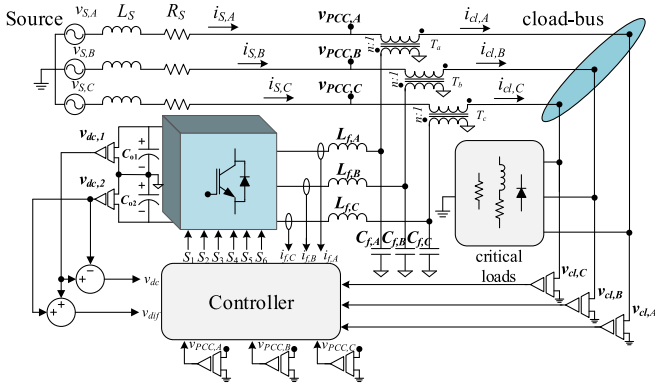


Fig. 3. General diagram of the series APF.

In the split capacitor VSC, unbalanced phase voltages cause ripple in the dc-bus voltage unbalance (voltage difference between the split capacitors), as the neutral conductor instantaneous current is not zero. This is not a problem with a properly sized dc-bus capacitance. However, the neutral conductor current cannot have a dc component in steady-state, as it would fully discharge one of the capacitors. Equal voltages across two capacitors is desirable to maximize the output voltage that can be achieved without over-modulation. Balanced dc capacitors also maximize the energy storage capacity of the dc bus for a given maximum capacitor voltage. Even if a certain amount of voltage unbalance is acceptable, this behavior can be unstable (i.e., the unbalance voltage diverges), and is hard to predict in the design phase of the converter and maintain during its lifetime. The voltage unbalance can be compensated by controlling the neutral current of the converter; however, the neutral current is

$$i_N = i_A + i_B + i_C \quad (1)$$

and the dc output current in each phase can have different polarities. Therefore, high dc current, with opposite polarities, can be seen in two phases, while the neutral dc current is zero, causing transformer saturation. Therefore, a better solution is to independently control each phase dc output current, indirectly controlling the neutral current, achieving dc-bus voltage balance, and preventing injection transformer saturation.

Another alternative power circuit topology is the four-leg VSC topology, where the neutral conductor is directly controlled [18]. By adding this extra leg there is no need to split the capacitors and unbalance control is unnecessary; however, the overall cost and complexity of the fourth leg approach is a drawback, as it requires a controller for the fourth leg, and additional switching elements. Furthermore, the four-leg VSC topology does not eliminate the problem of dc output current saturating the transformers, and still requires the control of phase dc output current proposed in this paper.

Therefore, in this paper, the proposed series APF is composed of a split capacitor 3P4W converter and an output filter. Three single-phase transformers are used to connect the series APF from the utility grid to load-bus as shown in Fig. 3. No PCC-bus loads are shown for simplicity. By measuring the load

voltages (v_{cl}), dc-bus voltages (v_{dc}), and inductor filter currents (i_f), the proposed control strategy can provide pulsewidth modulation (PWM) signals to the converter to achieve satisfactory voltage quality at the load-bus. PCC-bus voltage (v_{PCC}) is also measured to synchronize the load-bus voltage reference.

III. SERIES APF CONTROL STRATEGY

The block diagram of the proposed control strategy for a 3P4W series APF with split dc-bus capacitors is presented in Fig. 4. It is composed of two external control loops, which controls dc-bus total voltage and dc-bus voltage unbalance, and two internal control loops (repeated for each phase), which controls the dc output current and load-bus voltage. The controllers are $C_{v,cl}(s)$, one for each load-bus voltage, $C_{i,f}$, one for each dc output current, C_{dif} for the dc-bus voltage unbalance, and C_{dc} for the total dc-bus voltage. Sensors are represented by blocks $h_{v,cl}$, $h_{i,f}$, h_{dif} , and h_{dc} , for the load-bus voltage, dc output current, dc-bus voltage unbalance, and dc-bus total voltage, respectively.

The inverter PWM gain is represented by block G_{PWM} , and small signal models representing the dc-bus voltage unbalance as a function of dc-output current [$V_{dif}(s)/i_f(s)$], dc-bus total voltage as a function of load-bus voltage [$v_{dc}(s)/v_{cl}(s)$], output current of the inverter (before the coupling transformer) as a function of the duty ratio, [$i_f(s)/d(s)$], and load-bus voltage (after the coupling transformer) as a function of the output current [$v_{cl}(s)/i_f(s)$], are also used.

A. Control of Load-Bus Voltage

The load-bus voltage v_{cl} is directly controlled by the innermost control loop, formed by $C_{v,cl}$, G_{PWM} , $h_{v,cl}$, i_f/d , and v_{cl}/i_f . The reference for the load-voltage controller is generated by a PLL, and is purely sinusoidal, with amplitude defined by the dc-bus voltage control loop. This strategy avoids the power calculation and harmonic extraction required in other control strategies. The harmonics in load voltage cause an error in the input of controller $C_{v,cl}$, which acts on the duty ratio to track the sinusoidal reference. The branch in the control loop at i_f is not considered in the load-bus voltage design, and the dc-current control loop should be designed to not affect the load-bus voltage loop. Therefore, the load-bus control loop can be simplified to the same as in [11], where the converter duty ratio is set by $C_{v,cl}$ as to control the load-bus voltage at line frequency and its harmonics.

B. Control of DC Output Current

Each phase also has a dc output current control loop. The dc output current of the inverter, measured before the transformer, is compared with its reference i_f^* , compensated by the controller $C_{i,f}$, and given as a dc-voltage reference to the load-bus control loop. This strategy is designed due to the dc-blocking nature of the coupling transformer. As an example, a simplified block diagram of the series APF control with load-bus side feedback is shown in Fig. 5. The dc offset error, v_{off} , of the voltage sensor $h_{v,cl}$, could cause a dc error in the input of controller

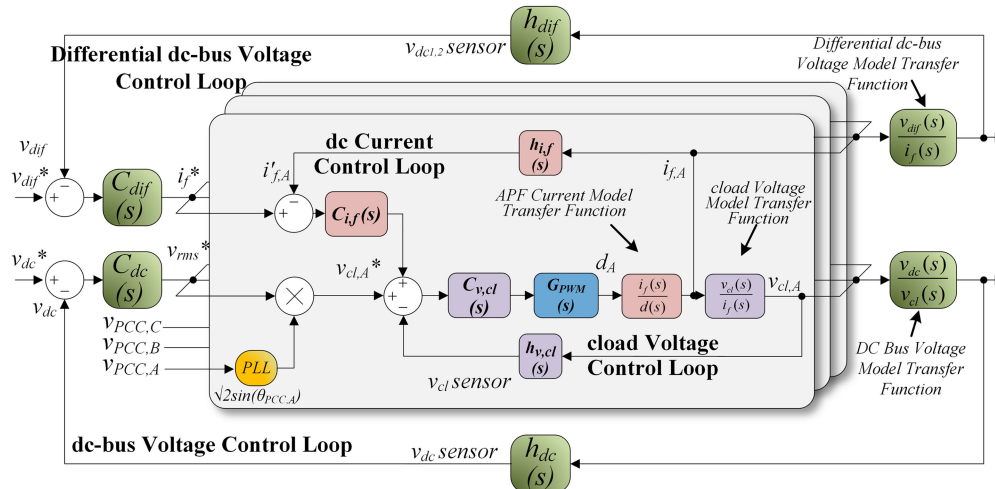


Fig. 4. Block diagram of the series APF control strategy including the representation of small signal models.

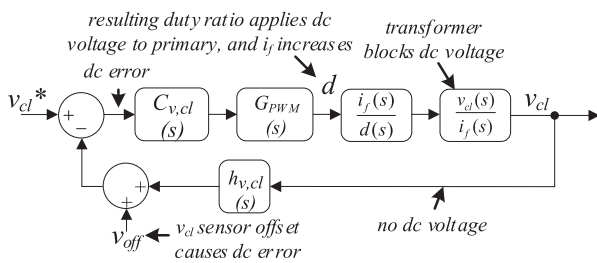


Fig. 5. Example of how cload sensor dc offset can cause dc current in the transformer.

The proposed control strategy in Fig. 4 solves this problem by adding a compensating dc voltage to the cload-bus voltage reference. This dc voltage reference is generated by the dc current control loop to ensure the dc current on the primary side of the transformer is within the reference i_f^* . To allow the design of these control loops, the small signal model of the VSC is split in two parts, the output current (before the transformer) as a function of the duty ratio, and the cload-bus voltage as a function of the converter output current (after the transformer). Both models are further developed in Section IV.

Considering that the dc output current control loop is designed to controlling the primary side dc current, it needs high dc gain to achieve low steady state error, but should have high attenuation at line frequency and its harmonics to avoid injecting harmonic content in the cload-bus voltage reference. The dc output current control loop includes the $C_{v,cl}$ controller, which

should be designed for high gain at line frequency to create the load voltages with low harmonic content. Therefore, the dc-current control loop naturally includes a source of high gain at line frequency. Therefore, proper design of $C_{i,f}$ and $h_{i,f}$ should have high attenuation at line frequency to compensate the gain from $C_{v,cl}$. This allows the product of $C_{i,f}$ and $h_{i,f}$ to be considered negligible when analyzing the load-bus voltage control loop in Fig. 4, as previously considered.

C. Control of Total DC-Bus Voltage

The rms amplitude of the load voltage v_{rms}^* is set by the total dc-bus voltage control loop, formed by controller C_{dc} , sensor h_{dc} , model $V_{\text{dc}}/V_{\text{cl}}(s)$, and the load-bus voltage control loop. A decrease in the load voltage increases the voltage drop in the series APF, which also increases the absorbed active power. An increase in the load voltage has the opposite effect, decreasing the absorbed active power. By changing the active power flow into the converter, the charge rate of the dc bus is controlled.

The three load-bus voltage controllers receive sinusoidal voltage references with the same amplitude, v_{rms}^* . The four-wire split-capacitor inverter can generate each phase voltage independently, allowing the controllers to balance the phase voltages to the same reference, with the required power transfer across phases occurring through the dc-bus capacitor.

If the source voltages are unbalanced, and since the load-bus voltage is balanced due to action of the load-bus controllers, each phase of the series APF can be either absorbing or providing active power. Equating the active power absorbed by the series APF, p_{APF} , considering steady-state operation with sinusoidal load and source voltages results in the following:

$$p_{\text{APF}} = \sum_{n=A,B,C} V_{\text{APF},n} \cdot I_{S,n} \cdot DF_n \quad (2)$$

where $V_{\text{APF},n}$ is the rms value of the voltage injected by the series APF, $I_{S,n}$ is the rms value of the source current, and DF_n is the displacement power factor of the load connected to each phase. Index $n = A, B, C$ denotes the phases in the system.

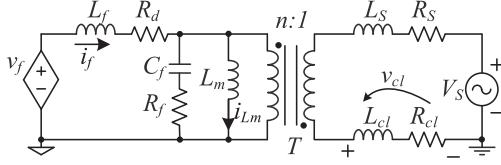


Fig. 6. Equivalent model representation of the series APF and power line considered to obtain small signal models of the load-bus voltage and primary side dc current.

For balanced phase voltages and loads, the voltage drop in each phase of the series APF is given by

$$V_{APF} = \frac{P_{APF}}{3 \cdot I_S \cdot PF}. \quad (3)$$

In steady-state, since the dc-bus voltage is constant, no active power flows into the dc-bus capacitor, all the active power absorbed by the series APF is therefore caused by its losses. This implies that a high-efficiency series APF must be used with this control technique to achieve acceptable load bus voltage amplitude. Furthermore, light load and poor load power factor increase the voltage drop. More details about this technique are given in [4] and [17].

The dc-bus total voltage C_{dc} should also be designed with high attenuation at line frequency to not affect the sinusoidal shape of the load-bus voltage reference. Therefore, the bandwidth of the total dc-bus controller is typically designed to be one decade below the line frequency.

D. Unbalance Control of DC-Bus Voltage

If the dc-bus capacitors were ideal, the dc-bus voltage unbalance would be zero, if the dc term of the neutral current of the inverter is zero. This could be achieved by setting the dc output current reference, i_f^* , to zero. In practice, the dc-bus capacitors have different leakage currents, and a small dc-current is still required in the neutral conductor. Therefore, i_f^* is set by the dc-bus voltage unbalance controller C_{dif} , to control the dc output current to achieve $V_{dif} = V_{dif}^* = 0$.

The dc-bus voltage unbalance control loop is also designed with high attenuation at line frequency to not affect the sinusoidal shape of the load-bus voltage reference.

IV. MODELS FOR CONTROLLER DESIGN

To design the controllers in the proposed strategy, small signal models are necessary to relate the output current of the converter with the duty cycle, and the load-bus voltage with the output current of the converter. The equivalent circuit used for modeling the converter is shown on Fig. 6. The transformer magnetizing inductance and an equivalent series resistance of the primary are considered in the model.

For the small signal analysis, the first step is to calculate the average value of the converter output voltage $v_f(t)$ before the LC filter, at the switching frequency $1/T_s$, which is

$$\langle v_f(t) \rangle = \frac{1}{T_s} \int_0^{d(t)T_s} \frac{v_{dc}(\tau)}{2} d\tau + \frac{1}{T_s} \int_{d(t)T_s}^{T_s} \frac{-v_{dc}(\tau)}{2} d\tau. \quad (4)$$

The small signal analysis is applied to (4) by substituting $v_{dc}(t) = V_{dc} + \hat{v}_{dc}(t)$, $d(t) = D + \hat{d}(t)$, and $\langle v_f(t) \rangle = V_F + \langle \hat{v}_f(t) \rangle$, with the hat symbol denoting the small signal variation, and capital letters the dc term. Second order terms and the variation of the dc-bus voltage are considered negligible, resulting in the small signal converter output voltage, which is given by

$$\langle \hat{v}_f(t) \rangle = V_{dc} \hat{d}(t). \quad (5)$$

The voltage source is considered a constant value at the switching frequency such that its small signal approximation is $\langle \hat{v}_s(t) \rangle = 0$.

The small signal model relating the converter output current and the duty cycle is found by substituting the small signal approximation of the VSC output voltage and the source voltage in the equivalent circuit in Fig. 6. R_d is the equivalent resistance of the filter inductor and transformer primary winding. L_m is the magnetizing inductance of the transformer. The load, at fundamental frequency, is represented by L_{cl} and R_{cl} . Using circuit analysis and applying the Laplace transform results in

$$\frac{\hat{i}_f(s)}{\hat{d}(s)} = \frac{V_{dc}}{R_d + sL_f + \left(R_f + \frac{1}{sC_f} \right) // sL_m // (R_{eq} + sL_{eq})} \quad (6)$$

where $R_{eq} = R_{cl} + R_s$ is the total resistance in the secondary side and $L_{eq} = L_{cl} + L_s$ is the total inductance. Symbol $//$ represents the parallel equivalent of two impedances. The transformer is considered to have 1:1 turns ratio, and the reflected impedance should be used when the turns ratio are different.

The small signal model of the load-bus voltage as a function of the output current is found by considering that the converter output current is a controlled current source modeled by (6). By applying this small signal approximation, and using circuit analysis and the Laplace transform, the model is found as follows:

$$\frac{\hat{v}_{cl}(s)}{\hat{i}_f(s)} = \left(\left(R_f + \frac{1}{sC_f} \right) // sL_m // (R_{eq} + sL_{eq}) \right) \times \frac{R_{cl} + sL_{cl}}{R_{eq} + sL_{eq}} \quad (7)$$

V. DESIGN OF SERIES APF CONTROL LOOPS

The proposed control strategy for the series APF is verified in a 3 kVA prototype. The parameters of the prototype and the connected load are given in Table I. The load-bus voltage controller is implemented using analog circuits and the remaining controllers are implemented digitally. The transformer leakage inductance L_{lk} is also used for filtering the VSC output voltage, and is directly added to the filter inductance L_f , as the filtering capacitors C_f are placed in the secondary of the transformer. Placing the filtering capacitors in the primary side changes the output filter topology to “LCL,” and the model presented in this paper should not be used if that is the case. The digital controllers were designed in the “s” domain and discretized, as they have low bandwidth when compared to the sampling frequency. The open loop transfer function for designing the load-bus voltage

TABLE I
EXPERIMENTAL PARAMETERS. TRANSFORMER VALUES ARE PRIMARY
SIDE REFERRED

Symbol	Quantity	Value
S_L	Three-Phase load Apparent Power	3 kVA
$V_{cl,nom}$	load-bus Nominal Voltage	220 Vrms
V_{dc}	Total dc-bus Voltage	400 V
ω	Angular Frequency	$2\pi 60$ rad
L_f	AC Side Inductors	550 μ H
R_{d,L_f}	L_f Series Resistance	0.1 Ω
C_f	AC Side Capacitors	10 μ F
L_{lk}	Transformer leakage inductance	330 μ H
$R_{d,T}$	Transformer Series Resistance	0.6 Ω
L_m	Transformer Magnetizing Inductance	0.2 H
n	Transformer turn ratio	$1/\sqrt{3}$
$C_{O,1}, C_{O,2}$	dc-bus Capacitors	3 mF
$\bar{Z}_S$	Source Impedance	$0.160 + j0.377 \Omega$
$\bar{Z}_{cl}$	Equivalent load Impedance	$66.13 + j20.8 \Omega$
S_R	Resistive load Power	40% S_L
S_{RL}	Resistive-inductive load Power	35% S_L
S_{CFR}	3 ϕ Capacitive Filter Rectifier Power	25% S_L
f_s	Switching Frequency	20 kHz

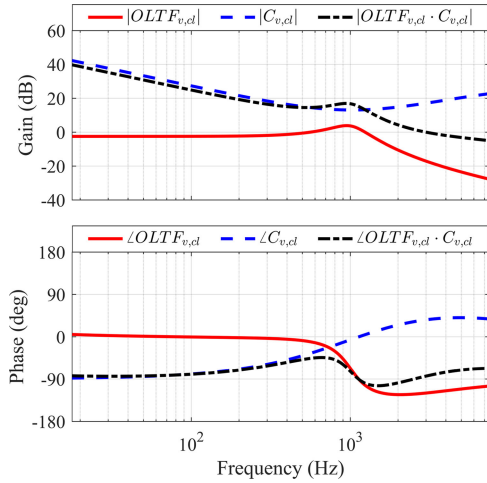


Fig. 7. Bode plots of the load-bus control loop.

controller is

$$OLTF_{v,cl} = G_{PWM} \frac{\hat{i}_f}{\hat{d}} \left(\frac{\hat{v}_{cl}}{\hat{i}_f} h_{v,cl} + C_{i,f} h_{i,f} \right). \quad (8)$$

It is assumed that $C_{i,f} h_{i,f} \approx 0$. The chosen controller is a proportional-integral-derivative (PID) controller, with an additional filtering pole, which ensures a crossover frequency of 3 kHz with phase margin of 96°. Fig. 7 presents bode plots of $OLTF_{v,cl}$, $C_{v,cl}$, and the compensated loop transfer function $OLTF_{v,cl} \cdot C_{v,cl}$.

For the dc current controller the open loop transfer function is

$$OLTF_{i,f} = \frac{C_{v,cl} G_{PWM} \frac{\hat{i}_f}{\hat{d}}}{1 + C_{v,cl} G_{PWM} \frac{\hat{i}_f}{\hat{d}} h_{v,cl}} h_{i,f}. \quad (9)$$

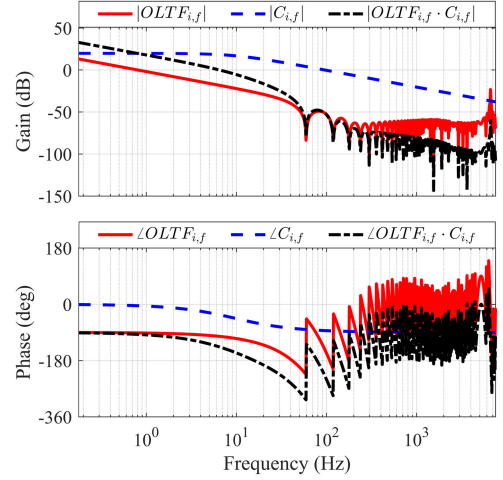


Fig. 8. Bode plots of the dc current control loop.

Since the feedback of the current loop is at branch i_f , $v_{cl}(s)/i_f(s)$ appears in the denominator of $OLTF_{i,f}$ but not the numerator. Model $v_{cl}(s)/i_f(s)$ has a zero at the origin of the s plane, which cancels the integrator from $C_{v,cl}$ in the denominator. Since term $C_{v,cl}$ also appears in the numerator of $OLTF_{i,f}$, $OLTF_{i,f}$ already has an integrator, and the controller designed for the dc current loop has only a proportional term with an additional filtering. The controller is designed with 6.4 Hz crossover frequency and phase margin of 44°. The bode plots of $OLTF_{i,f}$, $C_{i,f}$, and $OLTF_{i,f} \cdot C_{i,f}$ are shown in Fig. 8. Furthermore, to not affect the load-bus voltage reference at line frequency, a moving average filter is applied to the current feedback, attenuating the measured current at line frequency and its harmonics.

The dc-bus voltage control uses the strategy presented in [17] and the small signal for $\hat{v}_{dc}/\hat{v}_{cl}$ is

$$\frac{\hat{v}_{dc}}{\hat{v}_{cl}} = \frac{-3R_{cl}V_S}{sC_oV_{dc}}. \quad (10)$$

The open loop transfer function $OLTF_{v_{dc}}$ of the dc bus is shown in (11). The load-bus voltage control loop is simplified into the gain $1/h_{v,cl}$, as it has high bandwidth when compared to the dc-bus voltage control loop. The controller designed for dc-bus voltage control has proportional-integral action with an additional filtering pole, that results in a 6.6 Hz crossover frequency with phase margin of 82°. The bode plots of $OLTF_{v_{dc}}$, C_{dc} , and $OLTF_{v_{dc}} \cdot C_{dc}$ are shown in Fig. 9 [the 180° phase shift caused by the signal in (10) is not shown]. Notice that the model in (10) has an integrator since no loss in the dc bus was modeled, and in practice an integrator is necessary to achieve zero steady-state error

$$OLTF_{v_{dc}} = \frac{1}{h_{v,cl}} \frac{\hat{v}_{dc}}{\hat{v}_{cl}} h_{dc}. \quad (11)$$

The model for the voltage unbalance as a function of the dc current was presented in [3] and is

$$\frac{\hat{v}_{dif}}{\hat{i}_f} = \frac{3}{2sC_o}. \quad (12)$$

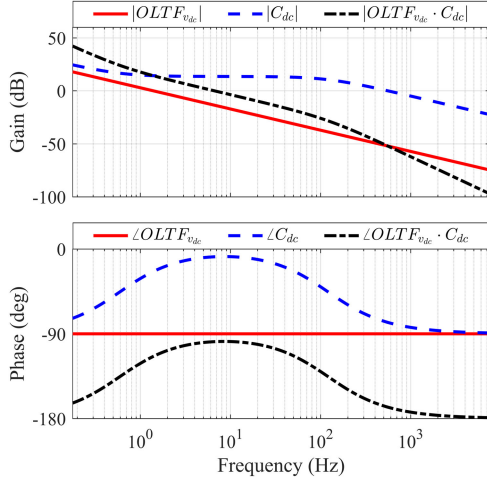


Fig. 9. Bode plots of the dc-bus voltage control loop.

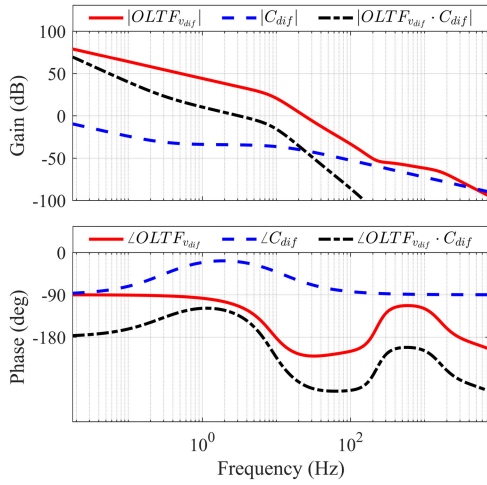


Fig. 10. Bode plots of the dc-bus unbalance voltage control loop.

Since the dc current control loop has bandwidth of 6.4 Hz, it cannot be approximated as $1/h_{i,f}$, and the dc-bus voltage unbalance open loop is

$$OLTF_{v_{dif}} = \frac{\hat{v}_{dif}}{\hat{i}_f} h_{dif} \frac{A}{1 + A h_{i,f}} \quad (13)$$

where

$$A = C_{i,f} \frac{C_{v,cl} G_{PWM} \frac{\hat{i}_f}{d}}{1 + C_{v,cl} G_{PWM} \frac{\hat{i}_f}{d} h_{v,cl}}. \quad (14)$$

A proportional-integral controller with additional filtering pole was designed for a 3.1 Hz crossover frequency with a phase margin of 46° . The bode plots of $OLTF_{v_{dif}}$, C_{dif} , and $OLTF_{v_{dif}} \cdot C_{dif}$ are shown in Fig. 10. The integral action in C_{dif} is required to achieve zero steady-state error, as the integrator in (12) is again caused by the model by not considering losses in the dc bus.

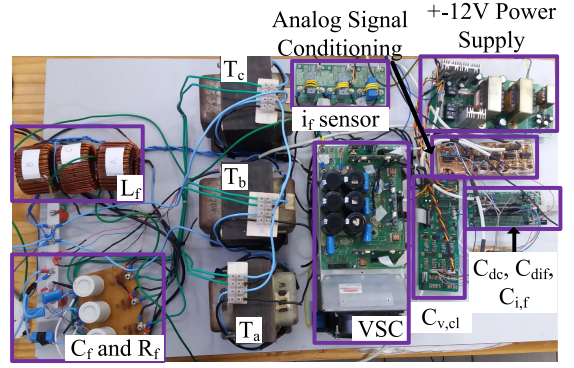


Fig. 11. Series APF, 3 kVA prototype.

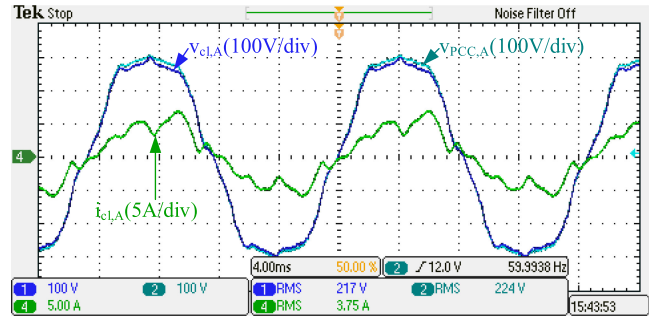


Fig. 12. Experimental waveforms without the VSC.

TABLE II
EXPERIMENTAL CLOAD-BUS AND PCC-BUS RMS VOLTAGES WITH THE COUPLING TRANSFORMERS PRIMARY SIDE SHORT CIRCUITED

Phase	PCC-bus (Vrms)	load-bus (Vrms)	Drop (%)
A	225.8	219.8	2.68
B	226.4	220.3	2.66
C	236.4	226.38	4.28

VI. EXPERIMENTAL RESULTS

The control strategy was validated experimentally with the prototype shown in Fig. 11. The system is initially run without the series APF VSC, but with the injection transformer connected and its primary side short circuited. Experimental waveforms of phase A are shown in Fig. 12, where the measured THD of load current, cload voltage, and PCC voltage are 9.7%, 9.3%, and 26.5%, respectively. The objective of running the system with the injection transformer is to verify its series voltage drop, since the dc-bus control strategy will increase this voltage drop for compensating the losses in the series APF VSC. The rms values of the cload-bus and PCC-bus voltages are given in Table II, the voltage drop is $\approx 3\%$, and phase C presents deviation in its voltage amplitude.

The phase voltage waveforms of the system running in its nominal operation point are shown in Figs. 13 and 14, for the PCC-bus and cload-bus, respectively. Waveforms of the cload, PCC, and transformer injected voltage of phase A are shown in Fig. 15. The voltage injected by the series APF has significantly lower amplitude than the PCC-bus and cload-bus voltage. The

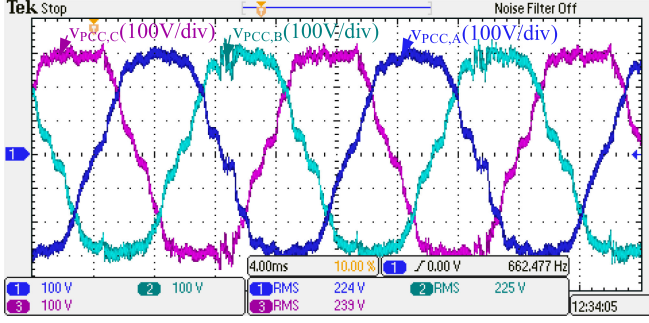


Fig. 13. Experimental PCC-bus voltage waveforms of the series APF.

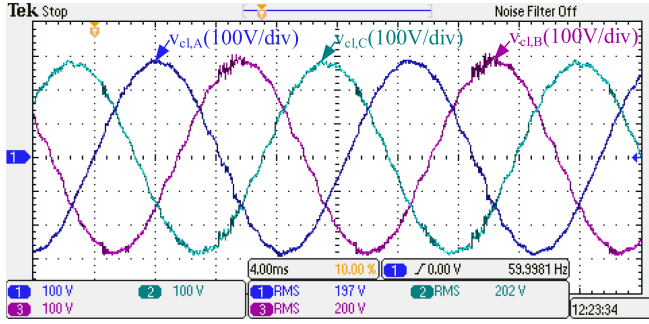


Fig. 14. Experimental load-bus voltage waveforms of the series APF.

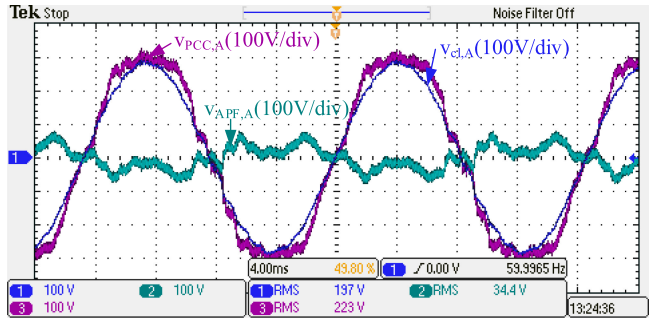


Fig. 15. Experimental waveforms of phase A load voltage, PCC voltage, and series APF injected voltage.

harmonic spectrum of the PCC-bus and load-bus voltages, of phase C, are shown in Fig. 16.

Experimental values of rms voltage and THD are given in Table III, for two dc-bus voltages, 200 V and 400 V. In nominal operation the load-bus voltage THD is significantly improved, from an average of 9.9% to 2.5%. When operating with nominal dc-bus voltage there is significant voltage drop of $\approx 13\%$. Since the displacement factor of the load is not particularly low, and the load current is at its maximum value, (3) indicates this excessive drop caused by losses in the series APF VSC. However, since in this application the series APF needs to inject voltages with only a percentage of the fundamental (harmonic amplitude), it is possible to decrease the dc-bus voltage to improve system efficiency. A reduction in the dc-bus voltage to 200 V decreases the voltage drop to $\approx 6\%$. A VSC with lower voltage switches could be used to further improve efficiency,

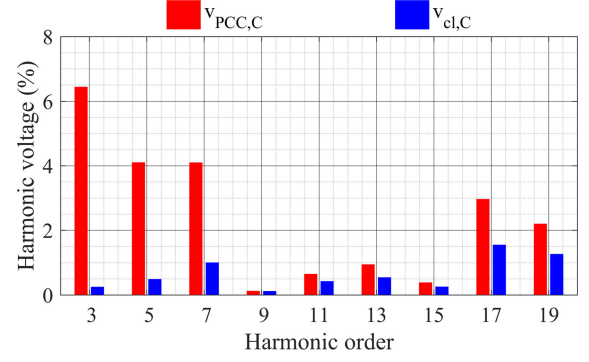


Fig. 16. Experimental harmonic spectrum of phase C voltages as percentage of fundamental.

TABLE III
EXPERIMENTAL LOAD-BUS AND PCC-BUS RMS VOLTAGES WITH THE COUPLING TRANSFORMERS PRIMARY SIDE SHORT CIRCUITED

Measurement	Location	v_{dc}^*	Phase A	Phase B	Phase C
THD (%)	PCC-bus	400V	9.5	9.7	10.5
		200V	9.2	9.2	10.5
	load-bus	400V	2.3	2.6	2.7
		200V	3.0	3.2	3.3
	PCC-bus	400V	227.1	226.7	237.0
		200V	225.8	225.3	235.4
RMS value (V)	load-bus	400V	201.0	199.1	200.4
		200V	215.3	213.1	214.6

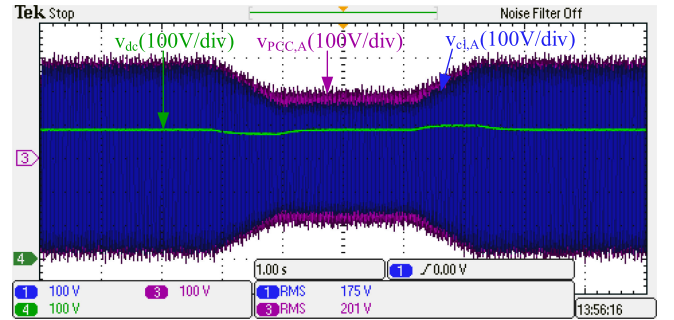


Fig. 17. Experimental waveform of the dc-bus voltage during PCC-bus rms voltage variation.

or alternatively, a different transformer turns ratio can be used to decrease the VSC current while keeping the 400 V dc-bus voltage. Both of these changes come at the cost of decreasing the maximum amplitude of voltage sags and swells that can be compensated, which is related to the maximum voltage injected by the split capacitor series APF, and can be given by

$$V_{APF,max} = \frac{V_{dc}}{2n}. \quad (15)$$

A. Control of DC-Bus Voltage and DC Output Current

A variation in the source voltage is used for validating the total dc-bus voltage control, with experimental waveforms shown in Fig. 17. The source voltage rms value is varied by ± 80 V in a linear ramp with two seconds duration. The negative variation

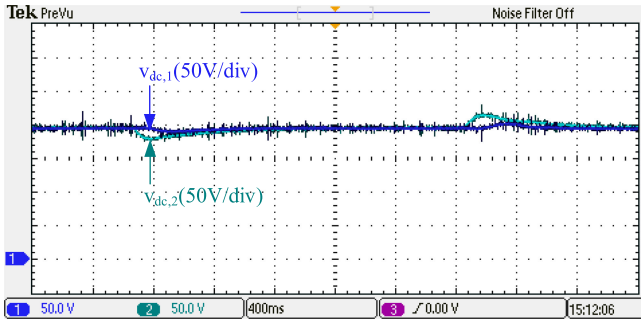


Fig. 18. Experimental waveforms of the $V_{dc,1}$ and $V_{dc,2}$ after 167 W load connected/disconnected in parallel to the $C_{o,2}$ capacitor.

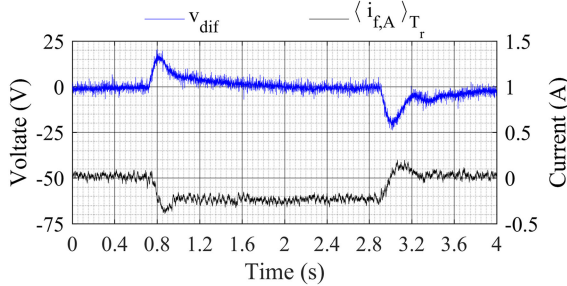


Fig. 19. Experimental waveforms of V_{DIF} and $\langle i_{F,A} \rangle_{T_r}$ after 167 W load connected/disconnected in parallel to the $C_{o,2}$ capacitor.

in source voltage results in a dc-bus voltage drop of 13.5 V, while the positive variation results in a dc-bus voltage increase of 13.8 V.

The dc-bus unbalance control was validated by connecting and removing a 167 W load in parallel to the $C_{o,2}$ dc-bus capacitor, causing a variation in V_{dif} of 16 V and -19 V, respectively. The experimental voltage waveforms of the dc-bus capacitors are shown in Fig. 18. The result is satisfactory, with the voltage unbalance being corrected for both positive and negative load steps.

To correct the dc-bus unbalance, the controller needs to impose a dc current in the primary side of the transformer, which has low amplitude compared to the fundamental component of the primary current, and cannot be visualized in the captured waveforms. Therefore, the primary side current data points, from phase A, were imported into a data processing software, and a moving average filter, with window size equal to the line period, was used to compute the dc current. That is, $\langle i_F \rangle_{T_r}$ is computed.

The primary side dc current and the dc-bus differential voltage, from the same experiment shown in Fig. 18, are shown in Fig. 19. Without the unbalanced load in the dc bus, the primary side current is close to zero, and after the unbalanced load is connected, the dc current increases to 240 mA. Therefore, the control strategy achieves the objective of controlling the dc-bus unbalance and keeps the dc current in the injection transformer controlled and close to zero.

VII. CONCLUSION

This paper presented a complete control strategy for a 3P4W series APF, which uses injection transformers to improve the

PCC-bus voltage in a secondary cload-bus. This control strategy uses cload-bus voltage feedback that provides increased harmonic elimination with simpler control as it can compensate the voltage drops in the injection transformer. A new strategy for controlling the dc output current of the converter, to avoid transformer saturation, was developed, and is also used for controlling the dc-bus capacitor voltage unbalance. Small signal models required for designing the proposed dc output current controller were also presented. The dc current control strategy can also be applied to other converters, including DVR and UPQC, when the series connected inverter uses load-bus voltage feedback.

The experimental results showed the viability of the control strategy. The connection of an unbalanced load in the dc bus does not cause steady state unbalance in its voltage, or transformer saturation. Operation without the dc-bus voltage unbalance controller and the primary side dc current controller was not possible, as the voltage from one of the dc-bus capacitors drops to zero, showing that the complete control strategy presented in this paper is necessary and an important contribution, if use of load-bus voltage feedback is desired.

The operation with lower dc-bus voltage shows that the voltage drop in the series APF, necessary for compensating its losses in the proposed control strategy, can be small enough to achieve satisfactory load voltages, but is still a point that requires improvement as the phase of the voltage drop in the series APF is synchronized with the PCC-bus phase, resulting in a reactive voltage drop if the load displacement factor is not unity. Future work can verify the possibility of improving load-bus voltage amplitude by varying the series APF voltage drop phase angle.

ACKNOWLEDGMENT

The authors would like to thank FAPESC and CAPES for the financial support of this paper.

REFERENCES

- [1] P. Fang Zheng, "Application issues of active power filters," *IEEE Ind. Appl. Mag.*, vol. 4, no. 5, pp. 21–30, Sep./Oct. 1998.
- [2] A. M. Rauf and V. Khadkikar, "An enhanced voltage sag compensation scheme for dynamic voltage restorer," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2683–2692, May 2015.
- [3] R. J. Millnitz dos Santos, J. C. da Cunha, and M. Mezaroba, "A simplified control technique for a dual unified power quality conditioner," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5851–5860, Nov. 2014.
- [4] E. R. Ribeiro and I. Barbi, "Harmonic voltage reduction using a series active filter under different load conditions," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1394–1402, Sep. 2006.
- [5] J. G. Pinto, H. Carneiro, B. Exposto, C. Couto, and J. L. Afonso, "Transformerless series active power filter to compensate voltage disturbances," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, Aug. 2011, pp. 1–6.
- [6] G. A. de Almeida Carlos and C. B. Jacobina, "Series compensator based on cascaded transformers coupled with three-phase bridge converters," *IEEE Trans. Ind. Appl.*, vol. 53, no. 2, pp. 1271–1279, Mar. 2017.
- [7] Y. Chang, L. Jinjun, W. Xiaoyu, and W. Zhaoan, "A novel control of series active power filter without harmonics detection," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 1112–1115.
- [8] B. Wang and M. Illindala, "Operation and control of a dynamic voltage restorer using transformer coupled H-bridge converters," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1053–1061, Jul. 2006.

- [9] S. A. O. D. Silva, P. F. Donoso-Garcia, and P. C. Cortizo, "A three-phase series-parallel compensated line-interactive ups system with sinusoidal input current and sinusoidal output voltage," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf. 34th IAS Annu. Meeting*, vol. 2, 1999, pp. 826–832.
- [10] F. Mekri, M. Machmoum, N. Ait-Ahmed, and B. Mazari, "Saturation influence on the performances of series active power filter," in *Proc. 35th Annu. Conf. IEEE Ind. Electron.*, Nov. 2009, pp. 3258–3263.
- [11] J. Dias, M. Mezaroba, C. Rech, L. Michels, and T. D. Busarello, "Controle digital simplificado para um compensador unificado de qualidade de energia," *Eletrônica de Potência*, vol. 16, no. 3, pp. 212–221, 2011.
- [12] G. S. Fischer, A. Mengatto, and M. Mezaroba, "A control strategy for a series APF with load-bus side feedback that avoids transformer saturation," in *Proc. Brazilian Power Electron. Conf.*, Nov. 2017, pp. 1–6.
- [13] P. Mysiak, W. Sleszynski, and A. Cichowski, "Experimental test results of the 150kva 18-pulse diode rectifier with series active power filter," in *Proc. 10th Int. Conf. Compat., Power Electron. Power Eng.*, Jun. 2016, pp. 380–383.
- [14] J. Turunen, M. Salo, and H. Tuusa, "The influence of the dc-link voltage control on the current harmonic filtering of the series hybrid active power filters," in *Proc. 31st Annu. Conf. IEEE Ind. Electron. Soc., IECON*, 2005, pp. 1–6.
- [15] V. Khadkikar, "Enhancing electric power quality using UPQC: A comprehensive overview," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2284–2297, May 2012.
- [16] M. Aredes and E. H. Watanabe, "New control algorithms for series and shunt three-phase four-wire active power filters," *IEEE Trans. Power Del.*, vol. 10, no. 3, pp. 1649–1656, Jul. 1995.
- [17] G. S. Fischer, A. Mengatto, and M. Mezaroba, "A small signal model for controlling the dc bus voltage of a series active power filter," in *Proc. IEEE 8th Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2017.
- [18] F. Turnbull, "Inverter with electronically controlled neutral terminal," U.S. Patent 3 775 663, Nov. 27, 1973.



Guilherme da Silva Fischer received the B.S. and M.Eng. degrees in electrical engineering from Santa Catarina State University, Florianópolis, Brazil, in 2016 and 2018, respectively.

He is currently with WEG Automation in research and development of low voltage inverters for electric motors. His research interest includes control and modulation techniques for power converters.



energy efficiency.

Alisson Mengatto was born in Videira, Brazil, in 1993. He received the B.S. degree in electrical engineering from Santa Catarina State University, Florianópolis, Brazil, in 2016, where he is currently working toward the M.S. degree.

From 2013 to 2018, he was a Research Assistant with the Electrical Energy Processing Group. He is currently with Itaipu Binacional hydroelectric as a power plant and substation operator. His research interests include power electronics for renewable energy sources and electric vehicles, power quality, and



Luis Gustavo Kremer received the B.S. degree in electrical engineering from Santa Catarina State University, Florianópolis, Brazil, in 2018.

In 2012, he joined the Electrical Energy Processing Group from Santa Catarina State University, where he worked with power electronics for photovoltaic applications as an undergraduate researcher. He was also recipient of a scholarship to study for a year at the University of Southern California in 2014 and joined a power electronics research group with the Illinois Institute of Technology in 2015.



Marcello Mezaroba (M'08) was born in Videira, Brazil, in 1972. He received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1996, 1998, and 2001, respectively.

Since 2002, he has been with Santa Catarina State University, Joinville, Brazil, where he is currently an Associate Professor. In 2004 was a Co-Founder of the SUPPLIER company, Joinville, Brazil, where he is currently the Technical Director. He is a member of the Brazilian Power Electronics Society (SO-

BRAEP). He has extensive experience in the coordination and execution of research and development projects and he was responsible for the design and execution of several industrial technological products placed in the national market. He was the Coordinator of the Graduate Program in electrical engineering with UDESC and participated in the Research and Graduate Committees. He was elected for the deliberative council of the SOBRAEP in 2013 and 2015, respectively, and in 2017, he was elected as Vice-President. Since 2018, he has been the Editor-in-Chief for the *Brazilian Power Electronics Journal*. His research interests include soft-switching commutation, power conditioning, renewable-energy sources, ac and dc power sources, and power processing and control in microgrids.