

Module Integrated Buck Inverter: Analysis and Design

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Abstract—This paper proposes a new grid current controller for a photovoltaic (PV) module integrated buck inverter using a single pulsewidth modulation switch and an unfolding H-bridge, which significantly reduces switching losses. To achieve this, an internal grid current loop with active damping is presented with an *LCL* filter to connect it to the utility grid. The problem of the filter natural resonance is solved by means of a virtual impedance (active damping), demanding no additional sensor. Experimental results obtained from a 200-W prototype achieved a European efficiency of 96.27% with a current total harmonic distortion of 3.7%.

Index Terms—Active damping, *LCL*-filter, module integrated converters (MIC), unfolding, virtual impedance.

I. INTRODUCTION

ADVANCES in photovoltaic (PV) technologies and decreasing PV module prices have been contributing to the considerable increase in PV solar energy market investments. In addition, due to the new regulatory standards, residential low power single-phase plants are proliferating in many countries and have been proving to be a market opportunity for small power string-inverters and module integrated converters (MIC) technology advances. In residential and commercial buildings such as houses, data centers, and small businesses and bank offices, there are large number of loads, most of which comprises electronic light bulb devices, data storage computers, and other low power electronic equipment. To supply such load profile, PV installations features such as redundancy, modularity, and scalability are important characteristics, which are quite suitable for photovoltaic ac modules (MIC) [1], [2].

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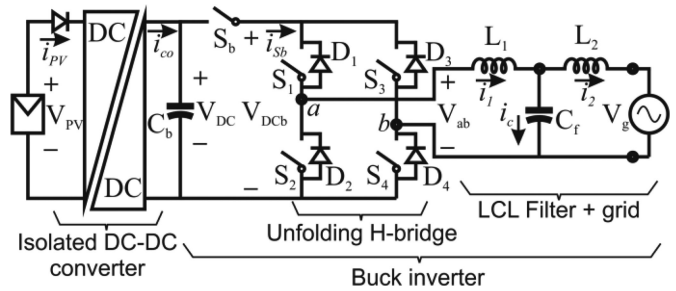


Fig. 1. Diagram of the proposed MIC topology.

Grid-tied MIC topologies have been presented in the literature in three distinct categories [1], [3]–[10]: first, MIC with dc bus [1], [3]–[5], second, MIC with pseudo dc bus [6]–[8], or third, MIC without dc bus [2], [9], [10]. All of them have many advantages when compared to other grid-tied PV inverters. They provide partial shadow and mismatching problem immunity, as well as galvanic isolation by means of high-frequency transformers. Moreover, MIC without dc bus requires a more complex design. It avoids the use of bulky dc capacitors at the price of using an ac–ac stage with many switching devices [8]. On the other hand, MIC with dc bus presents the simplest power stage among MIC topologies [2]. In addition, the dc-bus capacitor provides power decoupling for the inherent pulsating single-phase power, which further simplifies the system control design. Nevertheless, it suffers from high switching losses. In spite of reducing switching losses by employing a low frequency unfolding H-bridge, the MIC with pseudo dc bus yields an oversized transformer designed for the low frequency current component at the double grid frequency that flows through it.

Aiming to associate the design and control simplicity of the MIC with dc bus and low switching losses of the MIC with pseudo dc bus, a different topology was proposed by Pacheco Meurer *et al.* [11]. The proposed dc–ac stage was modified in such a way that it incorporated a buck converter with a merged unfolding H-bridge. A high order *LCL* filter is adopted to improve the grid filter attenuation (see Fig. 1). The buck switch is modulated by the high-frequency pulsewidth modulation (PWM) and the H-bridge switches operate at line frequency, reducing the overall inverter losses. Furthermore, in the proposed topology, the buck diode is suppressed and the free-wheeling stage is performed by the diodes of the H-bridge switches.

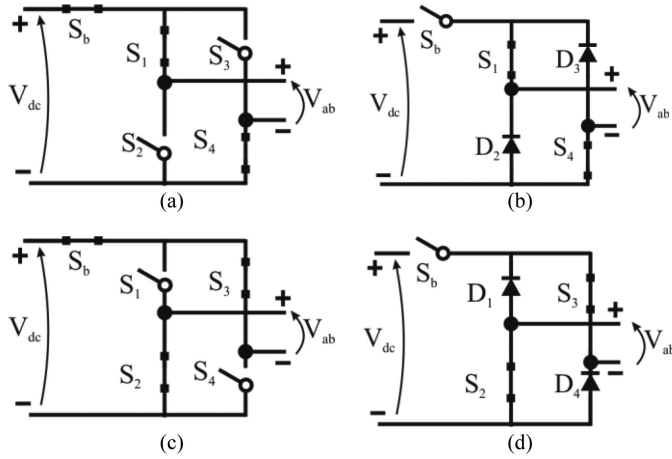


Fig. 2. Diagram for the states of operation for the buck inverter. (a) State 1 (power transfer in grid positive half-cycle). (b) State 2 (zero). (c) State 3 (power transfer in grid negative half-cycle). (d) State 4 (zero).

Among many approaches to provide *LCL* resonance damping discussed in the literature [12], [13], this paper presents an active damping technique with grid-current feedback similar to that proposed in [17], however, with improvement in the damping loop admittance, providing additional filtering capability to high-frequency measurement noise with the inclusion of an additional pole.

Despite proposing a two-stage microinverter topology (see Fig. 1), this paper focuses on only analyzing the dc–ac stage, in which the main objective is to present its modulation and control system structure and design. Notably, the proposed control system can be used in standard PWM H-bridge or multilevel inverters, requiring the use of the adequate modulation.

In this manner, this paper is organized as follows. Buck inverter operation and modulation is discussed in Section II. Section III provides a detailed modeling of the buck inverter, taking into account the *LCL* filter without damping and with active damping using the grid-current feedback. A detailed design of the controllers is presented in Section IV. Finally, Section V gives an experimental prototype of 200 W that was developed to obtain results to compare with the standard IEEE 1549, which specifies limits on the harmonic current injection to the utility grid.

II. OPERATION OF THE BUCK INVERTER

The buck inverter (see Fig. 1) consists of five active switches and a third order *LCL* filter (L_1 , L_2 , and C_f). The active switch S_b operates at a high frequency (PWM) and the other four H-bridge switches (S_1 through S_4) operate at line frequency. The five switches are activated in such a way that the buck converter operates in four possible switching states (see Fig. 2 and Table I). Table I gives that voltage V_{ab} assumes three distinct values: $+V_{DC}$, $-V_{DC}$, and zero (0). The zero value can be obtained with states 2 and 4. In these states, the buck freewheeling stage is accomplished by the antiparallel diodes (D_2 – D_3) and (D_1 – D_4), respectively. The other states transfer power from the PV to the

TABLE I
SWITCHING STAGE FOR BUCK INVERTER

State	Switching stage					V_{ab}
	S_b	S_1/D_1	S_2/D_2	S_3/D_3	S_4/D_4	
1	1	1	0	0	1	$+V_{DC}$
2	0	1	1 ^(*)	1 ^(*)	1	0
3	1	0	1	1	0	$-V_{DC}$
4	0	1 ^(*)	1	1	1 ^(*)	0

* antiparallel diode forward bias (conducting stage).

utility grid. States 1 and 2 take place during the positive grid voltage semicycle. States 3 and 4 occur during the negative grid voltage semicycle.

A. Modulation Function of the Buck Inverter

The buck inverter topology was developed to reduce switching losses of the high switching frequency inverter of the MIC. It is based on a well-known approach to reduce standard single and three-phase inverter switching losses that use discontinuous pulsewidth modulation (DPWM) [14]. In such a technique, the modulating signal is clamped to the dc-bus voltage for one half of the period and there are no switching instances during this time interval [see Fig. 3(a)]. The modulating signal for inverter leg “a” is clamped to the negative dc bus for the entire negative output voltage semicycle. On the other hand, the modulation signal for inverter leg “a” is clamped to the negative rail during the positive output voltage semicycle. Voltage V_a is switched between the positive dc-bus voltage and zero only during the positive output voltage semicycle, and voltage V_b is switched between the positive dc-bus voltage and zero only during the negative output voltage semicycle. Thus, only one phase leg switches at any instant, resulting in a 50% reduction in switching loss [15].

Another approach for modulating the signal is shown in Fig. 3(b), which is an advanced discontinuous pulsewidth modulation (ADPWM) that provides the same voltage modulation for V_a and V_b . The difference of these modulating signals is that both leg “a” and leg “b” are clamped to the positive dc bus for the positive and negative semicycle, respectively.

In order to achieve the benefits of both modulations avoiding any switching instant for the H-bridge switches, the modulating signals of the DPWM and ADPWM have been combined in order that the clamped intervals are gathered to form the H-bridge modulation. The switching interval of the DPWM and ADPWM modulating signals are gathered to form the buck switch modulation [see Fig. 3(c)].

For a standard three level PWM and the H-bridge PWM inverter, all four switches operate at PWM frequency. The PWM signal for each H-bridge leg is obtained by comparing one modulator (1) with a triangular carrier signal. For the buck inverter, the H-bridge leg modulating signals are always at $+1$ or -1 , ensuring no switching instant. To perform sinusoidal PWM, one additional switch and modulating signal is required. This signal is obtained combining the half cycles [see Fig. 3(c)].

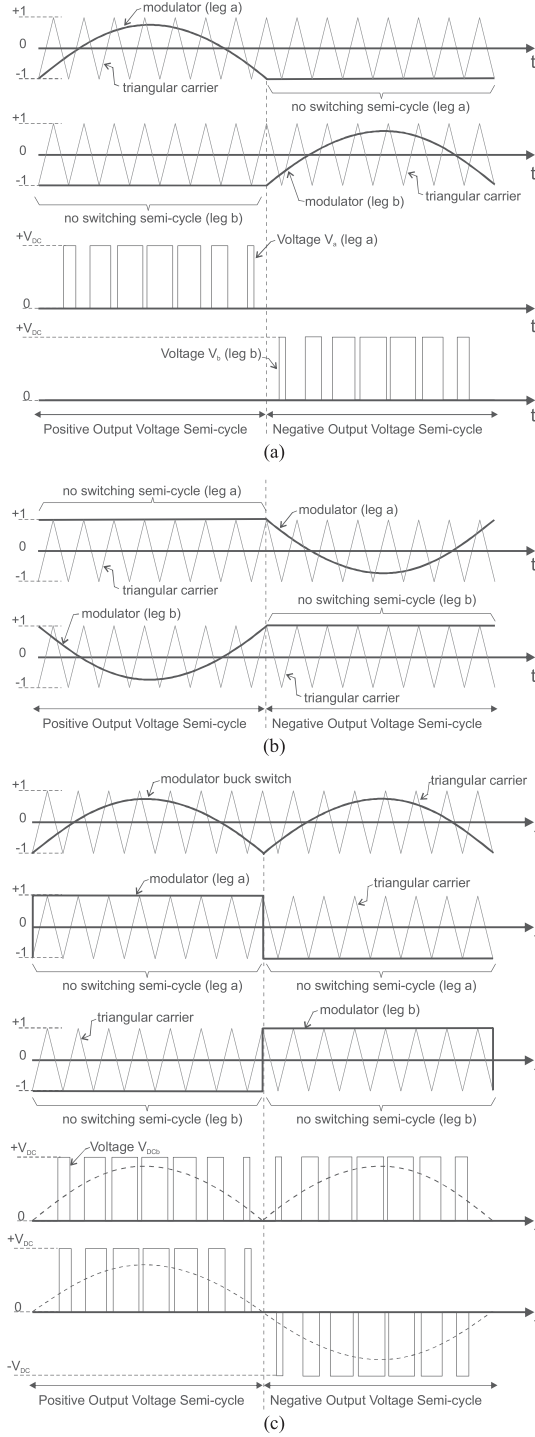


Fig. 3. Modulation strategy. (a) DPWM modulating signals. (b) ADPWM modulating signals. (c) Buck inverter modulating signals.

Equation (1) is a sinusoidal modulating signal (u), commonly used for PWM inverters and used to obtain the modulating signals for the buck inverter. Equation (2) presents the modulating signal for the PWM switch (S_b), meanwhile (3) and (4) present the modulating functions (u_2) and (u_3) associated with leg a and b , respectively, as follows:

$$u = M \sin(\omega t) \quad (1)$$

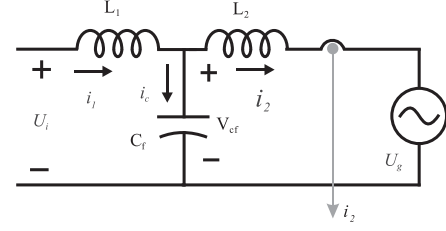


Fig. 4. Inner current loop modeling circuit.

$$u_1 = |u| = \begin{cases} M \sin(\omega t), & 0 < \omega \leq \pi \\ -M \sin(\omega t), & \pi < \omega < 2\pi \end{cases} \quad (2)$$

$$u_2 = \begin{cases} +1, & 0 < \omega \leq \pi \\ -1, & \pi < \omega < 2\pi \end{cases} \quad (3)$$

$$u_3 = \begin{cases} -1, & 0 < \omega \leq \pi \\ +1, & \pi < \omega < 2\pi. \end{cases} \quad (4)$$

III. BUCK INVERTER MODELING

In this section, a linear time-invariant small-signal state-space model for the buck inverter is presented.

The proposed buck inverter utilizes a multiloop control method. It comprises an outer voltage loop control and two inner current loops. The grid inductor inner current loop is responsible to ensure stability over a wide range of operations, providing fast dynamic responses, which requires wide bandwidth in order to compensate for grid voltage harmonics. The other inner current loop is dedicated to the virtual impedance implementation.

To model the grid inductor inner current loop of buck inverter, the power circuit to be modeled is shown in Fig. 4. It comprises the LCL components and two voltage sources, one of them representing the PWM voltage U_i and the other the grid voltage U_g . In addition, the grid current i_2 that is the output variable is also identified. Equations (5)–(7) present the dynamics of the inverter considering the average model as

$$\frac{L_1 di_1(t)}{dt} = U_i(t) - v_{Cf}(t) \quad (5)$$

$$\frac{C_f dv_{Cf}(t)}{dt} = i_1(t) - i_2(t) \quad (6)$$

$$\frac{L_2 di_2(t)}{dt} = v_{Cf}(t) - U_g(t) \quad (7)$$

$$U_i = dV_{in}. \quad (8)$$

A. Undamped Grid Inductor Inner Current Loop Model

The grid inductor inner current plant is modeled according to the space-state equation (9), where the terms $[i_1, V_{cf}, i_2]^T$ are the states of the plant (x), (u) represents the inputs of the system (U_i and U_g), and (y) is the output of interest i_2

$$\begin{aligned} \dot{x} &= \mathbf{A}x + \mathbf{B}u \\ y &= \mathbf{C}x + \mathbf{E}u. \end{aligned} \quad (9)$$

The system matrices are presented in the following:

$$\mathbf{A} = \begin{bmatrix} 0 & -1/L_1 & 0 \\ 1/C_f & 0 & -1/C_f \\ 0 & 1/L_2 & 0 \end{bmatrix} \quad (10)$$

$$\mathbf{B} = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & \frac{-1}{L_2} \end{bmatrix}, \mathbf{C} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}, \mathbf{E} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}.$$

The transfer function for the grid current (i_2) by the input modulating signal (U_i) is given by (11). We can observe by its denominator that there is no damping coefficient in the characteristic equation (11). Thus, it presents an infinite gain at the resonance frequency, which may cause instability problems

$$G_p(s) = \frac{i_2(s)}{U_i(s)} = \frac{1}{s(C_f L_1 L_2 s^2 + (L_1 + L_2))}. \quad (11)$$

The transfer function of the grid inductor grid current (i_2) by the grid voltage source (U_g) is given by

$$G_{vg}(s) = \frac{i_2(s)}{U_g(s)} = -\frac{(s^2 C_f L_1 + 1)}{s(C_f L_1 L_2 s^2 + (L_1 + L_2))}. \quad (12)$$

B. Damped Inner Current Loop Model

Aiming to mitigate the *LCL* natural resonance related to problems without the need of including dissipative resistors, an active damping method is used. In such an approach, active resonance damping gets integrated into the inner current control loop [16]. To save the need for more sensors without the adoption of complicated sensorless resonance damping schemes, one well-known technique is to use the grid-current feedback to provide appropriate resonance damping. This approach can be seen as the insertion of the virtual impedance (Z_s) in a series with the grid inductor L_2 .

The drop caused by the virtual impedance Z_s is included to the model of *LCL* filter presented by block diagrams in Fig. 5(a). By means of a step-by-step rearrangement using the rules of blocks diagram algebra, the Z_s block in Fig. 5(a) is moved to the feedback loop, as shown in Fig. 5(b), where transfer function $G_i(s)$ is represented as the feedback loop transfer function, and is given by [17]

$$G_i(s) = \frac{G_{vg}(s)Z_s}{G_p(s)} = Z_s (s^2 C_f L_1 + 1) = \frac{Z_s}{\omega_z^2} (s^2 + \omega_z^2). \quad (13)$$

By using (13), the transfer function $G_i(s)$ presents a pair of conjugated zeroes at ω_z . In the s -domain, it represents a second-order derivative (s^2) with a high-pass filter action, which may amplify noise at high frequencies, in addition to its magnitude dropping far below zero at a frequency of ω_z and the phase going to 180° .

To avoid the problems of such high-pass filter behavior, the term s^2 is replaced with the transfer function determined by (14). In this transfer function, the s^2 part is simulated only in a frequency range around the resonance frequency ω_c . Frequency analysis is carried out by making $s = j\omega$ in (14) and solving it

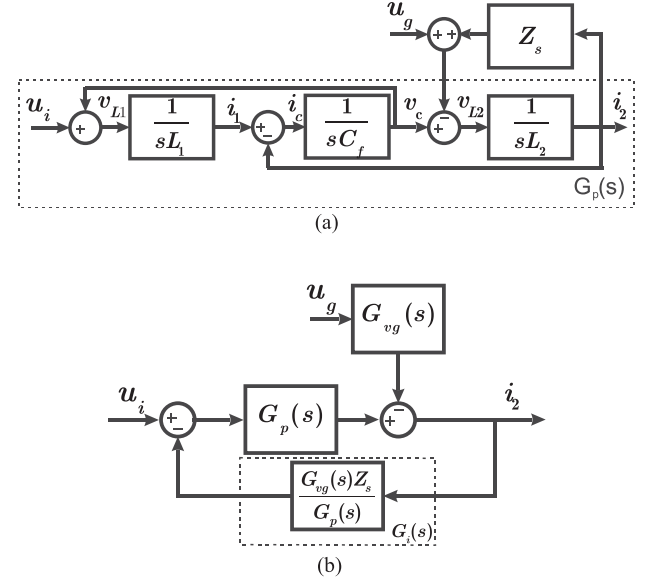


Fig. 5. Block diagram for active damping. (a) $G_p(s)$ with inclusion of impedance Z_s in series with L_2 . (b) $G_{vg}(s)$ and $G_p(s)$ with virtual impedance Z_s in the feedback loop.

for the magnitude (15) and phase (16), as follows:

$$G_a(s) = \frac{\omega_c^2 s^2}{s^2 + \omega_c^2} \quad (14)$$

$$20 \lg |G_\omega(s)|_{s=j\omega} = 20 \lg \frac{\omega^2 \omega_c^2}{|\omega^2 - \omega_c^2|} \quad (15)$$

$$\angle G_\omega(s)|_{s=j\omega} = \angle \frac{\omega^2 \omega_c^2}{\omega^2 - \omega_c^2} = \begin{cases} -180^\circ (\omega < \omega_c) \\ 0^\circ (\omega > \omega_c) \end{cases} \quad (16)$$

Practical realization of (14) implies in the inclusion of the damping term ξ , as shown in (17) and as proposed in [17]. The transfer function of virtual impedance (18) is obtained by just substituting (17) in (13), as this function presents a pair of complex conjugated poles at frequency ω_c

$$G_x(s) = \frac{s^2 \omega_c^2}{s^2 + 2\xi \omega_c s + \omega_c^2} \quad (17)$$

$$G_{sx}(s) = \frac{Z_s}{\omega_z^2} \left(\frac{s^2 \omega_c}{s^2 + 2\xi \omega_c s + \omega_c^2} + \omega_z^2 \right). \quad (18)$$

In order to improve the high frequency attenuation of the feedback loop signal, a first-order low-pass filter $G_f(s)$, given in (19), is inserted. The resulting feedback loop transfer function $G_{fsx}(s)$ (20) is shown in Fig. 6, where the cascade resulting block $G_{sx}(s)$ and $G_f(s)$ present the plant with active damping loop

$$G_f(s) = \frac{1}{\omega_\tau s + 1} \quad (19)$$

$$G_{fsx}(s) = \frac{(C_f L_1 Z_s \omega_c^2 + Z_s) s^2 + Z_s \xi s + Z_s \omega_c^2}{\omega_\tau s^3 + (\xi \omega_\tau + 1) s^2 + (\omega_\tau \omega_c^2 + \xi) s + \omega_c^2}. \quad (20)$$

Fig. 7 presents the frequency response for transfer functions $G_i(s)$, $G_{sx}(s)$, and $G_{fsx}(s)$. The $G_i(s)$ response presents a null

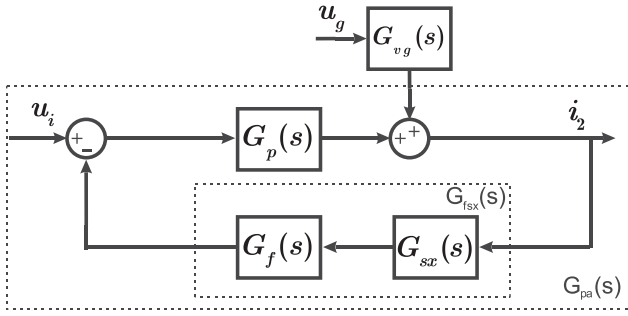
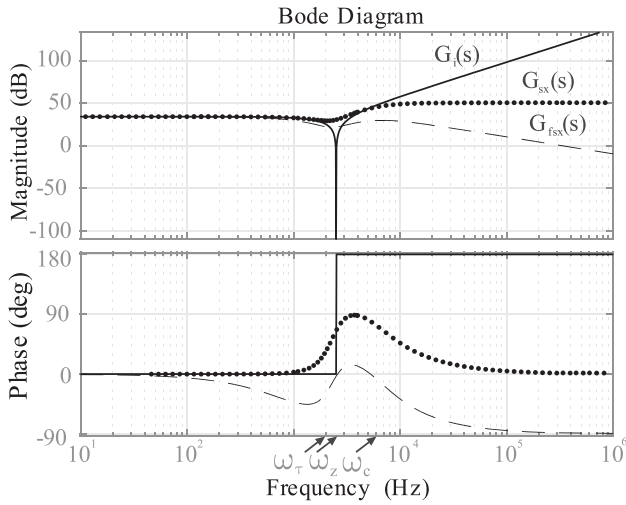
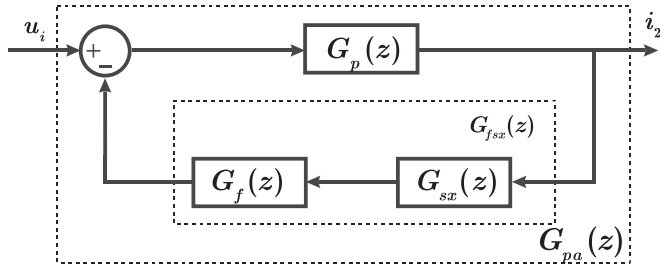
Fig. 6. Block diagram of plant with active damping feedback ($G_{fsx}(s)$).Fig. 7. Frequency response for transfer functions $G_i(s)$, $G_{sx}(s)$, and $G_{fsx}(s)$, where $\omega_z = 12$ kHz, $\omega_c = 2.51$ kHz, and $\omega_c = 4.93$ kHz.

Fig. 8. Discrete time domain block diagram of inner current loop plant with active damping feedback.

magnitude at resonance frequency ω_z due to the transfer function not having any type of damping. The frequency response of $G_{sx}(s)$ shows an attenuation in ω_z ; by including two complex poles at frequency ω_c and driving the $G_{sx}(s)$ phase to zero degrees again, the gain attenuation at high frequencies is not enough.

To solve this issue, the inclusion of a low-pass filter in $G_{sx}(s)$ with cutoff frequency ω_τ lag the phase plus 90° and provide the required high-frequency attenuation.

The inner current loop plant $G_p(s)$ and transfer function $G_{fsx}(s)$ were discretized including a zero order holder approach. Fig. 8 presents the block diagram of closed loop for

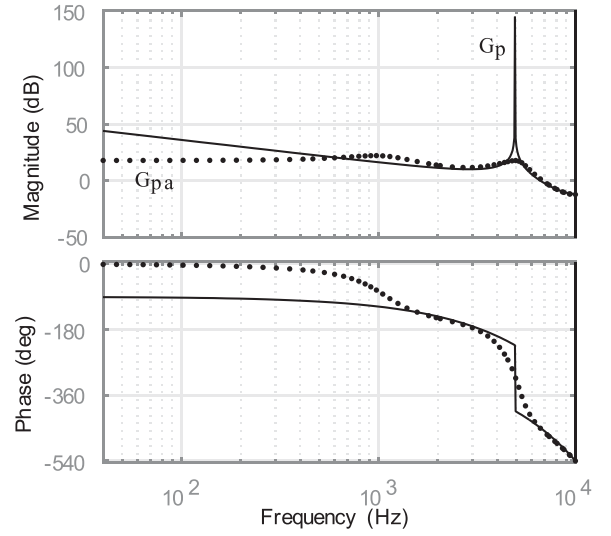
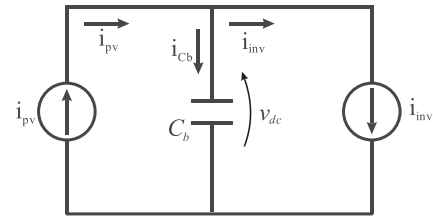
Fig. 9. Frequency response for the open loop damped $G_{pa}(z)$ and undamped $G_p(z)$ transfer functions of the inner current loop.

Fig. 10. Equivalent circuit for the outer voltage loop plant.

active damping, where the sinusoidal input voltage (u_g) is considered a disturbance and can be therefore disregarded [18].

Fig. 9 shows the frequency response for the undamped plant $G_{pd}(z)$ and damped plant $G_{pa}(z)$. The main objective of damping the resonance LCL filter was achieved, although there were differences in low frequencies in gain and phase. To compensate this, a proportional integral (PI) controller will be included in current loop to improve the gain in low frequencies.

C. Outer Voltage Loop

To control the bus voltage V_{DC} and zero steady state error, an outer voltage feedback control loop is used. The outer loop is designed to track the reference signals with zero steady state error. The equivalent circuit for the outer loop can be seen in Fig. 10. It consists of an input current i_{PV} that encompass the low frequency dynamics of the PV panel and the front-end dc-dc converter, an ideal (lossless) bus capacitor C_b , and the current source i_{inv} that represent the dynamics of the inner current control loop.

Considering that the current source i_{inv} represents the current injected into the grid, assuming that the current control loop achieve this propose of unit power factor, it is possible to match the input power supplied by the inverter by (21) and (22). These equations demonstrate that the average voltage value at dc link multiplied by an input average current value is equal to the

effective grid voltage multiplied by an effective grid current

$$\overline{v_{dc} i_{inv}} = V_{g,rms} i_{2,rms} \quad (21)$$

$$\overline{i_{inv}} = \frac{V_{g,rms} i_{2,pk}}{\overline{v_{dc}} \sqrt{2}}. \quad (22)$$

The dynamic analysis of the circuit given in Fig. 10 is carried out with what represents the power balance of capacitor C_b . By applying Kirchoff's Current Law to the circuit, it yields

$$i_{pv} - C_b \frac{d\overline{v_{dc}}}{dt} - \overline{i_{inv}} = 0. \quad (23)$$

Substituting (22) into (23) results in the following:

$$i_{pv} - C_b \frac{d\overline{v_{dc}}}{dt} = \frac{V_{g,rms} i_{2,pk}}{\overline{v_{dc}} \sqrt{2}}. \quad (24)$$

In the small signal model, each variable can be expressed as its constant component (average value) plus a small perturbation. For instance, the following expression shows this representation for the voltage v_{dc}

$$v_{dc} = \overline{v_{dc}} + \widehat{v_{dc}}. \quad (25)$$

By including the perturbation analysis to the variables in (24), and disregarding the dc and high-order terms, the linearized equation is obtained. Finally taking into account that i_{PV} is a disturb, one can find the small signal for v_{dc} as a function of current i_2 as

$$-C_b \frac{d\widehat{v_{dc}}}{dt} = \frac{V_{g,rms} \widehat{i_{2,pk}}}{\overline{v_{dc}} \sqrt{2}}. \quad (26)$$

By applying the Laplace transform in (26) and rearranging the terms of the equation, transfer function $G_{vi}(s)$ is obtained as shown in the following:

$$G_{vi}(s) = \frac{\widehat{v_{dc}}}{\widehat{i_{2,pk}}} = -\frac{V_{g,rms}}{SC_b \overline{v_{dc}} \sqrt{2}}. \quad (27)$$

IV. CONTROLLER DESIGN

A. Current Control

The digital current controller is designed to obtain a good dynamic response, with a good reference tracking and periodic disturbance rejection [21]. To achieve the goals of the controller, some requirements are necessary, such as wide bandwidth and high gain in magnitude for low-order harmonics. An adequate phase margin to ensure stability is also required. The inner current loop is comprised of active damping $G_{pa}(z)$, including zero-order-holder and one-sample delay [19] (see Fig. 11).

The inner current controller transfer function $C_i(s)$ is composed of two different controller blocks in (28). The Proportional-Integral equation (28) is used to increase the magnitude of the plant transfer function at low frequencies and introduce a phase lag of 90° . A multiresonant controller (29) is tuned to track grid reference at 60 Hz to solve the low-order harmonic distortion [22]. The controller is cascaded using an integrator tuned to the desired frequency [20]–[22], and low-order harmonics 3th, 5th, and 7th, where ω_r represents the frequency of interest, index h represents the harmonic order, and constants

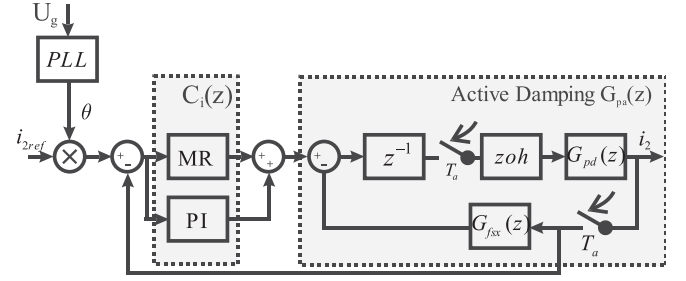


Fig. 11. Block diagram of closed-loop damped current plant with PI-MR controller.

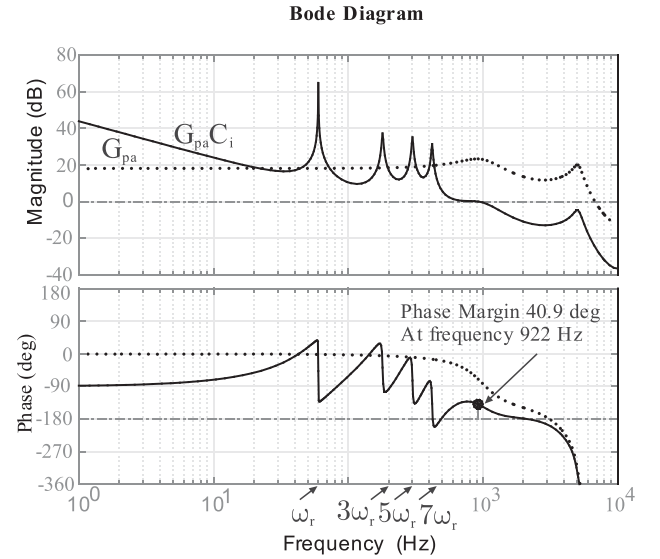


Fig. 12. Frequency response for the compensated and uncompensated inner current plant.

ξ_p and ξ_z are the damping coefficient of poles and zeros used to avoid the infinite gain at resonant frequencies.

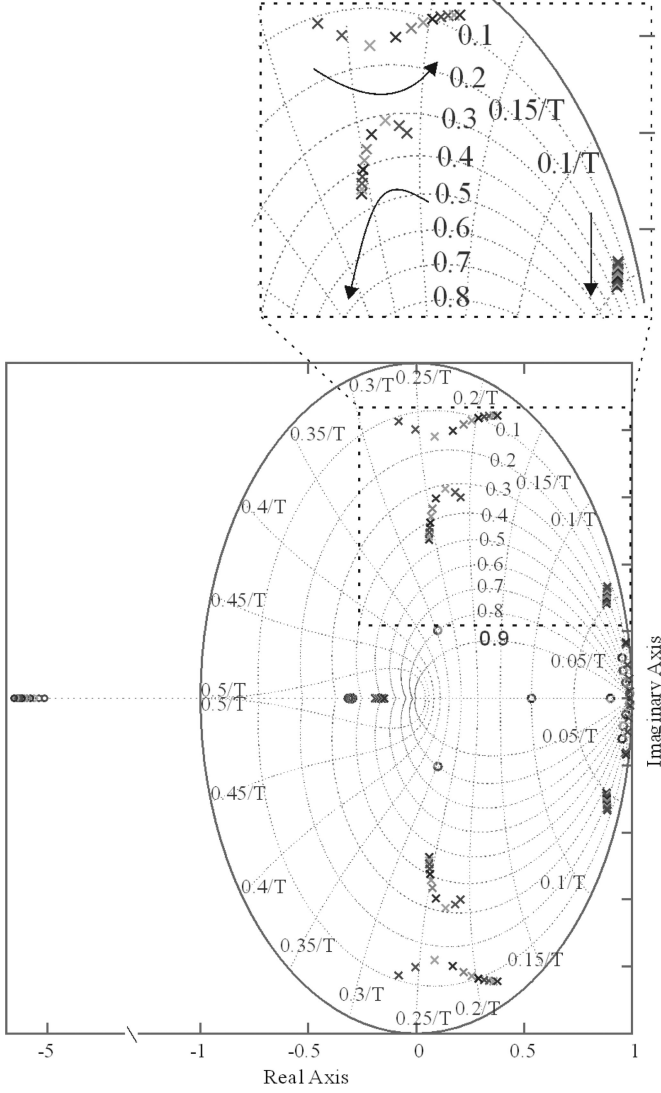
Determination of the grid voltage phase and angle is achieved by making use of a phase-locked loop (PLL) algorithm

$$PI(s) = k_{pi} + \frac{k_i}{s} \quad (28)$$

$$MR(s) = \sum_{h=1,3,5,7} k_h \frac{s^2 + 2\xi_z(h\omega_r)s + h\omega_r^2}{s^2 + 2\xi_p(h\omega_r)s + h\omega_r^2}. \quad (29)$$

Fig. 12 presents the frequency response of the plant with active damping uncompensated $G_{pa}(z)$ and plant including compensator $C_i(z)$, where the achieved margin phase was 40.9° . Additionally, the crossover frequency band width (BW) is 922 Hz and the resonant controller frequencies are 60, 180, 300, and 420 Hz.

1) *Robustness and Parametric Analysis:* The robustness of the controller is an important characteristic. Due to parametric uncertainties concerning the grid impedance and some other disturbances [18], [22]–[23], that may yield variations of the LCL filter natural frequency of resonance, a parametric analysis is necessary.

Fig. 13. Pole-zero map considering parametric variation of inductance L_2 .

In order to evaluate the robustness of the controller, parametric variations from 0 to 100% of L_2 with 10% of increment in each variation was applied to the system. The pole-zero map of grid current closed loop is depicted in Fig. 13. The variation of closed-loop poles is shown in the details demonstrated in the detached rectangle, where arrows indicate the direction of pole variation with the increase of the plant gain. Furthermore, the zeros out of unitary circle demonstrate that the damped plant (G_{pa}) is of nonminimum phase.

Moreover, the robustness of the system in the presence of weak grids is demonstrated, where the poles stay inside of unitary circle in all ranges of variation, demonstrating the stability of system.

B. Voltage Controller

The main goal of the outer loop is to control the bus voltage (v_{Cb}) and provide the reference value for the inner current control loop [24]. Furthermore, the pulsed power oscillations at 120 at the dc bus to be rejected is required [25].

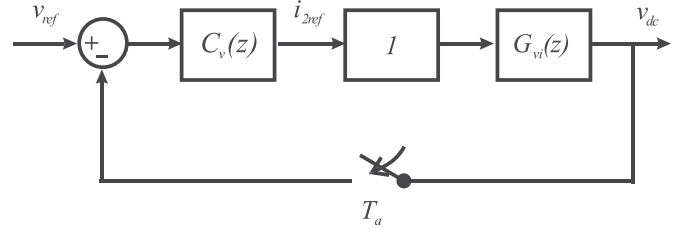


Fig. 14. Block diagram of voltage closed loop.

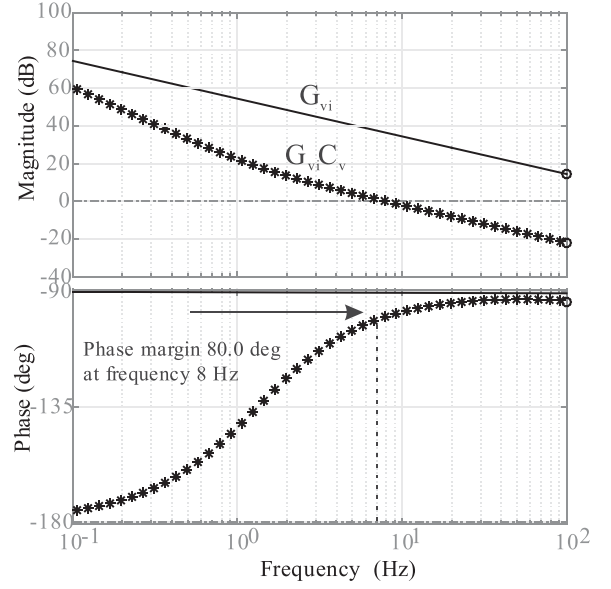


Fig. 15. Uncompensated and compensated voltage plant.

To control the bus voltage V_{DC} , the outer voltage loop feedback is presented in Fig. 14. The voltage controller C_v generated the reference for the internal current loop, which is represented as the unitary block.

Aiming to achieve the abovementioned goals, a PI controller (30) is implemented. It is designed to ensure a null error in steady state with the margin of phase of 80° .

Furthermore, the system bandwidth is designed to present a value lower than 10 Hz, in such a way that the outer and inner feedback loops are decoupled. It also must attenuate consistently the magnitude gain at 120 Hz, avoiding dc-bus voltage oscillations to be inserted in the inner current loop reference

$$C_v(s) = K_{pv} + \frac{K_{iv}}{s}. \quad (30)$$

Fig. 15 shows the open loop frequency response for the uncompensated (G_v) and compensated ($G_{vi}C_v$) plant. It can be seen that the bandwidth is around 8 Hz and the phase margin is close to 80° .

V. EXPERIMENTAL RESULTS

To verify the theoretical analyses, a 200-W buck inverter was implemented in laboratory. The digital controllers were implemented with a Texas Instruments digital signal processor (DSP) TMS320F28335 floating point at 150 MHz 32-b CPU.

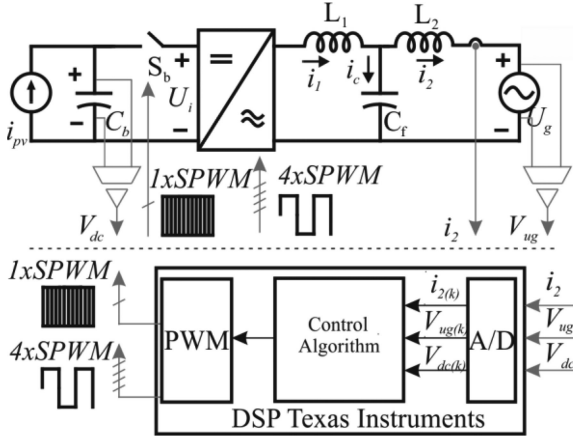


Fig. 16. Hardware implementation.

TABLE II
EXPERIMENTAL VALUES

Parameter	Value	Parameter	Value
Power	200 W	L_1	5.4 mF
V_{in}	400 Vdc	L_2	2.3 mF
V_g	220 RMS	C_f	0.5 μ F
Switching frequency (f_s)	20 kHz	C_b	220 μ F
Sample frequency (f_a)	20 kHz	Grid frequency (f_n)	60 Hz
Resonance frequency (ω_{res})	4.93 kHz	ω_c	$1.1\omega_z$
Z_s	50	ζ	0.7
ω_r	2 kHz	ω_z	2.51 kHz

Fig. 16 presents the hardware implementation, and the sensor readings are obtained through the DSP analogic to the digital converter A/D. Signals obtained from MIC are the bus voltage (V_{dc}), grid source voltage (V_{ug}), and grid source current (i_2). These signals are used by Control Algorithm, which consists of the control loop explained by the block diagrams of Figs. 11 and 14. This algorithm generates the SPWM signals that control the only switch that operates at the high frequency of 20 kHz, and the four switches of unfolding at the low frequency of 120 Hz.

The system parameters are summarized in Table II. The switching frequency (f_s) adopted was 20 kHz, the DSP sample frequency (f_a) was also 20 kHz. The parameters of inner control loops ω_r are defined according to (19), to obtain a cutoff frequency one decade below f_s . Frequency ω_c is the angular frequency of virtual impedance, it is designed to be right above the natural frequency ω_z ($1.1\omega_z$) in order to cancel its effect.

The virtual impedance Z_s is defined with the drop in the active damping control loop [see Fig. 5(a)], as this parameter was adjusted by the bode plot until a good damping response was obtained. The damping coefficient ζ was chosen equal to 0.7, in order to avoid the infinite gain in (17).

The LCL filter design was elaborated according to the work presented in [12], to attend the criterion of resonance frequency of LCL filter.

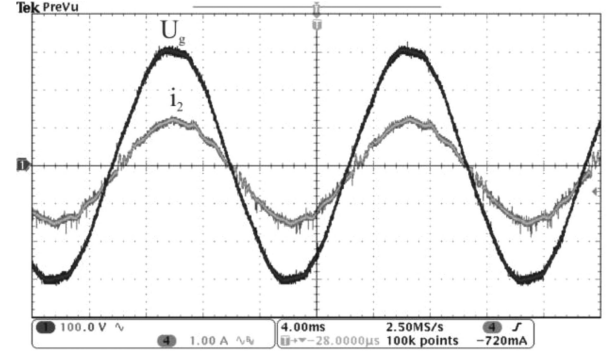
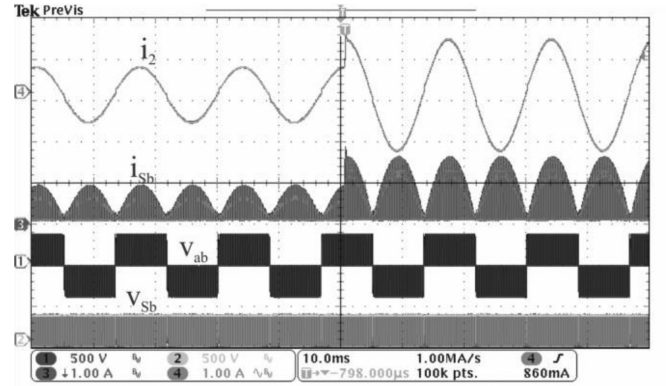
Fig. 17. Experimental waveforms i_2 e V_g .

Fig. 18. Main experimental waveforms with step in grid current reference.

Fig. 17 presents the grid voltage (U_g) and grid current (i_2). The PLL algorithm ensures the unity power factor, guaranteeing that the buck inverter provides a 200-W active power to the grid.

Some disturbances of grid current at zero crossing were also observed. It can be justified by the discontinuous operation of the buck at very light loads. In spite of it, the controller can quickly reject the disturbance every half cycle.

The buck inverter operation can be verified with the waveforms shown in Fig. 18. It shows the unipolar PWM waveform (V_{ab}) applied to the LCL filter as well as the voltage and current through the buck switch. In a way to demonstrate the performance of current controller, the current reference step is also verified in Fig. 18, showing the fast convergence for the new reference value of i_2 .

Fig. 19 presents THD limits according to IEEE Standard 1547 and individual harmonics of current grid (i_2). The measured THD value of 3.7% was obtained from a digital power meter from YOKOGAWA.

The efficiency curve for the buck inverter prototype is shown in Fig. 20 for different solar irradiance values. In accordance with the European efficiency (31), the buck inverter achieved 96.27%. The evaluated points were acquired for an irradiance range from 50 to 1000 W/m²

$$\eta_{EU} = 0,03\eta_{5\%} + 0,06\eta_{10\%} + 0,13\eta_{20\%} + 0,10\eta_{30\%} + 0,48\eta_{50\%} + 0,20\eta_{100\%} \quad (31)$$

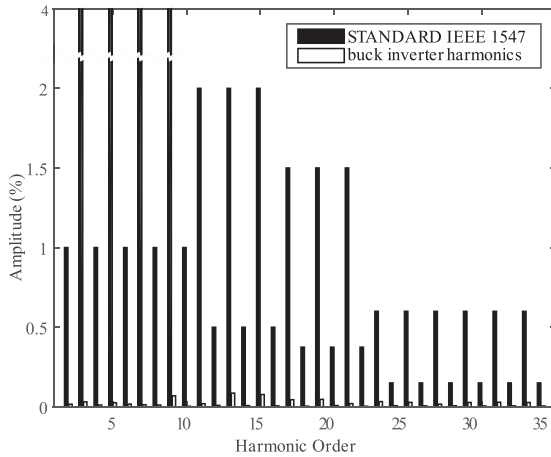
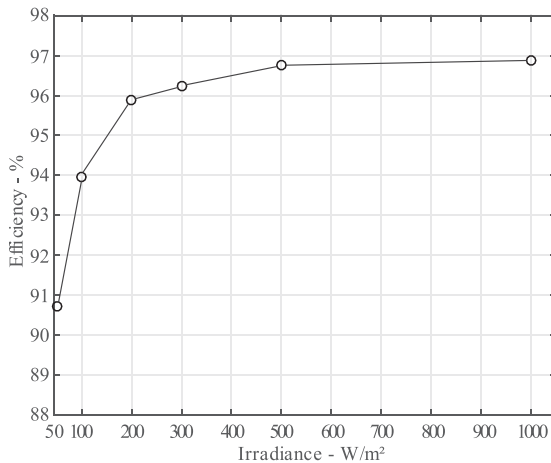
Fig. 19. Harmonic spectrum of grid current i_2 .

Fig. 20. Efficiency curve for the buck inverter against the irradiance.

VII. CONCLUSION

This paper presented and analyzed a new single-phase voltage-fed inverter applied to PV MIC systems. The named buck inverter with *LCL* filter was discussed, designed, and closely analyzed. The main advantage of this topology is that it makes use of a single high-frequency PWM switch with an unfolding H-bridge. The active damping for the *LCL* output filter was achieved by employing an additional grid-current feedback with a new damping impedance function that avoids the need for additional current sensors and handles the high-frequency noise at the measured variable. Furthermore, the active damping does not depend on grid inductance, which means that it works very well with parametric uncertainties at the point of connection with the power grid.

Experimental results obtained from a 200-W prototype showed the very good performance of the buck inverter in transient and steady-state operation. Measured grid current THD complied with IEEE1547 (THD less than 5%) and the European efficiency was 96.27%, which ensures that the buck inverter is a strong candidate to perform as the dc-ac stage for PV MIC systems.

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