

ANPC Inverter With Integrated Secondary Bidirectional Dc Port for ESS Connection

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Abstract—This paper proposes a new inverter topology based on the active neutral-point-clamped (ANPC) converter with capability to integrate one energy storage system (ESS) per inverter leg with an independent state of charge control, so that each inverter leg has two dc ports and one ac port. The primary dc port is common to all inverter legs and it is connected to the main power source. The secondary dc port is suitable for ESS connection because of its two-quadrant operation, with bidirectional current capability, so that the ESS can be charged and discharged with regulated current. Integration of a secondary dc port with independent control also allows the use of different ESS technologies for each inverter leg to compose a hybrid ESS. Redundant switching states of the proposed structure are used to balance the energy exchanged between the secondary dc port and the dc bus capacitors. Theoretical propositions were experimentally validated through a 1-kW single-phase inverter with a secondary dc port connected to a 230-V ESS and ac port connected to an LC filter feeding a linear load. Low total harmonic distortion (THD) sinusoidal current is generated at the ac port while charging or discharging the ESS with a constant current.

Index Terms—Active neutral-point-clamped (ANPC) converter, distributed power generation, energy storage, integrated secondary Dc port, multilevel voltage source inverter (VSI).

I. INTRODUCTION

THE efforts to reduce the use of fossil fuels for electricity generation are resulting in an increasing penetration of renewable energy sources (RES), mainly photovoltaic (PV) and wind. The distributed generation is changing the management of the grid to a more distributed scheme and introduces several challenges that must be carefully addressed due to the stochastic

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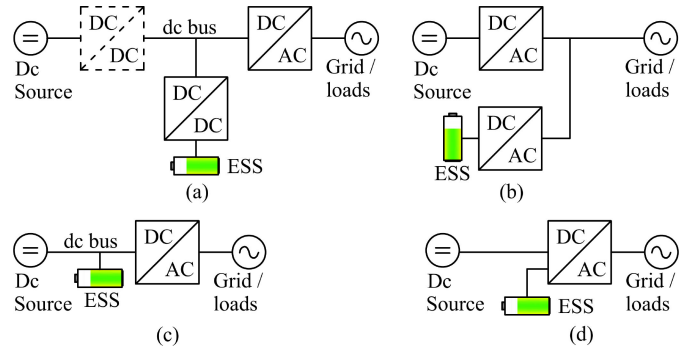


Fig. 1. Main configurations for connection of the ESS. (a) Connection to the dc bus of the inverter through a bidirectional dc–dc converter. (b) Connection to the ac bus through a dedicated inverter. (c) Connected directly to the dc bus. (d) Connected directly to the inverter topology.

nature of these energy sources. For instance, energy storage systems (ESS) can be used to minimize the effect of the RES power variations and to add other functions, such as load leveling, energy arbitrage, primary frequency regulation, and end-user peak shaving [1].

The ESS is an auxiliary system connected to a main power system. The connection configuration defines the ESS voltage and current level, the arrangement of storage elements, the configurations of dc–dc and dc–ac converters, modulation and control schemes, etc. Moreover, the use of different ESS technologies, composing a hybrid ESS (HESS), is a solution for systems that present high power peaks and need high energy storage capacity, in order to maximize ESS life cycle and meet design specifications [2]. HESS combines high-power quick response devices with high-energy slow response devices [1]. HESS configurations can add more converters to the circuit and complexity to the modulation and control systems.

In the industry and literature, the most common way of ESS connection is using a dedicated dc–dc or dc–ac converter as can be seen in Fig. 1(a) and (b). Power converters are used to adapt the ESS output voltage and current to the required levels at the interconnection point (dc bus and ac bus, respectively).

Connection presented in Fig. 1(c) is obtained with the ESS directly connected to the dc bus. The neutral-point-clamped (NPC) converter is reported in the literature as an example of inverter topology suitable for the direct connection of HESS in the dc bus [3]–[6]. In this case, the modulation must be designed to generate balanced sinusoidal currents from an unbalanced dc bus. In [3], a space vector modulation and control system were proposed to simultaneously generate sinusoidal currents

and control the HESS state of charge (SOC). In [5], the NPC inverter with ESS connected to the dc bus is presented for a PV application, and the control system was able to control the power flow between the PV, battery, and grid, and simultaneously provide maximum power point tracking (MPPT) operation for the PV array. A microgrid application of a four-leg NPC inverter featuring an HESS connected directly to the dc bus was presented in [6]. Disadvantages of the operation with an unbalanced dc bus is related to the modulation system that requires complex calculations, and most of them need to be done in real time, higher voltage over the switches due to the unbalanced dc bus, and the NPC converter is limited to the connection of two types of ESS.

Another option for ESS connection is depicted in Fig. 1(d). In this case, the inverter circuit must present a degree of freedom and appropriate circuit nodes for ESS connection. Few topologies exhibit these characteristics. The Z-source inverter (ZSI) [7] is also capable of ESS integration exploring the shoot-through state [8]–[10]. The disadvantage of the ZSI is related to its limitation to integrate more than one ESS in the same inverter.

Therefore, this paper proposes a new converter topology, based on the active NPC (ANPC) converter, which can integrate one independent ESS per inverter leg, and control the ac power dispatch to the grid or local loads. Each inverter leg has a main dc port, common to all legs, a secondary bidirectional dc port, and an ac port. Moreover, the secondary dc port of each inverter leg is controlled independently, using the redundant switching states of the inverter. The power flow of each port is controlled separately, allowing MPPT, ESS charge or discharge and to feed power to the grid (or loads). Therefore, in a three-phase system, for example, an HESS can be created connecting different ESS technologies to each leg. Despite the enormous possibilities, the proposed structure requires a simple carrier-based modulation scheme and a classic control system.

This paper is organized as follows: ANPC inverter is reviewed and the fundamentals of the proposed topology are presented in Section II. Section III presents the modulation strategy and Section IV deals with the control system. Section V is devoted to comparing the proposed topology with other solutions. Experimental results are presented and discussed in Section VI. These results prove the effectiveness of the proposed topology and the capability of independent control of the secondary dc port.

II. DESCRIPTION OF THE TOPOLOGY

The ANPC inverter was first proposed in [11] as an improvement of the NPC inverter [12], which exhibits unequal distribution of losses among the semiconductor devices [13], [14]. Fig. 2 shows a simplified schematic of the ANPC voltage source inverter (VSI), composed of six switches with anti-parallel diodes per leg and a symmetric dc bus. The circuit can produce three levels, $+V_{dc}/2$, zero, and $-V_{dc}/2$. All the switching states for the ANPC VSI reported in the literature are shown in Table I, where the subscript x is the phase index ($x = a, b, c$). In [13], only states P, N, 0U1, 0U2, 0L1, and 0L2 were considered. New switching states were proposed in [15], namely, here 0U3 and 0L3, and other switching states were presented in [16], namely,

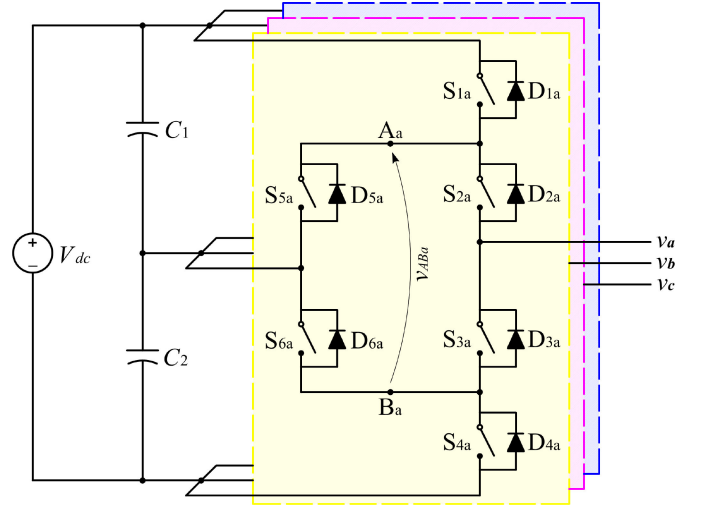


Fig. 2. Three-phase ANPC VSI circuit highlighting voltage across nodes A and B.

TABLE I
SWITCHING STATES OF THE THREE-LEVEL ANPC VSI

State	Switches						v_x	v_{ABx}
	S_{1x}	S_{2x}	S_{3x}	S_{4x}	S_{5x}	S_{6x}		
P	1	1	0	0	0	1	$V_{dc}/2$	$V_{dc}/2$
0U4	0	1	1	0	1	0	0	0
0U3	0	1	0	0	1	1	0	0
0U2	0	1	0	0	1	0	0	—
0U1	0	1	0	1	1	0	0	$V_{dc}/2$
0UL	0	1	1	0	1	1	0	0
0L1	1	0	1	0	0	1	0	$V_{dc}/2$
0L2	0	0	1	0	0	1	0	—
0L3	0	0	1	0	1	1	0	0
0L4	0	1	1	0	0	1	0	0
N	0	0	1	1	1	0	$-V_{dc}/2$	$V_{dc}/2$

here 0U4 and 0L4. State 0UL was not considered by [13] due to the difficulty of predicting losses in the power semiconductors. Nevertheless, in [15], the state 0UL was used to simplify the modulation scheme and to increase efficiency.

Most published papers about the ANPC converter concentrate efforts on modified or improved modulation strategies to reduce and/or distribute the losses in the semiconductors [15]–[18], regulation of neutral point voltage [19], performance evaluation considering the use of specific power semiconductors or applications [20]–[22], and fault-tolerant operation [23]. This paper does not aim the distribution of losses but the addition of new functionality to the ANPC inverter.

Analyzing all the possible switching states and evaluating the voltage between nodes A_x and B_x (v_{ABx}) of Fig. 2, one can observe that two voltage levels can be synthesized. There are five states that produce a zero level on v_{ABx} and four states that produce $V_{dc}/2$ level, as can be seen in Table I. Since there are no redundant switching states for P and N, $v_{ABx} = V_{dc}/2$ during these states. On the other hand, there are nine redundant switching states for the zero level on v_x : five produce zero voltage on v_{ABx} , two produce $V_{dc}/2$ and two (0U2 and 0L2)

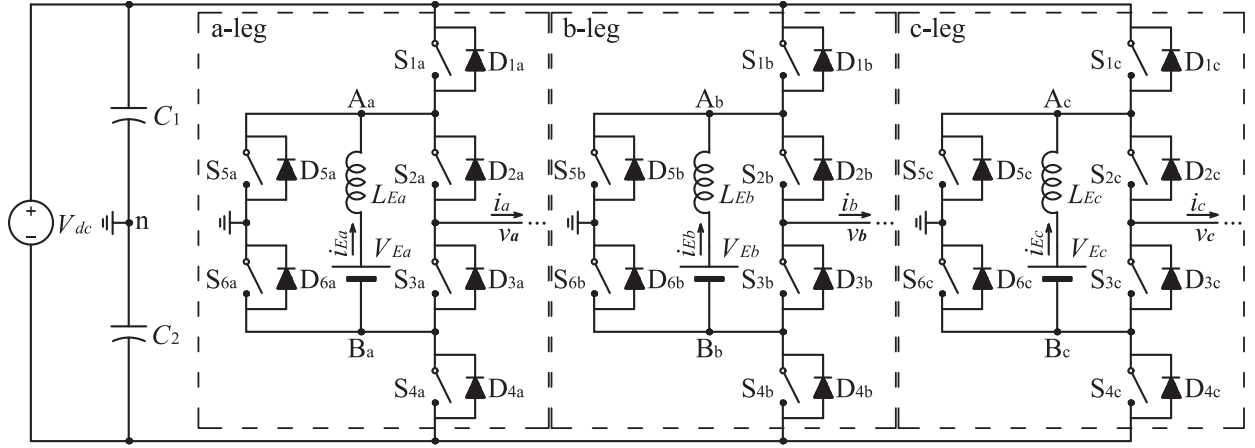


Fig. 3. Proposed three-phase ANPC-3P inverter with one independent ESS per inverter leg.

produce a voltage level on v_{ABx} that depend on the current polarity, so that they are not considered in the following analysis.

Choosing the appropriate time intervals for levels zero and $V_{dc}/2$ in v_{ABx} during zero level on the ac output voltage v_x , one can control the electrical parameters of a circuit connected between nodes A_x and B_x . With these considerations, a new inverter topology can be defined, including: a main dc source, common to all legs, represented by the voltage source V_{dc} , one ac output v_x , and one independent secondary dc port at the terminals A_x and B_x for each leg. Fig. 3 presents a three-phase inverter featuring three-port ANPC (ANPC-3P) inverter legs. Each inverter leg can be connected to an independent ESS.

The inductor L_{Ex} was inserted to allow the energy transfer from/to a voltage-source ESS connected to the secondary dc port with a limited current ripple. Other filter arrangements can be used to filter i_{Ex} , such as an LCL structure. The proper filter choice depends on the type of the source or load and on the design specifications. In some types of ESSs, which exhibit current source behavior, for example, the superconductive magnetic energy storage [1], the filter L_{Ex} is not necessary. In this paper, a simple inductive filter is considered to connect a voltage-source ESS, simplifying the analysis. Higher order filters, such as an LCL structure, should be considered to reduce filter volume.

In addition, due to the dv/dt associated to the nodes A_x and B_x , one can split the inductor L_E in two parts and add common-mode capacitors connected through the ESS terminals and the neutral point to reduce EMI.

In the following analysis, only a single-phase ANPC-3P inverter is considered. Each inverter leg has independent control of the secondary dc port. Thus, the results of the single-phase analysis can be extended for systems with any number of phases or legs. To simplify the notation, hereafter the subscript x is removed from the symbols associated with the secondary dc port.

A. Controllability of i_E

To control the power flow between V_E and the converter circuit, the current i_E must be controlled. This is possible if the

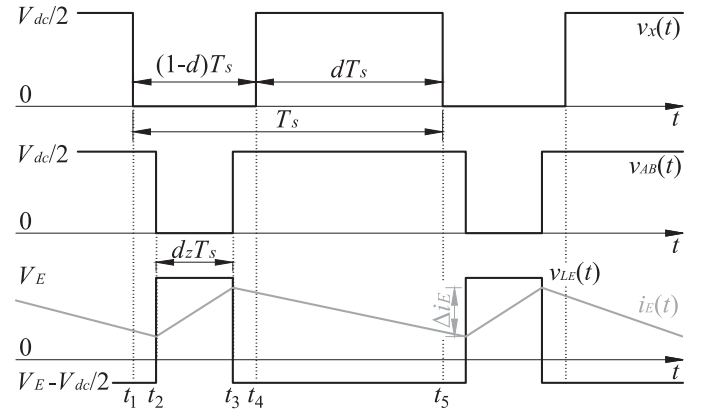


Fig. 4. Waveforms detailing the modulation of the secondary dc port.

average value of the voltage through L_E (v_{LE}) in a switching period T_s is zero. When the ac port uses the P or N state, interval $dT_s = t_5 - t_4$ in Fig. 4, there is no other possible level unless $V_{dc}/2$ to be applied on v_{AB} . In this case, the voltage through L_E is $V_E - V_{dc}/2$. When the ac port generates a zero level on v_x , interval $(1-d)T_s = t_4 - t_1$ in Fig. 4, it is possible to generate zero or $V_{dc}/2$ on v_{AB} . It is possible to find the time interval of the zero level on v_{AB} , represented by $d_z T_s$, applying the volt-second balance to the inductor L_E , resulting in

$$d_z = 1 - \frac{V_E}{V_{dc}/2}. \quad (1)$$

This zero level occurs during the interval $d_z T_s = t_3 - t_2$. In the intervals t_1 to t_2 and t_3 to t_4 , the switching state 0U1 or 0L1 can be used to generate zero level on v_x and maintain $V_{dc}/2$ on v_{AB} .

From waveforms shown in Fig. 4, one can observe that d_z can be adjusted according to the dc bus and ESS voltages in the following range:

$$0 < d_z < 1 - d \quad (2)$$

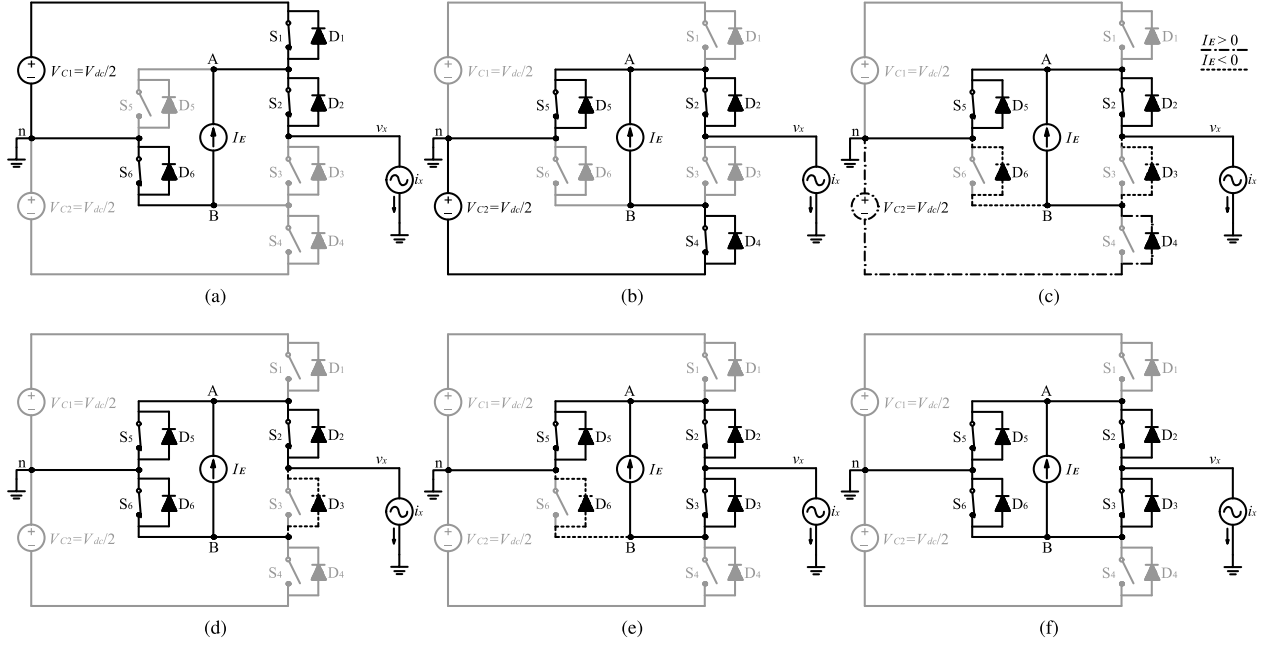


Fig. 5. Switching states (a) P, (b) 0U1, (c) 0U2, (d) 0U3, (e) 0U4, and (f) 0UL.

where, from the steady-state analysis of the ac port, d can be given by

$$d = \frac{\langle v_x(t) \rangle T_s}{V_{dc}/2} \quad (3)$$

and $\langle v_x(t) \rangle T_s$ is the average voltage synthesized by the inverter over one switching cycle.

The worst case to regulate the current i_E occurs at the peak value of the average voltage synthesized by the ac port (V_p), where d reaches its maximum value (d_{max}) and the zero level on v_x has its minimum time interval. Then, by substituting (1) and (3) in (2), it is possible to demonstrate that

$$V_p < V_E < V_{dc}/2. \quad (4)$$

If V_E is higher than $V_{dc}/2$, the voltage through L_E is always positive. If V_E is less than V_p , the term $V_E (1 - d) T_s$ is insufficient to compensate $(V_E - V_{dc}/2) d T_s$ and a low-frequency ripple appears. On the other hand, V_E can be higher than V_p due to the redundant switching states that allow the level $V_{dc}/2$ to be applied on v_{AB} during a zero level on v_x .

This range of V_E is also important to the design process. It can be used to accommodate the ESS voltage variation due to SOC and series resistance of the ESS. Duty cycle d_z should be adjusted to track the V_E changes.

B. Analysis of the Switching States

Despite many papers had done an extensively analysis about the ANPC switching behavior [13], [16], [17], [21], the inclusion of a current source between nodes A and B requires a new analysis.

The analysis of the switching states is presented assuming a current i_E with small ripple, so that the series connection of

L_E and V_E can be replaced by a current source (I_E). Current i_x is considered an ideal sinusoidal current source. The circuit is considered in steady state with currents i_x and I_E flowing through the circuit. Voltages on C_1 and C_2 are considered regulated at $V_{dc}/2$ and are represented by ideal voltage sources V_{C1} and V_{C2} , respectively.

Due to the symmetry of the inverter topology, only the switching states associated with the synthesis of the positive output level $+V_{dc}/2$ and zero output level through the upper conduction path (S_2 – S_5) are considered in the following analysis. This analysis can be extended to the remaining states.

The term switch is used through the text to describe the antiparallel association of a controlled switch with a diode. Positive currents are conducted by the controlled switch and the diode conducts negative currents.

Assuming these hypothesis, one can observe from Fig. 5(a) that switches S_1 , S_2 , and S_6 are conducting during state P. Diodes D_3 , D_4 , and D_5 are reverse biased. Current through the switches are $i_{S1} = i_x - I_E$, $i_{S2} = i_x$, and $i_{S6} = I_E$. The higher current stress on S_1 occurs for a concomitant positive peak of i_x and negative maximum of I_E (i.e., ESS recharging). It is important to note that in this state, there is a connection between V_{C1} and nodes A and B. Therefore, I_E exchanges energy with the positive dc bus (C_1).

State 0U1 is a very important switching state and it connects V_{C2} to the nodes A and B, as depicted in Fig. 5(b), while a zero level is generated on v_x . Switches S_2 , S_4 , and S_5 are conducting. Diodes D_1 , D_3 , and D_6 are reverse biased. Current through the switches are $i_{S2} = i_x$, $i_{S4} = -I_E$ and $i_{S5} = I_E - i_x$. The higher current stress on S_5 occurs for a concomitant maximum value of I_E and negative peak value of i_x . State 0L1 is redundant to 0U1 in terms of voltage levels applied to v_x and v_{AB} , but it allows the connection of V_{C1} to the nodes A and B. These states

allow modulation and control schemes to choose which dc bus exchanges energy with I_E and, therefore, plays a key role in this topology.

Switching states 0U2 and 0L2 have only two switches turned ON. As shown in Fig. 5(c) for the state 0U2, with only two switches turned ON, it is not possible to maintain the same voltage across v_{AB} for any value of I_E . Assuming $i_x = 0$ to simplify the analysis, for $I_E > 0$ diode D_4 is forward biased and conducts I_E . As a result, v_{AB} is $V_{dc}/2$. However, with $I_E < 0$ diodes D_3 and D_6 are forward biased and v_{AB} is zero. This is clearly an undesired condition and thus states 0U2 and 0L2 should not be used on the ANPC-3P inverter.

States 0U3 and 0U4 are very similar and they generate zero level on v_x and v_{AB} simultaneously. The difference of these states relies on the path used for I_E . As depicted in Fig. 5(d), 0U3 uses the left path (S_5 – S_6). And, in turn, 0U4 uses the right path (S_2 – S_3), as shown in Fig. 5(e). In both states only one inner switch is turned OFF, S_3 for 0U3 and S_6 for 0U4. Nodal analysis on S_3 shows that $i_{S3} = I_E - i_x$. Considering state 0U3, if i_{S3} becomes negative, diode D_3 is put into conduction state. The same applies to diode D_6 in 0U4 when $i_{S6} = I_E + i_x$ becomes negative. When these diodes are conducting, the upper and lower current paths are connected in parallel. The exact division of the currents are difficult to estimate and depends on several factors [13]. Therefore, the drawback of using these switching states is the difficulty to estimate losses on the inner switches.

Considering the possibility to connect the upper and lower current paths in parallel, state 0UL forces the parallel connection by turning ON the four inner switches simultaneously, as shown in Fig. 5(f). The upper and lower current paths, as well as the left and right current paths, are put in parallel regardless of I_E and i_x values. In [15], the state 0UL was used to improve efficiency and the losses were evenly distributed among the inner switches.

C. Analysis of the Commutations

There are basically three types of commutations between switching states, namely as: types I, II, and III. For type I commutation, only one switch is turned OFF and after a deadtime another switch is turned ON. This commutation is simple and it does not present major problems. An example of type I commutation is $P \leftrightarrow 0U3$.

Type II commutations are characterized by turning OFF two switches and, after, one or more switches are turned ON. Commutations of type II always involve to turn OFF S_1 or S_4 and commute other inner switches, for example, $P \leftrightarrow 0U4$, $0U1 \leftrightarrow 0L3$, among other commutations. If one choose to turn OFF before the deadtime all the switches that must turn OFF, the inner switches that remain turned ON may not guarantee the voltage levels in the dc and ac ports. When S_1 and S_4 are in the OFF state, inner switches can be commutated simultaneously without deadtime because there is no risk of short-circuiting the dc buses. Therefore, a better commutation strategy is to first switch S_1 or S_4 OFF, follow with a deadtime, and then commute inner switches.

Type III commutations are more complex and involve commutation of S_1 and S_4 , one of them turning OFF and the other

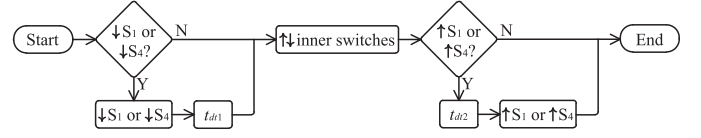


Fig. 6. General flowchart for commutations.

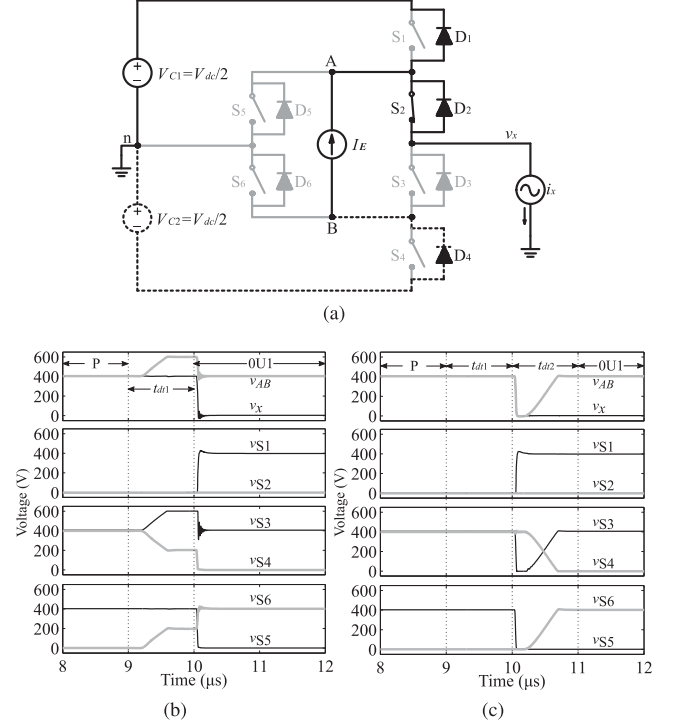


Fig. 7. (a) Circuit representing a possible overvoltage across S_3 during commutation $P \leftrightarrow 0U1$ dead time. (b) Spice simulation of commutation $P \leftrightarrow 0U1$ using single dead time. (c) Spice simulation of commutation $P \leftrightarrow 0U1$ using the proposed two dead time procedure.

turning ON. Type III commutations are: $P \leftrightarrow 0L1$, $N \leftrightarrow 0L1$, and $0U1 \leftrightarrow 0L1$. In a first step, the same procedure of type II commutation is executed, i.e., S_1 or S_4 is turned OFF and followed by a deadtime. Then, inner switches are commutated. To complete the commutation S_1 or S_4 need to be turned ON after a second deadtime. To better understand the necessity of a second dead time, consider the case of $P \rightarrow 0U1$. The first step is to turn OFF S_1 . After a deadtime S_6 is turned OFF and S_5 turned ON simultaneously. A deadtime must follow the commutation of the inner switches to avoid a short-circuit on the negative dc bus caused by the path S_4 – S_6 . A general procedure for commutations is proposed and it is shown in the flowchart of Fig. 6, which is valid for any commutation, where $\uparrow$ and $\downarrow$ indicates to turn ON and turn OFF a switch, respectively.

The use of two deadtimes helps to avoid other problems that can occur in intermediary switching states, which must ensure secure paths to I_E and i_x . Otherwise, destructive voltages can occur in some switches. Consider, for example, type III commutation $P \leftrightarrow 0U1$ again. If S_1 and S_6 are turned OFF simultaneously, only S_2 remains in conduction during the deadtime between the S_1 turn-off and S_5 turn-on. Fig. 7(a) shows the converter current paths in this situation. If the current through S_1 is negative, diode

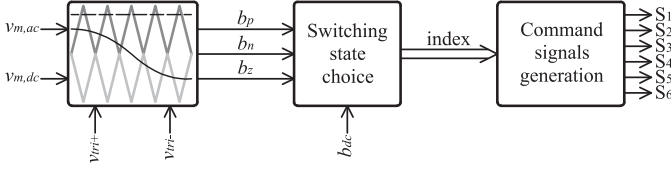


Fig. 8. Modulation block diagram.

D_1 remains in conduction during deadtime, I_E forces D_4 to turn ON and the total dc bus voltage V_{dc} appears across S_3 . Fig. 7(b) presents an LTSpice simulation using an IGBT IRGP50B60pd1 spice model, $I_E = 10$ A, $i_x = -10$ A, and $V_{dc}/2 = 400$ V. It is possible to see voltage across S_3 reaching its breakdown value of 600 V during deadtime. Another simulation was done using the proposed two deadtimes procedure and the results are shown in Fig. 7(c). As can be seen, using two deadtimes the voltages across all switches are clamped to $V_{dc}/2$. However, an undesired pulse ($V_{dc}/2 \rightarrow 0$) on v_{AB} occurs during this process.

The undesired pulse on v_{AB} is relatively simple to understand if one consider that in the P state the voltage v_{AB} is imposed by the positive dc bus and in the 0U1 state is imposed by the negative dc bus. Commutation P $\rightarrow$ 0L1 does not have the undesired commutation pulse because only the positive dc bus imposes the voltage v_{AB} (S_1 remains in conduction). Commutation P $\rightarrow$ 0U1 (type III) initially causes S_1 to turn OFF. As can be seen in Fig. 7(c), during first deadtime (t_{d1}), there is no change in the current paths and voltages v_x and v_{AB} are kept constant, since the S_1 current is negative and D_1 is conducting. At the end of the first deadtime, S_6 is turned OFF and S_5 is turned ON. Since the node B was initially connected to the neutral point potential through S_6 and switch S_5 instantaneously connects node A to neutral point, at this instant v_{AB} is undesirably commutated to zero. During the second deadtime, during S_6 turn-off and S_4 turn-on, D_4 starts conducting I_E and the voltage on node B falls to $-V_{dc}/2$. At this time v_{AB} returns to $V_{dc}/2$. Depending on the values of I_E and i_x , a similar process can occur in the first deadtime. In addition, a similar situation occurs for the commutation 0U1 $\rightarrow$ P. It is important to note that this pulse is very fast and has a negligible effect on the ESS current control.

III. MODULATION STRATEGY

A simple method for ac port and secondary dc port modulation for the ANPC-3P inverter is presented in this section.

Fig. 8 presents a block diagram for the modulation system and Fig. 9 shows the main waveforms associated to this modulation strategy. The first block generates three digital signals resulting of the comparison of modulating signals $v_{m,ac}$ (ac output) and $v_{m,dc}$ (secondary dc port) with the carriers v_{tri+} (positive carrier) and v_{tri-} (negative carrier), which are in phase opposition disposition [24]. Other carrier dispositions could be used, but they are not considered in this paper. When $v_{m,ac}$ is greater than v_{tri+} and v_{tri-} , b_p is high and P state must be selected in the second block. When $v_{m,ac}$ is lower than v_{tri+} and v_{tri-} , b_n is high and N state must be selected in the second block. When b_p and b_n are simultaneously low, a zero level must be applied on v_x and the modulation of the secondary dc port takes place.

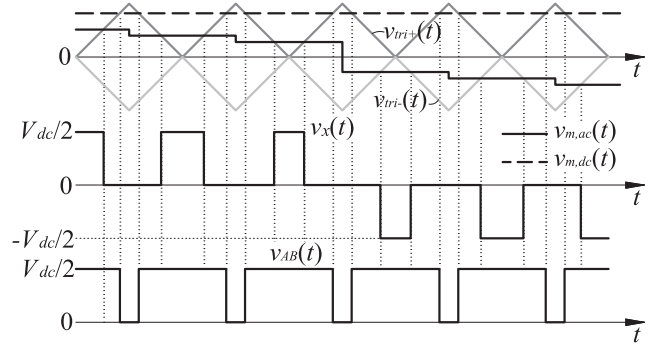


Fig. 9. Main waveforms of the modulation strategy.

When $v_{m,dc}$ is lower than v_{tri+} , b_z is high and a zero level is applied on v_{AB} . On the other hand, when $v_{m,dc}$ is greater than v_{tri+} , b_z is low and a $V_{dc}/2$ level is generated on v_{AB} . As can be seen in Fig. 9, after v_x was switched to zero, level $V_{dc}/2$ is maintained on v_{AB} . This is done using state 0U1 or 0L1. After, zero level is applied on v_{AB} using one of the five zero redundant states 0U3, 0U4, 0UL, 0L3 or 0L4. Completing the pulse on v_{AB} a level $V_{dc}/2$ is applied on v_{AB} using state 0U1 or 0L1 again. Next, a pulse $\pm V_{dc}/2$ is generated on v_x and the cycle is repeated.

The intermediary block in Fig. 8 is responsible to select the appropriate switching state according to the voltage levels requested by the first block and by the signal b_{dc} . As mentioned before, there are redundant switching states for level zero on v_x , as well for zero and $V_{dc}/2$ levels on v_{AB} . The intermediate block is programmed to select the appropriate redundant state to achieve one or more objectives. Redundant state selection is considered further in a specific section.

The intermediary block tells to the third and last block as to which switching state should be used to generate the command signals of the switches. This is done through an index that selects the corresponding state in the Table I. The last block execute the commutations following the procedure presented in Fig. 6.

A. Redundant Switching State Selection

Topologies that exhibit redundant switching states give some degrees of freedom to the converter design and operation. For instance, the ANPC inverter is widely investigated in literature considering better loss distribution among semiconductor devices using the redundant states. The inclusion of a secondary dc port exploring the redundant states is proposed in this paper.

When I_E is not zero, it is extremely important to balance the energy exchanged with both dc bus capacitors. States P and N do not present redundant states and current source I_E exchanges energy with C_1 and C_2 , respectively, in these states. However, during the zero level on v_x , the modulation strategy can choose the states 0U1 or 0L1 to generate $V_{dc}/2$ on v_{AB} . State 0U1 creates a path that allows I_E to flow through C_1 , as can be seen in Fig. 5(b). Similarly, state 0L1 creates a path that allows I_E to flow through C_2 . In this way, these redundant states have opposite effect on the dc bus capacitors voltages. Consequently, they are used to control the neutral point voltage. In the next

TABLE II
SELECTION LOGIC OF STATES 0U1 AND 0L1

I_E	V_{C1}	State
> 0	$> V_{dc}/2$	0U1
> 0	$< V_{dc}/2$	0L1
< 0	$> V_{dc}/2$	0L1
< 0	$< V_{dc}/2$	0U1

section, an ON-OFF controller is proposed to generate the signal b_{dc} , which request the switching state to the second block of the modulation strategy.

There are other redundant states that generate a zero level on v_x and v_{AB} , namely 0U3, 0U4, 0L3, 0L4, and 0UL. As discussed before, the first four states presents only one inner switch in the OFF state. The diode of this switch can start conducting for some values of i_x and I_E and put the upper and lower conduction paths in parallel. On the other hand, state 0UL force the parallel connection regardless of current values. Results presented in [15] demonstrate better performance using 0UL state. Moreover, using only one state for the zero level results in a simple modulation scheme.

IV. CONTROL SYSTEM

The control system is very dependent on the application and the type of filters used. Generation of high quality sinusoidal waveform can present some challenges to the control system in off-grid and grid-tied inverters, as very discussed in the literature. For the grid-tied PV inverter, it is necessary to control the currents injected to the grid as well as MPPT, while for a UPS application, the control variables are the sinusoidal output voltages. Since the secondary dc port is the main focus of this paper, the control of the ac side is not considered in this study, leaving the ac output in open loop with a sinusoidal output current.

Considering a simple inductive filter on the secondary dc port, the duty cycle to current transfer function is of first order and given by

$$\frac{I_E(s)}{d_z(s)} = \frac{V_{dc}/(2L_E)}{s + (R_E + R_{LE})/L_E} \quad (5)$$

where R_E and R_{LE} are the series resistances of V_E and L_E , respectively. Control of i_E current can be done by a simple PI controller to achieve a zero steady-state error.

During converter operation, the power exchanged with both dc bus capacitors must be balanced. As mentioned before, states 0U1 and 0L1 allow us to choose which dc bus exchanges energy with I_E . Despite possibilities of doing the selection of these states in open loop, a closed-loop strategy is very simple and requires the measurement of the voltage across one of the dc bus capacitors and measurement of I_E . In most applications, these two measurements are already utilized by other functions causing minimal impact on the system size and cost. Table II presents the resulting redundant state selection based on V_{C1} and I_E information.

Considering the strategy presented in Table II, one can see that for each condition of V_{C1} , there are two possible actions

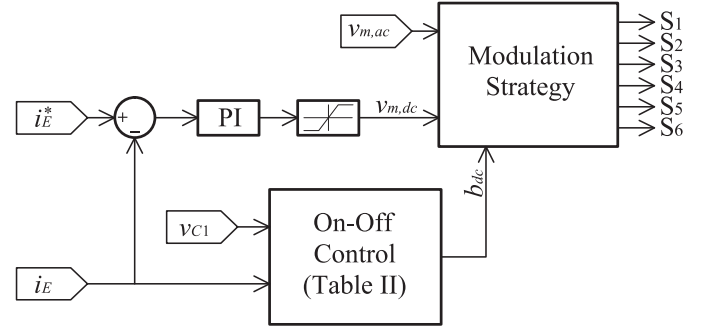


Fig. 10. Control system block diagram.

depending on the I_E polarity. For example, if $V_{C1} > V_{dc}/2$, it is possible to charge C_2 or discharge C_1 to balance the capacitor voltages. The first action can be accomplished through state 0U1 if $I_E > 0$, and the second action is realized using state 0L1 if $I_E < 0$. For $V_{C1} < V_{dc}/2$, the opposite actions can be taken.

In a three-phase configuration, similarly to conventional NPC and ANPC converters, there are redundant switching vectors that generate the same line-to-line ac output voltages, but with opposite effect on the dc bus capacitors voltages [25]. Consequently, these redundant switching vectors can also be used to control the dc bus capacitors voltages, similarly to conventional NPC and ANPC converters.

Fig. 10 presents a block diagram of the control system. In any case, the ac port current or voltage controller can be added and its output is connected to $v_{m,ac}$ input of the modulator. Secondary dc port current is regulated by a PI controller and after saturation the modulating signal $v_{m,dc}$ is connected to the modulator. The ON-OFF controller generates signal b_{dc} using i_E and v_{C1} measurements according to Table II.

V. COMPARATIVE ANALYSIS

This section presents a comparative analysis between two different solutions to connect a main dc source and an ESS to a three-phase utility grid. The first solution (Design 1) is based on the proposed topology and features the integration of the ESS to the main inverter, as illustrated in Fig. 1(d). The second solution (Design 2) features ac bus connection, as shown in Fig. 1(b), using three-phase NPC topologies for the main inverter and for the ESS inverter. For both solutions, the ESSs considered in this analysis is composed of series associations of valve-regulated lead-acid (VRLA) batteries, whose float and cut off voltages are 13.8 V (2.3 V/cell) and 10.5 V (1.75 V/cell), respectively.

The main parameters of both solutions are summarized in Table III. Although the Design 2 gives many degrees of freedom, one can see that it has a higher number of power semiconductors and isolated power supplies. In addition, since the ESS is connected directly to the dc bus, a higher number of series-connected batteries must be used. Therefore, when the ESS voltage variations are taken into account, the voltage stresses across power semiconductors are similar for both ANPC-3P and dedicated ESS NPC converters. On the other hand, Design 1 presents inherent ESS redundancy due to the

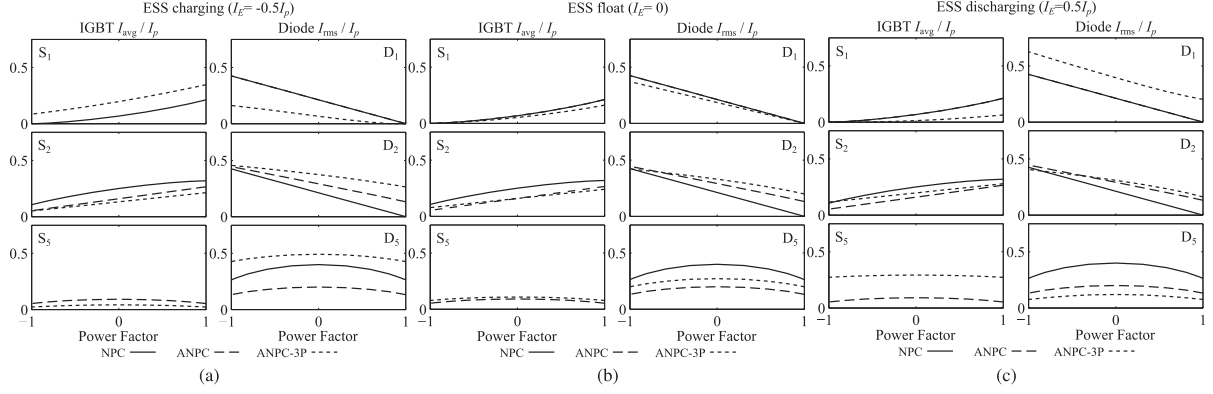


Fig. 11. Simulation results showing current stress of IGBTs and diodes for different power factor and: (a) ESS charging ($I_E = -0.5I_p$), (b) ESS float ($I_E = 0$), and (c) ESS discharging ($I_E = 0.5I_p$).

TABLE III
COMPARATIVE ANALYSIS BETWEEN TWO DIFFERENT SOLUTIONS TO CONNECT
A MAIN DC SOURCE AND AN ESS TO A THREE-PHASE UTILITY GRID
(LINE-TO-LINE GRID VOLTAGE (V_{LL}): 380 V RMS)

Parameter	Design 1 - Fig. 1(d)		Design 2 - Fig. 1(b)	
	Single inverter 3 ϕ ANPC-3P	Main inverter 3 ϕ NPC	ESS inverter 3 ϕ NPC	
Number of IGBTs	18	12	12	
Number of Diodes	18	18	18	
Isolated power supplies	11	10	10	
$V_{E,min}$	$> V_{LL}\sqrt{2/3}$ (350 V)	-	$> 2V_{LL}\sqrt{2/3}$ (650 V)	
Number of series-connected batteries	33 per leg	-	62	
$V_{E,max}$	$33 \cdot 13.8$ V (460 V)	-	$62 \cdot 13.8$ V (860 V)	
$V_{dc,min}$	$> 2V_{E,max}$ (920 V)	$> 2V_{LL}\sqrt{2/3}$ (720 V)	$V_{E,min}$ (650 V)	
Voltage stress	$V_{dc}/2$ (460 V)	$V_{dc}/2$ (360 V)	$V_{E,max}/2$ (430 V)	

splitted ESS configuration. Each ESS has independent control and they can be at different operating modes at the same time. Moreover, different ESS technologies can be used to compose a hybrid solution with extended lifecycle and better performance.

In another analysis, ANPC-3P is compared to the NPC and standard ANPC topologies in terms of current stress. The three topologies are simulated considering ideal semiconductor devices, no deadtime, sinusoidal ac current in the ac side, constant I_E , each pole of dc bus is an ideal voltage source, and ESS is an ideal voltage source. Based on the analysis presented in Table III and considering an inverter output line-to-line voltage equal to 380 V_{rms}, NPC and ANPC converters are simulated with $V_{dc} = 720$ V and the proposed ANPC-3P is simulated with $V_{dc} = 920$ V and $V_E = 350$ V. In addition, output currents are considered independent of the amplitude modulation index and d_z . ANPC topology is simulated using state 0UL as proposed in [15], without the objective to distribute losses. In state 0UL, the currents are considered equally divided across upper and lower paths for i_x , and left and right paths for I_E . Simulation results are

presented in Fig. 11 to demonstrate the impact of the integration of the ESS on the current stresses of the semiconductors. Only the upper switches are considered due to the inverter circuit symmetry and the modulation strategies used. The same results apply to lower switches and diodes. ESS current $I_E = 0.5I_p$ was chosen to result approximately in nominal power for each ESS, where I_p is the inverter phase peak current.

One can observe from Fig. 11(a) (ESS charging) and from Fig. 11(c) (ESS discharging) that S_1 , D_1 , and D_5 present higher current stresses. These are expected results once the inverter is processing ac power plus ESS power. Condition of Fig. 11(c) for PF < 0 (active power flow from ac grid) can be avoided as it is not usual in many applications to have an inverter drawing power from the grid and the ESS discharging at the same time. Condition of Fig. 11(a) for PF > 0 (active power flow to ac grid) almost occur in every application. For some applications, such as renewable generation, this additional current stress on S_1 can be alleviated because the inverter is designed to nominal power of the main dc source. Thus, when the ESS is recharged, the power fed to the grid should decrease. Otherwise, for UPS applications, for example, the ESS can be in recharge mode while the inverter has nominal power at the output. In this case, there will be a higher current stress that need to be taken into account in the designing process.

VI. EXPERIMENTAL RESULTS

Proposed topology and related theoretical propositions have been validated through a single-phase inverter prototype. The main parameters of the prototype are presented in Table IV.

The main dc port V_{dc} is connected to 2×275 V regulated dc power supply. The ac output is filtered by an LC filter that feeds a resistive load of approximately 1 kW in open loop. This filter and load arrangement results in a sinusoidal current such as used in theoretical analysis. Secondary dc port is connected to an ESS composed of 19×12 V VRLA batteries connected in series. Maximum recharge current of the ESS is set to 2 A, following the battery manufacturer recommendation. ESS discharge current is limited to result in maximum ac power, avoiding reverse power in the power supplies connected to the main dc port.

TABLE IV
MAIN PARAMETERS OF THE PROTOTYPE

Parameter	Value
Output ac power (P_o)	1 kW
ESS power (P_E)	1 kW
Dc bus voltage (V_{dc})	550 V
ESS voltage (V_E)	230 V
Ac voltage (V_{ac})	127 V rms
Ac filter inductor (L)	6 mH ($R_s = 0.3 \Omega$)
Ac filter capacitor (C)	1 μ F
Ac load (R)	15 Ω
ESS filter (L_E)	10 mH ($R_s = 0.5 \Omega$)
ESS internal resistance (R_E)	0.5 Ω
Ac frequency (f_{ac})	60 Hz
Carrier frequency (f_c)	10.26 kHz
Sampling frequency (f_s)	10.26 kHz
Switches S_1 - S_6	IGBT IRGP50B60pd1

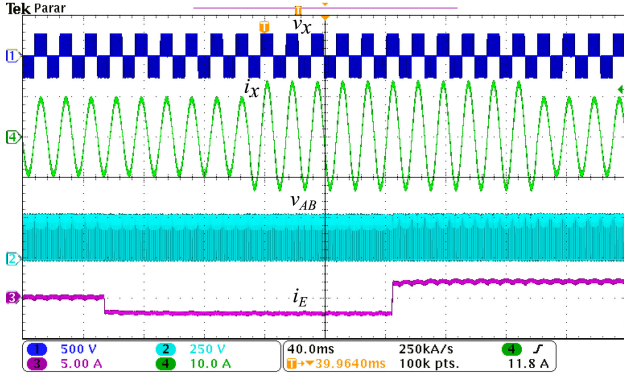


Fig. 12. Experimental results for steps on currents i_x and i_E .

Inductor L_E is designed through its maximum current ripple specification, using

$$L_E = \frac{d_z V_E}{\Delta I_E f_s} \quad (6)$$

A relative high inductance is needed due to the necessity of maintaining small current ripple during ESS float mode and the use of a first-order inductive filter (L_E). Current ripple ΔI_E was chosen to be approximately 0.35 A when $V_E = 230$ V. This current ripple causes minimal temperature rise in the battery, allowing it to be kept connected to the inverter for long periods in float mode. To reduce filter volume a higher order filter such as an LCL structure could be considered.

Modulation and control systems are implemented using the Texas Instruments TMS320F28335 microcontroller. Ac output is kept in open loop and the output current is adjusted using the modulation index. A PI controller is used to control the ESS current. Deadtimes t_{dt1} and t_{dt2} are adjusted to 500 ns.

Fig. 12 initially shows results with current i_E regulated at 0 A. Then, a step of -2 A (ESS recharge mode) occurs and the current is regulated at this reference. As can be seen, there is a high-frequency ripple caused by converter switching and a small low frequency ripple due to low frequency ripple on dc bus capacitors voltages. Afterwards, a step is applied at the ac current by changing the modulation index. In both dc and ac

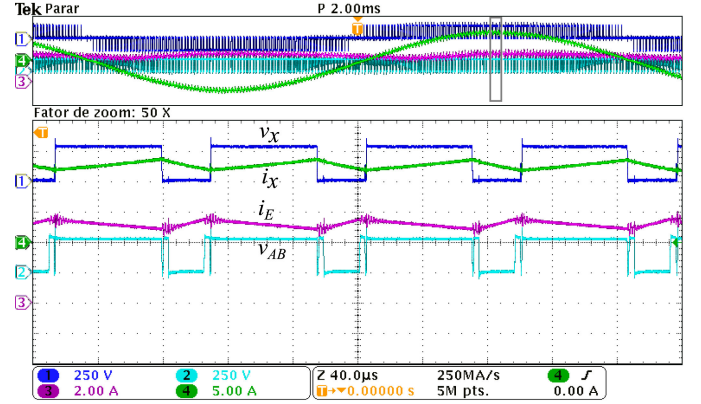


Fig. 13. Experimental results detailing voltages and currents on the ac and secondary dc ports. Current i_x at peak positive value and $i_E = 5$ A.

current steps, the currents do not interfere each other, showing that the modulation of one power port is independent of the other. The last dc current step brings ESS from recharge to discharge mode with 2 A current. As can be seen, the inverter is able to simultaneously generate a sinusoidal current on the ac port and a dc current on the secondary dc port.

Fig. 13 presents details of voltages and currents on the ac and dc power ports for ESS discharging with nominal current of 5 A. It is possible to see fast commutations on v_{AB} when v_x commutates. Voltage v_{AB} goes from $V_{dc}/2$ to zero and back to $V_{dc}/2$. This commutation occurs during deadtime as described in the theoretical analysis. These fast pulses have a negligible effect on the ESS current control.

VII. CONCLUSION

This paper presented a new VSI topology capable of integrating an ESS through a bidirectional dc port.

Switching state and commutation analysis were presented to prove the feasibility of ESS connection between internal nodes of an ANPC converter. Moreover, switch commutation sequence with two deadtimes was also proposed.

Simple carrier-based modulation strategies can be used in the proposed topology and two modulating signals are required, one for the ac port and one for the dc port.

Comparative analysis demonstrated that ANPC-3P requires a higher dc bus voltage in comparison to conventional NPC or ANPC. However, for an NPC design that considers the ESS voltage variation due to SOC and series resistance, the dc bus voltage of ANPC-3P and NPC are similar. In terms of current stress, for the proposed modulation scheme, S_1 , D_1 , and D_5 present higher current stress for some operating modes and applications.

Experimental results obtained through a single-phase 1-kW inverter prototype proved the feasibility of the proposed topology, allowing control of the ESS and simultaneously the generation of sinusoidal current in the ac port. This topology is suitable for applications like UPS, renewable energy generation, and electrical vehicles.

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interests include renewable energy sources, distributed generation, static converters, and digital control.



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