

**SANTA CATARINA STATE UNIVERSITY – UDESC
COLLEGE OF TECHNOLOGICAL SCIENCE – CCT
GRADUATE PROGRAM IN ELECTRICAL ENGINEERING – PPGPEEL**

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**SEMICONDUCTOR GALVANIC ISOLATION BASED DC-DC *BUCK* CONVERTER
FOR BATTERY CHARGING APPLICATIONS**

JOINVILLE

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Master's thesis presented to the Graduate Program in Electrical Engineering of the College of Technological Science of the Santa Catarina State University, as partial requirement for obtention of the title of Master in Electrical Engineering.

Supervisor: Joselito Anastácio Heerdt

Co-supervisor: Frank Weiner Heerdt

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Dedicated to my family!

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“Failure is part of the process of success. People
who avoid failure also avoid success.”
(Robert T. Kiyosaki)

RESUMO

Os carregadores de bateria têm sua importância no vasto e crescente mercado de produtos alimentados a bateria, pois são usados em uma ampla variedade de aplicações. Esses carregadores são comumente encontrados em uma configuração com dois estágios de conversão em alta frequência, sendo o primeiro um estágio AC-DC, geralmente com correção do fator de potência e o segundo, um estágio de DC-DC que provê isolamento e regula corrente e tensão na saída. Este trabalho propõe estudar e projetar o estágio DC-DC de um carregador de bateria voltado para aplicações industriais com Isolamento Galvânico a Semicondutor (SGI), visando adquirir conhecimento sobre esta nova tecnologia na qual, mesmo sem a necessidade de um transformador, permite o isolamento galvânico. Algumas topologias são propostas e a selecionada é então projetada e analisada juntamente com os resultados da simulação. O cumprimento da norma do produto traz, entre outros, critérios de segurança, que orientam a análise sobre isolação galvânica, onde é estabelecida a máxima corrente de toque permitida. Um conversor prático é então montado permitindo resultados experimentais.

Palavras-chave: Isolação galvânica a semicondutor. Conversor Buck. Carregador de bateria. Corrente de toque. Conversor DC-DC.

ABSTRACT

Battery chargers have their importance in the large and growing market of battery-powered products as they are used in an extensive variety of applications. These chargers are commonly found in a high-frequency two stage configuration, being the first one an AC-DC conversion stage, usually with a power factor correction and the second one a DC-DC conversion stage which provides isolation and regulates the output current and voltage. This work proposes to study and design the DC-DC stage of a battery charger focused on industrial applications systems with Semiconductor Galvanic Isolation (SGI), aiming to acquire knowledge on this new technology which exempt the need for a transformer yet allowing galvanic isolation. Some topologies are proposed, and the selected one is then designed and analyzed along with simulation results. The compliance on product standard brings, among others, safety criteria, which guides an analysis of one such criterion about galvanic isolation, on which the maximum permissible touch current is established. A practical converter is then assembled allowing experimental results.

Keywords: Semiconductor Galvanic Isolation. Buck Converter. Battery Charger. Touch Current. DC-DC Converter.

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ACRONYMS

AC	Alternating Current. 19, 45, 46
CCM	Continuous Conduction Mode. 37, 38, 47, 49, 70, 72, 87
CM	Common-mode. 41, 42, 74
CRM	Critical Conduction Mode. 70
DC	Direct Current. 19, 21, 23, 24, 34, 41, 45, 52, 87
DCM	Discontinuous Conduction Mode. 70
DM	Differential-mode. 41, 42, 74, 75
ESR	Equivalent Series Resistance. 55, 57, 60, 63
PCB	Printed Circuit Board. 84, 94
PFC	Power Factor Correction. 19, 32, 45
PWM	Pulse Width Modulation. 25
SIG	Semiconductor Galvanic Isolation. 7, 8, 19, 28–30, 32–36, 41, 42, 45, 52, 53, 94
UPS	Uninterruptible Power Supply. 19, 21
ZVS	Zero Voltage Switching. 8, 24, 25

LIST OF SYMBOLS

C_1	Capacitor on the first stage <i>Buck</i> converter
$C_{1,min}$	Minimum capacitance for CCM at the first stage <i>Buck</i> converter
C_2	Capacitor on the second stage <i>Buck</i> converter
$C_{2,min}$	Minimum capacitance for CCM at the second stage <i>Buck</i> converter
C_{ds}	Switch's drain-source capacitance
C_{gd}	Switch's gate-drain capacitance
C_{gs}	Switch's gate-source capacitance
C_{iss}	Switch's input capacitance
C_{oss}	Switch's output capacitance
C_{rss}	Switch's reverse transfer capacitance
D_1	Duty cycle on the first stage <i>Buck</i> converter
D_{1B}	Bottom diode on the first stage <i>Buck</i> converter
D_{1F}	Freewheeling diode on the first stage <i>Buck</i> converter
D_{1T}	Top diode on the first stage <i>Buck</i> converter
$D_{1,max}$	Maximum duty cycle on the first stage <i>Buck</i> converter
$D_{1,min}$	Minimum duty cycle on the first stage <i>Buck</i> converter
$D_{1,nom}$	Nominal duty cycle on the first stage <i>Buck</i> converter
D_2	Duty cycle on the second stage <i>Buck</i> converter
D_{2B}	Bottom diode on the second stage <i>Buck</i> converter
D_{2F}	Freewheeling diode on the second stage <i>Buck</i> converter
D_{2T}	Top diode on the second stage <i>Buck</i> converter
$D_{2,max}$	Maximum duty cycle on the second stage <i>Buck</i> converter
$D_{2,min}$	Minimum duty cycle on the second stage <i>Buck</i> converter
$D_{2,nom}$	Nominal duty cycle on the second stage <i>Buck</i> converter
f_s	Switching frequency
$I_{D1,avg,max}$	Maximum average current on D_1
$I_{D1,Pk}$	Peak current on D_1
$I_{D1F,avg,max}$	Maximum average current on D_{1F}
$I_{D1F,Pk}$	Peak current on D_{1F}
$I_{D2,avg,max}$	Maximum average current on D_2

$I_{D2,Pk}$	Peak current on D_2
$I_{D2F,avg,max}$	Maximum average current on D_{2F}
$I_{D2F,Pk}$	Peak current on D_{2F}
$I_{L1,avg,max}$	Maximum average current on L_1
$I_{L1,Pk}$	Peak current on L_1
$I_{L2,avg,max}$	Maximum average current on L_2
$I_{L2,Pk}$	Peak current on L_2
I_o	Output current
$I_{o1,avg,max}$	Maximum average current on the output of the first stage <i>Buck</i> converter
$I_{S1,avg,max}$	Maximum average current on the switches S_{1T} and S_{1B}
$I_{S1,Pk}$	Peak current on the switches S_{1T} and S_{1B}
$I_{S2,avg,max}$	Maximum average current on the switches S_{2T} and S_{2B}
$I_{S2,Pk}$	Peak current on the switches S_{2T} and S_{2B}
L_1	Inductor on the first stage <i>Buck</i> converter
L_{1min}	Minimum inductance for CCM at the first stage <i>Buck</i> converter
L_2	Inductor on the second stage <i>Buck</i> converter
L_{2min}	Minimum inductance for CCM at the second stage <i>Buck</i> converter
P_o	Output power
$R_{L1,max}$	Maximum resistance for L_1 being in CCM
$R_{L2,max}$	Maximum resistance for L_2 being in CCM
S_{1B}	Bottom switch on the first stage <i>Buck</i> converter
S_{1T}	Top switch on the first stage <i>Buck</i> converter
S_{2B}	Bottom switch on the second stage <i>Buck</i> converter
S_{2T}	Top switch on the second stage <i>Buck</i> converter
V_{1B}	Voltage across the switch-diode pair S_{1B} and D_{1B}
V_{2B}	Voltage across the switch-diode pair S_{2B} and D_{2B}
V_{1T}	Voltage across the switch-diode pair S_{1T} and D_{1T}
V_{2T}	Voltage across the switch-diode pair S_{2T} and D_{2T}
V_{AC}	Voltage alternating current
$V_{C1,max}$	Maximum voltage at C_1
$V_{C2,max}$	Maximum voltage at C_2

$V_{D1F,max}$	Maximum voltage stress at D_{1F}
V_{DC}	Voltage direct current
$V_{g,max}$	Maximum universal AC input voltage
$V_{g,min}$	Minimum universal AC input voltage
V_{i1}	Nominal input voltage at the first stage <i>Buck</i> converter
$V_{i1,max}$	Maximum input voltage at the first stage <i>Buck</i> converter
$V_{i1,min}$	Minimum input voltage at the first stage <i>Buck</i> converter
V_{L1}	Voltage across L_1
V_{L2}	Voltage across L_2
V_o	Output voltage
$V_{o,max}$	Maximum output voltage
$V_{o,min}$	Minimum output voltage
$V_{o1,min}$	Minimum output voltage at the first stage <i>Buck</i> converter
$V_{o1,nom}$	Nomonal output voltage at the first stage <i>Buck</i> converter
$V_{S1,max}$	Maximum voltage stress at S_{1T} and S_{1B}
$V_{S2,max}$	Maximum voltage stress at S_{2T} and S_{2B}
α_{D1D2}	Rating between D_1 and D_2
ΔI_{L1}	Peak-to-peak ripple current on L_1
ΔI_{L2}	Peak-to-peak ripple current on L_2
ΔV_o	Output voltage ripple at the second stage <i>Buck</i> converter
ΔV_{o1}	Output voltage ripple at the first stage <i>Buck</i> converter
η_1	First stage <i>Buck</i> converter efficiency
η_2	Second stage <i>Buck</i> converter efficiency

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1 INTRODUCTION

Battery chargers are in an extensive variety of applications ranging from smaller ones used to charge the lithium battery of mobile phones to larger ones used to quickly charge an electrical vehicle. The focus for this work is on industrial application systems, more often composed of a bank of lead-acid or alkaline batteries, and used as an Uninterruptible Power Supply (UPS) system for Direct Current (DC) loads. For this application there is emphasis on two options: the robust thyristor-based rectifier and the switched mode high-frequency rectifier.

Thyristor-based AC-DC converters are still commonly used and preferred in several industrial branches, power generation and substations to charge batteries and to maintain DC Power Systems. They have simple and well established circuitry which gives them the robustness needed to be operating for a long period, even in severe conditions. A 50/60 Hz transformer is used for isolation and adaptation of the voltage range, but the low operating frequency results in very large volume. The pulsed current at the input of the controlled rectifier bridge produces high levels of current harmonics resulting in very poor power factor, usually with the need for compensation. The increase in installed power requires a redesign of the magnetic elements, which is often not feasible in already-assembled systems due to the limited available footprint.

On the remaining segments, where there is no need for the thyristor-based rectifier benefit, one widely applied option is the switched mode high frequency rectifier, which brings volume reduction through frequency increase and current harmonics reduction with a Power Factor Correction (PFC) converter. There is also a possibility for them to be allocated in modular system to facilitate maintenance and system expansion.

On both options there is normally a need for isolation between the input and the output of the converter, conferring safety for the user and for the loads. Another needed feature is the voltage and current regulation at the output, where the battery is connected, so the charging could be done according to procedures that avoid degradation on the battery lifespan. On switched mode high frequency rectifier these two features are commonly met on a DC-DC stage of a two stage converter, being the first stage responsible for the Alternating Current (AC) to DC conversion.

Having in mind an industrial application for charging batteries and supplying uninterruptible power to DC loads, this work proposes to build an isolated DC-DC converter, second stage of a battery charger, with the Semiconductor Galvanic Isolation (SGI), which provides galvanic isolation without using a transformer. This proposal aims to acquire knowledge about this new technology and prospect its advantages and disadvantages.

The primary objective is to introduce a novel topology of DC-DC converter incorporating SGI technology and to investigate its operation, suitability as a second stage in a battery charger, and compliance with product standards. It aims to contribute with a new perspective of the technology.

Specific project objectives include:

- Demonstrating and analyzing the operation of the converter to ensure compliance with specified requirements, such as galvanic isolation, with a particular emphasis on evaluating touch current.
- Designing the converter based on typical application conditions.
- Conducting simulations to illustrate the operation of the converter and to validate the adequacy of the component design.

Finally, manufacturing the converter aims to experimentally verify and validate the theoretical proposals and designs.

A 2kW converter for charging a 48V battery bank is commonly found in commercial modular battery chargers, and is selected as the intended application for this work as for acquiring knowledge about the SGI technology.

This thesis is structured as follows: In Chapter 2 a literature review is made on the converter topology that could be suitable for the application; Chapter 3 runs through the topology options and describes the selected and proposed topology; Chapter 4 shows the proposed topology operation steps; On the Chapter 5, all necessary considerations are made for designing the converter; Chapter 6 displays the simulations made and their results are commented; On the Chapter 7 the experimental results are addressed with a mounted practical converter; Chapter 8 concludes this thesis and suggests future work.

2 LITERATURE REVIEW

On this chapter, the literature is reviewed on the relevant aspects of this thesis regarding the converters used for battery charging and sourcing DC power.

Most commonly, battery chargers and DC UPS use a two-stage converter, as reviewed in (INAMDAR; THOSAR; MANTE, 2019). The first stage handles the input power factor correction while the second regulates the output voltage level providing isolation.

The full converter is powered by the AC grid in its first conversion stage. However, since the focus of this work is on the second stage, the DC-DC topologies are reviewed.

On the next section DC to DC converters which are applicable to battery charging are reviewed, followed by a comparison on the cited topologies and their variations.

2.1 DC-DC TOPOLOGIES

This section brings a review on the literature about the second conversion step, namely DC-DC stage, the focus of this work, checking the proposed topologies and verifying their advantages and disadvantages among each other, describing its characteristics regarding the efficiency, constructive factors of the circuits and aspects that influence their functionality. Basic topologies are analyzed, and the literature is surveyed on converters based on those topologies bringing improvements on the characteristics aforementioned.

2.1.1 Flyback based

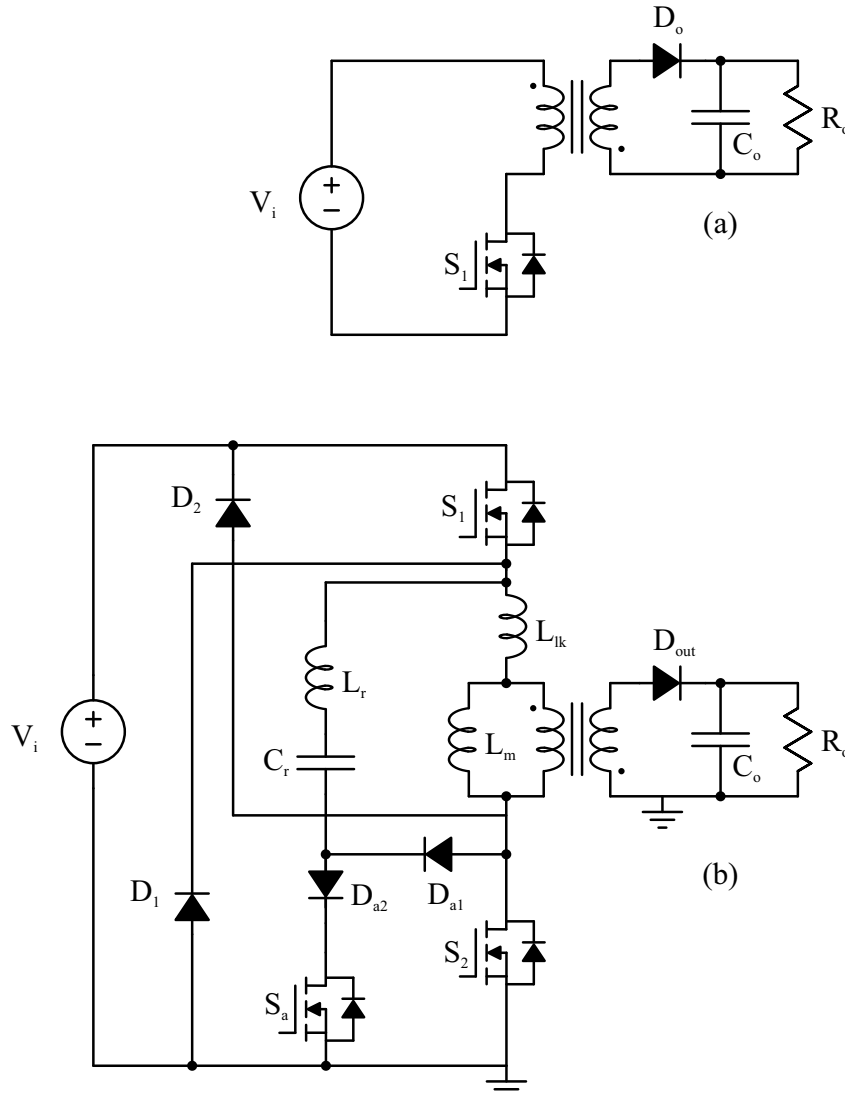
Flyback converter is broadly used in the daily context of house and commercial environment electronics, usually from 20 to 200 W as put in (KAZIMIERCZUK, 2008). The low part count, as can be seen in Figure 1 (a), makes it convenient for low power applications. It is based on the buck-boost converter by adding a isolation transformer, which also allows a wide voltage gain between the input and output.

The Flyback transformer can also be considered a magnetically coupled inductor, as in addition to transferring energy from the primary to the secondary, it works as an energy storage component, exempting the use of another inductor. In addition, the transformer can contain more than one secondary winding, making possible to have more than one output with equal or different potentials, even negative potentials, and all outputs will also be isolated from each other.

During the Flyback operation, when the switch turns off, the energy stored in the leakage inductance will discharge on the switch output capacitance, producing a high voltage stress. A Flyback based converter, using two switches, presented in the Figure 1 (b) by (YAZDANI; RAHMANI, 2014), solves this problem by returning the leakage inductance energy to the input source. In this proposed converter, all the switching element make their transitions on a zero-current condition and the auxiliary switch (S_a) does not need an isolated gate driver. The

two-switch Flyback topology by itself, limits the voltage stress on both main switch to the input voltage.

Figure 1 – Flyback based converters: (a) Flyback converter basic topology. (b) ZCT two-switch flyback converter by (YAZDANI; RAHMANI, 2014).

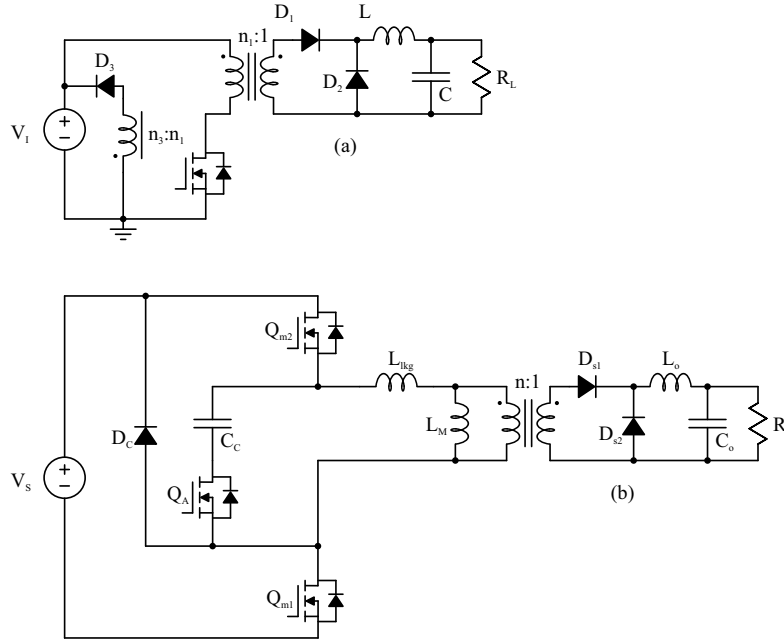


Source: (a) Made by the author (2023), adapted from (KAZIMIERCZUK, 2008). (b) Made by the author (2023), adapted from (YAZDANI; RAHMANI, 2014).

2.1.2 Forward based

The Forward converter, shown in Figure 2 (a), is also widely used for low and medium power applications on single output or multiple-output power supplies, usually from 30 to 500 W (KAZIMIERCZUK, 2008). In this case the transformer is not required to store magnetic energy, but it includes a tertiary winding in series with a diode to reset the core, commonly with the same number of turns as the primary, and in this condition, the voltage across the switch is twice the line voltage, thus, the switch must withstand high voltage stress. The output inductor usually requires an air gap in its core and may get a high volume.

Figure 2 – Forward based converters: (a) Forward converter basic topology. (b) Two-switch active-clamp Forward converter proposed by (PARK; MOON; YOUN, 2011).



Source: (a) Made by the author (2023), adapted from (KAZIMIERCZUK, 2008). (b) Made by the author (2023), adapted from (PARK; MOON; YOUN, 2011).

A two-switch Forward based converter is proposed by (PARK; MOON; YOUN, 2011), on this topology, depicted in Figure 2 (b), the voltage stresses on two main switches are limited to input voltage by a clamp diode. On the paper, the author also proposes a solution to eliminate the duty cycle limitation of 0.5 from the basic Forward required for the transformer reset.

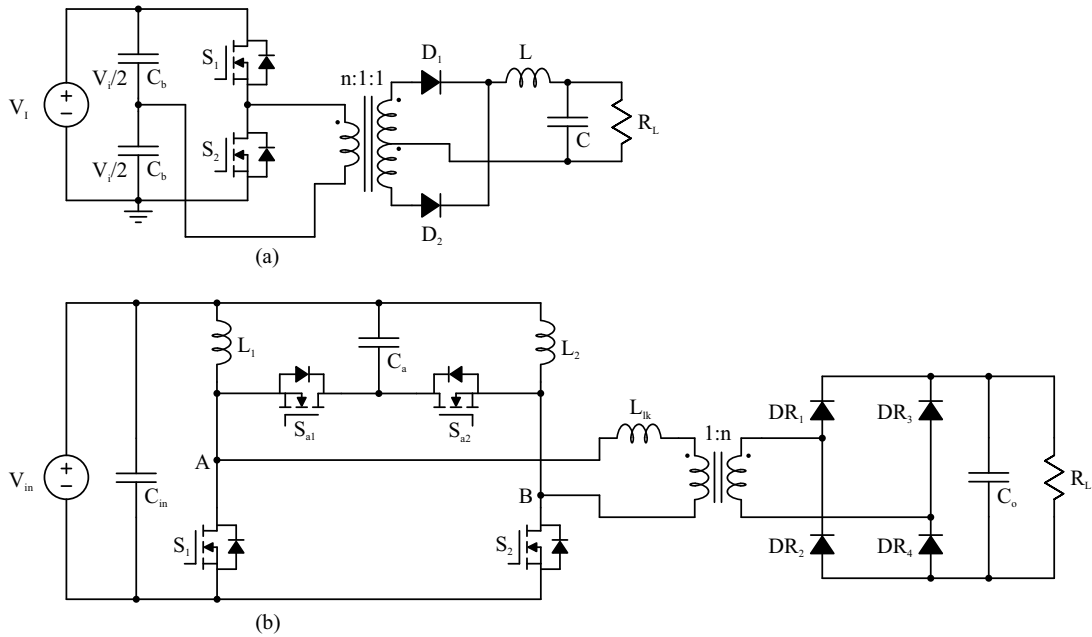
The double switch forward without active clamping is also widely used up to 2-3 kW converters for computer power supplies with an advantage of not suffering from shoot through in case of unwanted gate drive glitches.

2.1.3 Half-bridge based

Normally, the Half-bridge converter, as on the Figure 3, is used from medium to high power applications ranging from 150 W to 1 kW and is widely used in telecommunication power supplies (KAZIMIERCZUK, 2008). The voltage stresses on the main switches are reduced if compared to Forward basic topology and is equal to the maximum DC input voltage. Another advantage is that the core saturation problems are minimized because the DC component of the current through the primary is zero due to the coupling or blocking capacitors in series with the primary, since the primary is driven in both directions, the core is utilized more effectively. The core is half the size of equivalent transformers in single-transistor converters.

The disadvantages are the requirement of an additional power transistor and an isolated driver for the upper transistor. The maximum duty cycle is slightly less than 0.5 to avoid the situation, when both transistors are conducting at the same time.

Figure 3 – Half-bridge based converters: (a) Half-bridge DC-DC converter basic topology. (b) Active-clamped ZVS current-fed half-bridge DC-DC converter by (RATHORE; LI, 2011).



Source: (a) Made by the author (2023), adapted from (KAZIMIERCZUK, 2008). (b) Made by the author (2023), adapted from (RATHORE; LI, 2011).

A current-fed half-bridge DC-DC is presented in (RATHORE; LI, 2011), in this converter, normally there are a drawback of large voltage turn-off spike across the switches, so, an efficient active-clamp based solution was proposed to clamp the voltage across the switches at turn-off, allowing the selection and use of low voltage devices with low on-state resistance. The active-clamp also results in zero-voltage transition circuit aiding in achieving zero voltage switching of the devices improving the efficiency and allowing high switching frequency operation.

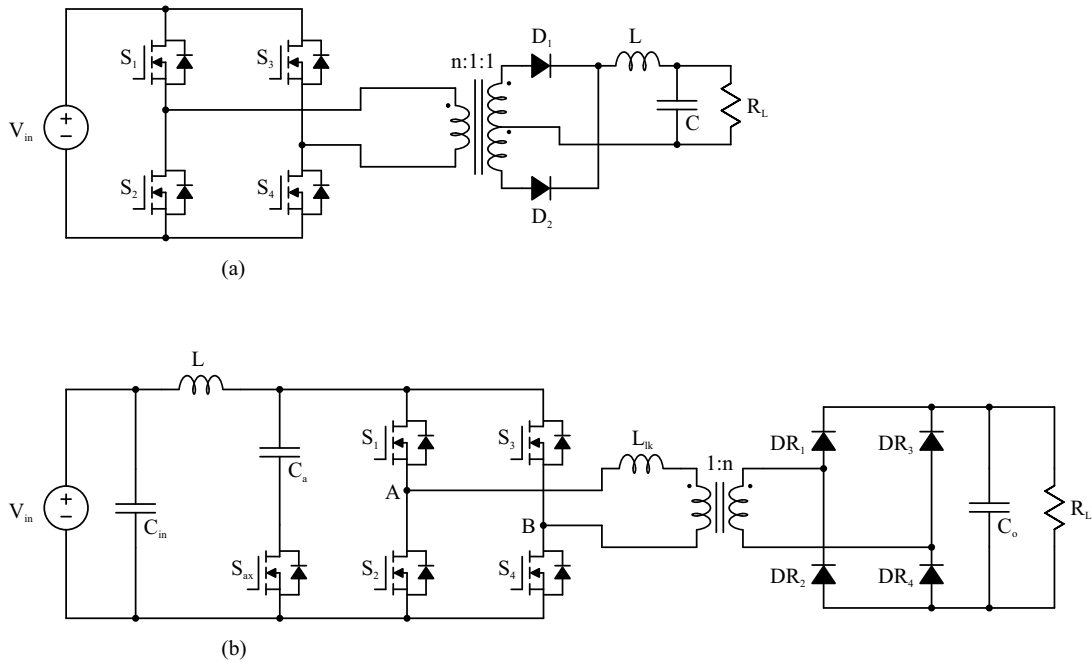
A drawback on this converter, for the battery charging application, is its output being a voltage source without a current smoothing mechanism, thus, current peak can be transferred to the battery and reduce its lifespan.

2.1.4 Full-bridge based

The Full-bridge DC-DC converter, with its basic structure presented on the Figure 4, offers the highest power levels of the reviewed transformer-isolated topologies, usually applied from 500 W to 5 kW (KAZIMIERCZUK, 2008). It draws two current pulses per switching cycle and is capable of delivering more output power if compared with the half-bridge converter. The voltage stresses of the switches are low and equal to the DC input voltage. The core is excited in both directions and is relatively small.

A current-fed full-bridge DC-DC converter is presented in (RATHORE; LI, 2011), with one additional active switch to permit ZVS operation and reduce turn-off voltage spike across the main switches, thus, improving performance. Although it carries the same drawback as on

Figure 4 – Full-bridge based converters: (a) Full-bridge DC-DC converter basic topology. (b) Active-clamped ZVS current-fed full-bridge DC-DC converter by (RATHORE; LI, 2011).



Source: (a) Made by the author (2023), adapted from (KAZIMIERCZUK, 2008). (b) Made by the author (2023), adapted from (RATHORE; LI, 2011).

the half-bridge option on the output not being current-driven.

2.1.5 Resonant converters

Resonant converters are differentiated by the addition of a resonant circuit, or resonant tank on the main topology circuit. They take advantage of the parasitic elements of the converter components, using them to perform soft switching, which can contribute to achieving high efficiency and possibly reducing electromagnetic interference problems.

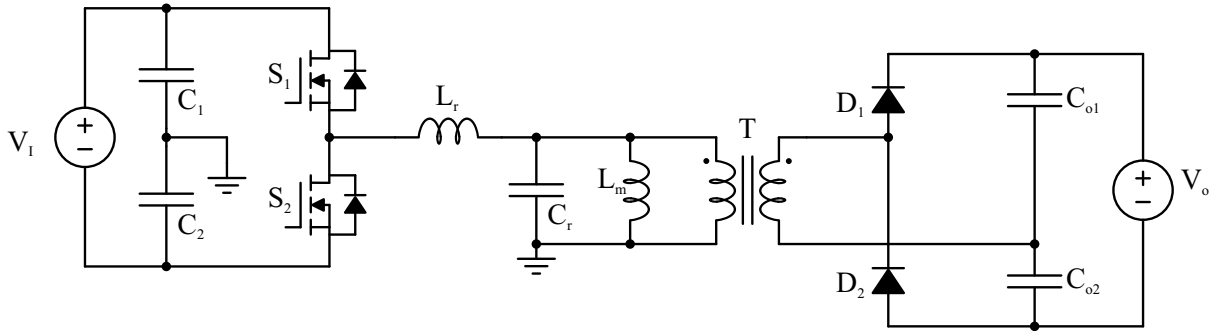
A half-bridge resonant converter is developed in (PONT et al., 2018) allowing an efficiency of 97.2%. The circuit, shown in the Figure 5, has a parallel resonant tank and uses Pulse Width Modulation (PWM).

Besides the benefit of this converter, the voltage-driven output is not a good option for letting current peaks to the battery.

2.1.6 Switched-capacitor converters

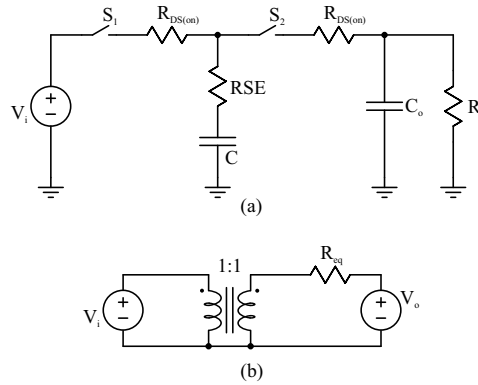
Long ago the switched-capacitor technique was used in signal processing, however, recently it became considered for power processing with the main benefits of not needing magnetic elements, reduced EMI levels and ease of manufacturing, although they usually have a large number of components, considerable power losses that depends on the converter parameters to be reduced and they are unaffected by the duty cycle, with means that they not controllable.

Figure 5 – Half-bridge parallel resonant convert by (PONT et al., 2018).



Source: Made by the author (2023), adapted from (PONT et al., 2018).

Figure 6 – Switched-capacitor converters: (a) Switched-capacitor basic cell shown in (MARTINS, 2013). (b) Equivalent circuit for the switched-capacitor basic cell.



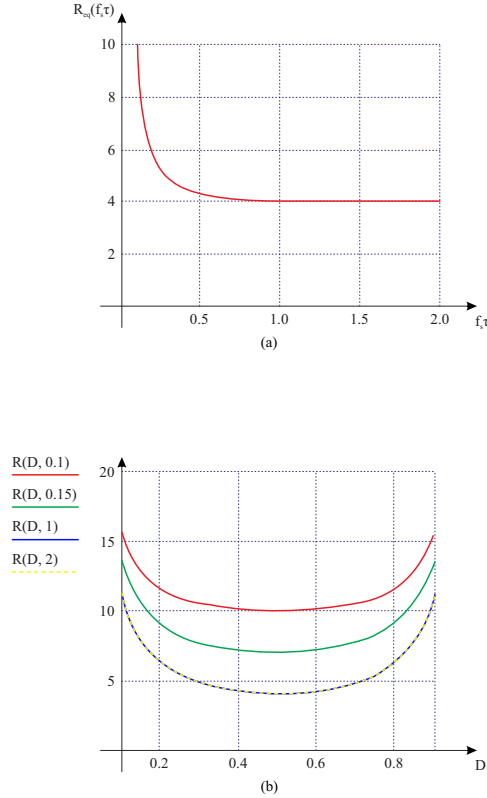
Source: Made by the author (2023), adapted from (MARTINS, 2013).

The basic cell is shown at Figure 6 (a), and it's equivalent circuit is represented by Figure 6 (b), have a resistive characteristic for the converter that varies with frequency and duty cycle, as can be observed at the Figure 7 and verified on the Equation 1. These factors must be observed in the design of the converter to reduce losses, improving its efficiency. The equivalent resistance is given by the Equation 1, exposed in (BARBI, 2019), with that, the charts on the Figure 7 can be drawn and show that the frequency must be high enough and the duty cycle 0.5 to match the lowest equivalent resistance, $R_{eq.min} = 4 \cdot R_{DSon}$.

$$R_{eq} = \frac{R_{DSon}}{f_s \tau} \frac{1 - e^{-\frac{1}{f_s \tau}}}{\left(e^{-\frac{D}{f_s \tau}} - 1\right) \left(e^{-\frac{(1-D)}{f_s \tau}} - 1\right)} \quad (1)$$

Even though this converter is not controllable, there are topologies based on the switched-capacitor technique that can reduce or increase the voltage level with a fixed gain. One example is the topology on the Figure 8, where each of the capacitors C_1 , C_2 , C_3 and C_4 are charged in series when S_1 is closed, so each one will have $1/4$ of the input voltage. Then, S_1 is opened and S_2 closed, and the capacitors will be in parallel with the load, which will have a quarter of input

Figure 7 – Equivalent resistance, relative to R_{DSon} , curves on the switched-capacitor based on Equation 1 by (BARBI, 2019). (a) Equivalent resistance according to the switching frequency multiplied by the time constant, for $D = 0.5$. (b) Equivalent resistance as a function of duty cycle, for different values of $f_s \tau$.



Source: Made by the author (2023), adapted from (BARBI, 2019).

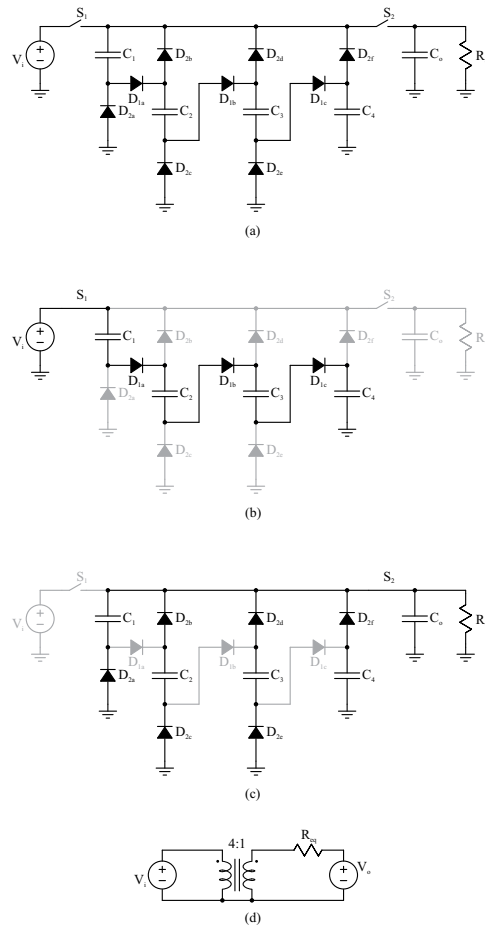
voltage aswell. This operation is depicted, respectively, on the Figure 8 (b) and (c), and Figure 8 (c) shows the equivalent circuit of this converter.

2.1.7 Semiconductor-Based Galvanic Isolation

Various applications, including the one addressed here, require galvanic isolation to comply with safety standards, to provide high impedance and block common-mode leakage current. Aiming to eliminate magnetic components providing a simple structure, improved manufacturability, smaller size (improved power density), easy to control and with high efficiency, a solution with a novel switched-capacitor based cell is developed by (ZHANG et al., 2018). The isolating switched-capacitor cell is demonstrated at Figure 9 (a), where the operation is similar of the switched-capacitor technique, but a switch on the negative current path S_2 uncouples the capacitor C_{mid} from the input power source V_{in} . The same occurs between C_{mid} and the load by the switches S_3 and S_4 , so, at any moment there is no connection between input power source and the load, granting galvanic isolation.

Nonetheless there is still a common-mode current that can circulate by the switch output capacitance that requires an additional compensation circuit to allow the compliance with safety

Figure 8 – Switched-capacitor step-down converters: (a) Step-down switched-capacitor converter $G = 1/4$ by (MARTINS, 2013). (b) First operation step. (c) Second operation step. (d) Equivalent circuit.

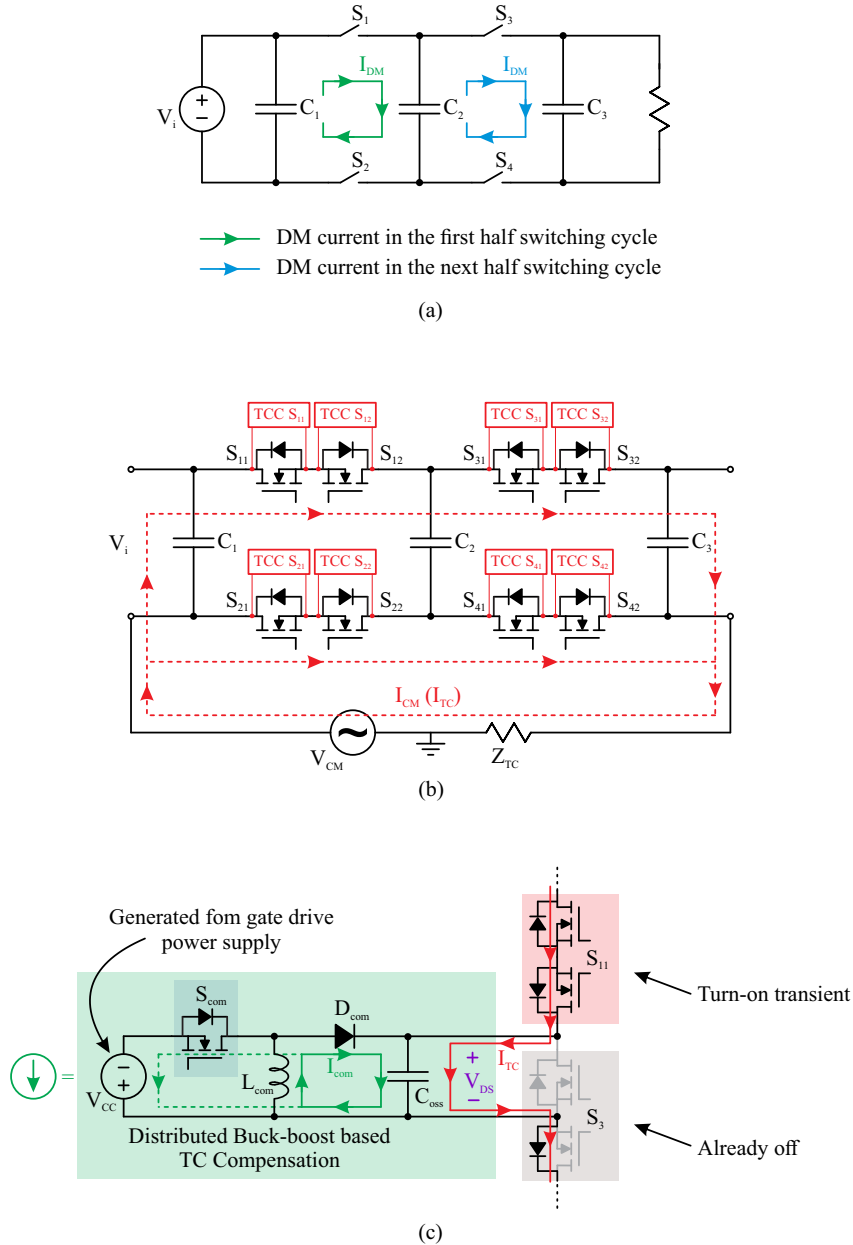


Source: Made by the author (2023), adapted from (MARTINS, 2013).

standards. An option is proposed at (YAO et al., 2020) with a Buck-boost circuit used to supply current for the switch output capacitance avoiding touch current circulation from charging it. The Figure 9 (b) presents the switched-capacitor SGI cell with discrete switches and $TCC S_{xx}$ represents the touch current compensation circuit attached to each main switch. The Figure 9 (c) shows the implementation of the compensation circuit with a Buck-boost converter.

Together, the touch current compensation circuit switches and the anti-series main switches count up to 16 components, but half of them, used on the compensation circuit are smaller ones, specified for reduced voltage and current. In general, the Buck-boost circuit have reduced power capacity compared to the main circuit.

Figure 9 – Semiconductor-Based Galvanic Isolation: (a) SGI-based switched capacitor 1:1 cell by (YAO et al., 2020). (b) SGI converter cell with distributed touch current compensation circuits proposed by (YAO et al., 2020). (c) Buck–boost circuit for TC compensation at turn-ON transients proposed by (YAO et al., 2020).



Source: Made by the author (2023), adapted from (YAO et al., 2020).

2.2 TOPOLOGY COMPARISON

A survey was made on the literature for DC-DC converters based on the topologies exposed in this section, with the objective of comparing them quantitatively, qualitatively and about the adherence with the application. The Table 2 summarizes the output power, efficiency, switching frequency and component count of each project.

Although the Flyback converter is recommended for low power applications, with a

modified circuit, as a two-switch Flyback, was possible to reach up to 1 kW output power in the literature, but the 2 kW established as an objective here was not found. The efficiency under the expected value also discards the selection of this topology for the application.

As well as on the Flyback converter, on the Forward converter, the current flows only in one way at the transformer, underutilizing B–H curve of the magnetic core and making it twice the size if compared to a topology where the current flows both ways. Both converters require an air gap on their inductors. For the similar reasons, as the Flyback, the Forward converter is discarded for the application. Another drawback of the modified converters, comparing with the base topology, is that they add complexity and more components to the system. Flyback and Forward converter both have only one active switch on their base topology, but, as can be seen in Table 2, the modified topology uses from 2 to 4 active switches, and the diode count also increases.

On the Half-bridge and Full-bridge converters, the current flow in both directions on the transformer, acting like a Push-pull technique, it puts the transformer in better use, thus, it can be reduced for the same power levels. The Full-bridge, however, have a smaller transformer due to using the full input voltage applied on both transformer sides. A resonant tank also can be added to improve the converter's efficiency and allowing soft switching. A practical example of this improvement can be seen in (PONT et al., 2018). There, a Half-bridge has a parallel resonant tank added and achieved 97.2% of efficiency. The voltage stress is also lower on these two converters if compared with Flyback and Forward.

As for the switched-capacitor and its variation with semiconductor-based galvanic isolation, high efficiency as Half-bridge and Full-bridge can be achieved, with practical examples summarized in Table 2 and shown in (MARTINS, 2013) and (ZHANG et al., 2018). Although some measures must be observed for it, as a high switching frequency and the use of 0.25 duty cycle. As the isolation is a goal here, only the circuit with SGI is applicable, and precautions must be taken care of to achieve safety standards, in special, the touch current under standardized limit. An efficient solution for it is presented on the literature by (YAO et al., 2020), but it brings the drawback of doubling the switch count. Nevertheless, the additional switches do not require additional sources for their driving circuits, as they can share the main ones. The lack of control on the output voltage could impose a problem for the battery charging, as it needs to have controlled current and voltage.

Table 2 – Comparison of projects found in the literature with surveyed DC-DC topologies

Base topology	Reference	P [W]	η [%]	f_s [kHz]	Active switch	Diode	Magnetics
Two-switch Flyback	(LIMA, 2020)	1000	90	30	4	12	2
Two-switch Flyback	(HOFSTAETTER, 2016)	200	73.8	62.5	2	3	1
Two-switch Flyback	(SOUZA, 2018)	85	87.5	100	2	3	1
Two-switch Flyback	(YAZDANI; RAHMANI, 2014)	60	87	100	3	5	2
Two-switch Forward	(TREVISI et al., 1998)	1500	90	77	2	6	3
Two-switch Forward	(ZHAO; DALI, 2007)	330	-	100	2	4	2
Two-switch Forward	(TOFOLI; GALLO; SILVA, 2006)	300	-	100	3	5	2
Two-switch Forward	(PARK; MOON; YOUN, 2011)	300	94.2	100	3	4	2
Resonant (Full-bridge)	(LIN; LIN, 2010)	576	94	100	4	2	2
Resonant (Half-bridge)	(PONT et al., 2018)	1000	97.2	50	2	2	2
Push-pull	(YUAN; CHANG; SONG, 2007)	1000	92	30	2	4	2
Push-pull	(MAO; WANG; YAN, 2005)	2000	95.8	100	4	4	2
Half-bridge	(RATHORE; PRASANNA, 2011)	500	95	100	2	4	3
Half-bridge	(GUILLAUME et al., 2006)	2000	95.8	50	2	4	4
Half-bridge	(RATHORE; LI, 2011)	1000	94.5	100	4	4	3
Full-bridge	(RATHORE; LI, 2011)	1000	94.2	100	5	4	2
Full-bridge	(BOTTION; BARBI, 2015)	4000	95	40	4	4	1
Full-bridge	(IKEDA; KUROKAWA, 2017)	10000	95	17.5	6	5	2
Switched-capacitor	(MARTINS, 2013)	120	95	50	2	9	0
Switched-capacitor (SGI)	(ZHANG et al., 2018)	2000	98	120	16	0	0

Source: Made by the author (2023).

2.3 GALVANIC ISOLATION

Galvanic isolation allows two or more circuits to operate without unwanted current flowing between them, or reduces this current to an acceptable level. This kind of current, between circuits, can cause malfunctioning, damage or even harm to a person operating it, which is the case of touch current.

One way to provide galvanic isolation to a circuit is by using an optical medium, employing an emitter such as a Light Emitting Diode (LED) and a receiver photodiode to transmit the information while the circuits have no current flow between them. This method is used to transmit signals from one circuit to another, as shown in (ISHIGAKI et al., 2017), where it is not used directly for the power converting circuit but for the auxiliary ones.

Another option is to use capacitive isolation, where a capacitor is placed between the two isolated circuits. The signal or power is transmitted by the capacitor's electrical field. This method has been applied for long ago in signal isolation, but recently its application in power transmitting is also being explored, as an example of (ZHU et al., 2010).

The most applied method in the power electronics is the magnetic galvanic isolation, which employs a transformer or a coupled inductor between circuits. This method is widespread and accepted in the literature for most of the isolated converters.

The SGI technology has not received enough discussion to be compared to traditional methods when it comes to standard compliance.

3 PROPOSED TOPOLOGY

From the topology review, some topologies have been shown to be suitable for the application, among them are the Half-Bridge and Full-Bridge based topologies, which brings a variety of benefits for the battery charger. In the literature, knowledge is available on various aspects of these converters, presenting a diversified range of topology variations, with each one bringing its own improvements.

For the SGI based topologies there is a narrow range of information, with few works exploring it for power processing. It is shown as an opportunity for new research on this recent technology that can give good results, given some aspects of the converter and its manufacturing.

This work proposes a new topology using SGI and aims to acquire knowledge about this new technology and prospect its advantages and disadvantages. Independent of the input of the full battery charger converter, the second stage, DC-DC converter is proposed.

The battery charging application sets some characteristics for the converter to be planned, as the input voltage. On this aspect, the DC-DC converter has its power usually supplied by a rectifier with PFC, which itself is powered by the main AC power line. As the input rectifier commonly has a *Boost* converter to perform PFC, its output will have a voltage level higher than the input peak value. Considering it as the input voltage for the DC-DC converter to be proposed, and set that it will charge 4 series connected 12 V batteries, it is defined that the converter will have its output voltage lower than its input voltage, thus a *Buck* converter.

It is known that the basic SGI cell, presented by (YAO, 2018), does not have the voltage control feature on its output, so it could not be used alone for this application. A third converter stage would be used for voltage regulation in that case, it would not need isolation since the SGI basic cell includes this feature. However, increasing one conversion stage is undesirable for complexity and efficiency matters. Keeping two conversion stages usually improve those characteristics.

Another viable option is to add the SGI feature to traditionally non-isolated converter to attain both voltage regulation control and galvanic isolation. It is made on the next section in the seek for a topology that comply with the battery charger requirements.

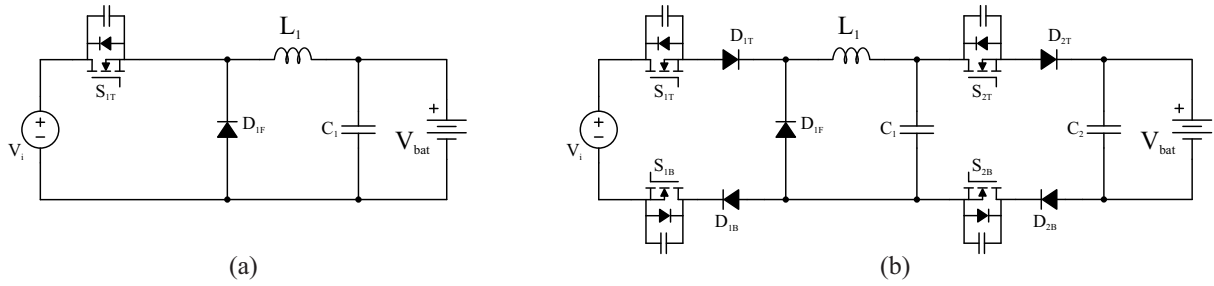
3.1 TOPOLOGY CANDIDATES

As the selected topology needs step-down voltage on the converter output, some base topology which includes this feature would be a nice way for starting, as the *Buck* and *Buck-Boost* converter. Then, the other aspect of the application needs to be considered followed by a benefit analysis of each option.

3.1.1 Classical *Buck* converter with SGI

The first option is to add the SGI feature to a classical *Buck* DC-DC converter with LC filter, as shown in Figure 10, composing a topology presented in (YAO, 2018). On this topology the output capacitor is split into two where the basic SGI cell is put.

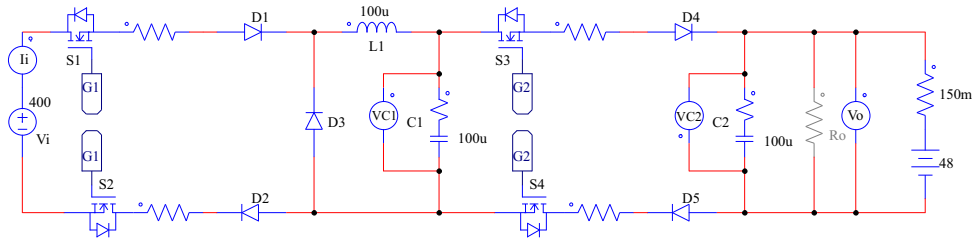
Figure 10 – Topology option: (a) DC-DC *Buck* converter basic topology. (b) DC-DC *Buck* converter with SGI.



Source: Made by the author (2023).

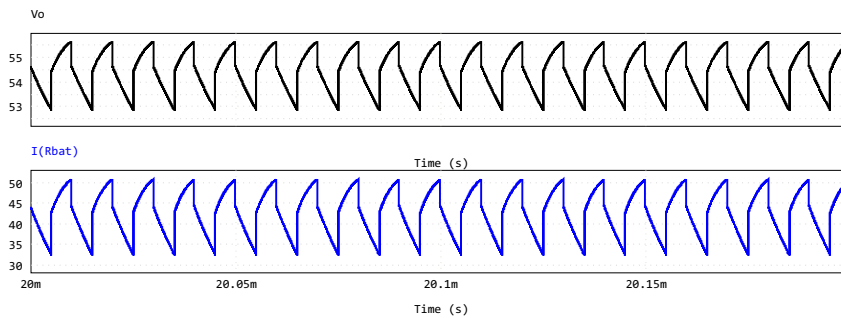
This option solves the problem of not having output voltage control and it can be regulated at the goal value. But the drawback is the high current ripple on the battery, as the result shown in Figure 12 simulated with the circuit on Figure 11, caused by having only a parallel capacitor on the converter output. Even though a battery can be charged with it, the ripple would cause a reduction on the battery lifespan.

Figure 11 – Simulation circuit for the DC-DC *Buck* converter with SGI.



Source: Made by the author (2023) on PSIM.

Figure 12 – Simulation results for the DC-DC *Buck* converter with SGI.

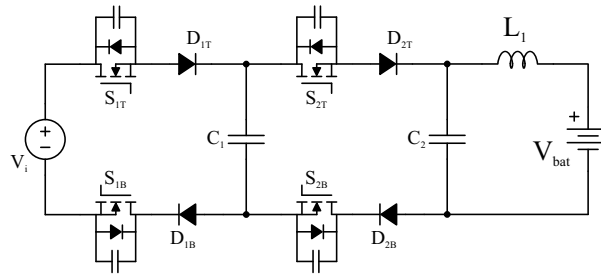


Source: Made by the author (2023) on PSIM.

3.1.2 Using the Inductor at the Output

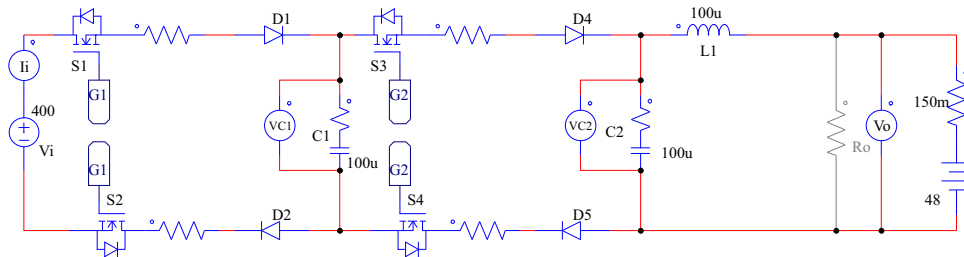
To solve the current ripple to the battery, an inductor could be placed on the output, as shown in the Figure 13, but the problem of voltage controlling would not be completely solved, as the inductor now is not at the switching elements path, but after them, acting substantially as a filter after a basic SGI cell. So, the voltage could be controlled but it will have dependence on the load.

Figure 13 – DC-DC converter with SGI basic cell and Inductor at the output.



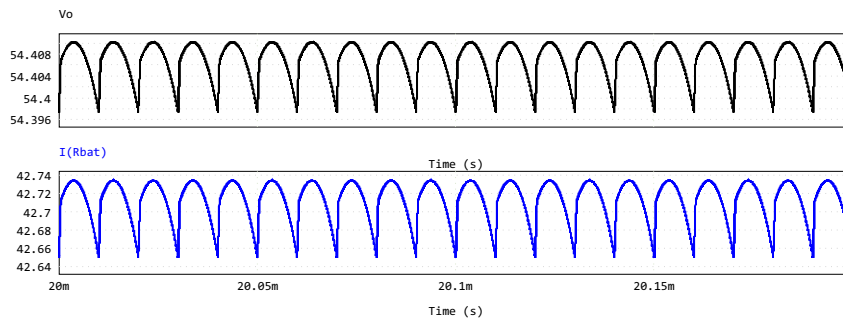
Source: Made by the author (2023).

Figure 14 – Simulation circuit for DC-DC converter with SGI basic cell and Inductor at the output.



Source: Made by the author (2023) on PSIM.

Figure 15 – Simulation results for the DC-DC converter with SGI basic cell and Inductor at the output.

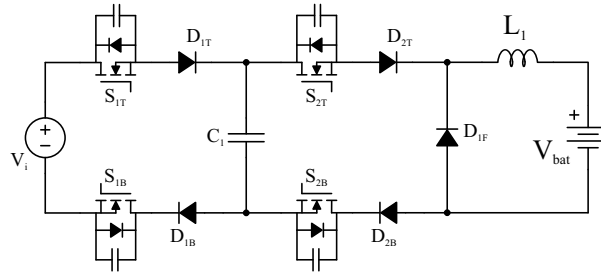


Source: Made by the author (2023) on PSIM.

Replacing the output capacitor by a diode, as in Figure 16, would put the output inductor at the switches path, but directly connected to the battery to be charged, so the voltage ripple

would depend on the battery. If the converter is to be used as a DC power supply for a resistive load, the voltage ripple would get high values, as the voltage on the inductor may vary abruptly and there is no voltage smoothing mechanism. The simulation for this topology is done by the circuit in Figure 17 and the results shown at Figure 18.

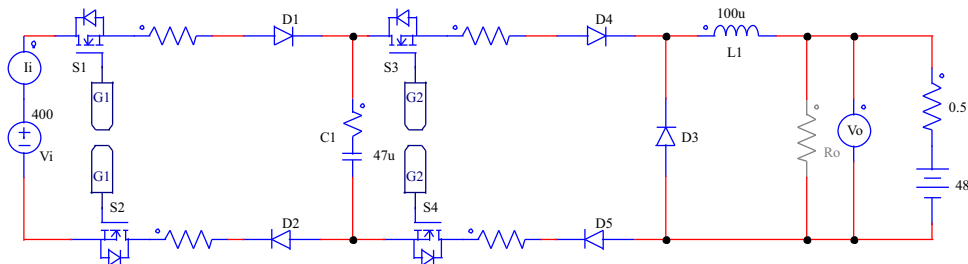
Figure 16 – DC-DC converter with SGI, Inductor at the output and freewheeling diode.



Source: Made by the author (2023).

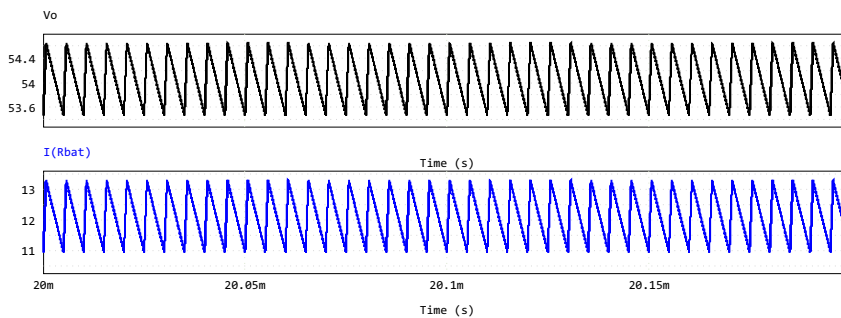
This converter can also be viewed as a SGI switched capacitor followed by a *Buck* converter with a inductive output filter.

Figure 17 – Simulation circuit for the DC-DC converter with SGI, Inductor at the output and freewheeling diode.



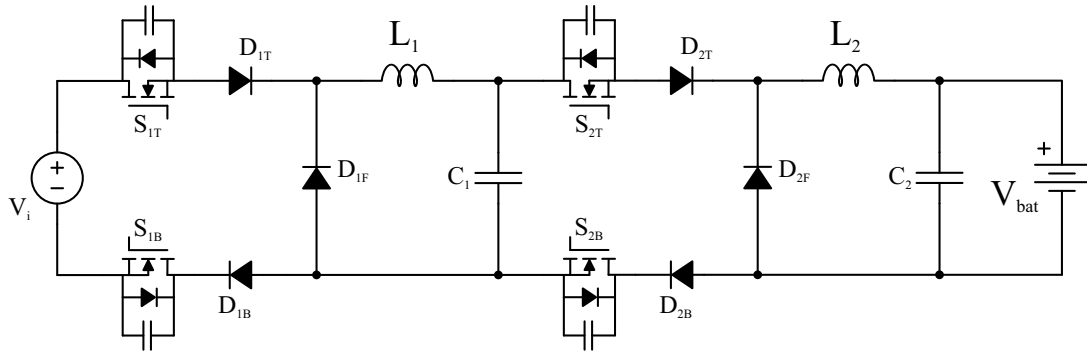
Source: Made by the author (2023) on PSIM.

Figure 18 – Simulation results for the DC-DC converter with SGI, Inductor at the output and freewheeling diode.



Source: Made by the author (2023) on PSIM.

Figure 19 – Proposed converter topology.



Source: Made by the author (2023).

3.2 SELECTED TOPOLOGY

The selected topology for this project took into consideration aspects in which some aforementioned topology options did not reach and the capacity to provide conditions on understanding the SGI technology. The DC-DC *Buck* converter base is still a good option for the reasons cited before, and the selected topology uses it.

Two cascaded DC-DC *Buck* converter with included SGI feature, as in Figure 19, is selected as the topology for the project. This topology provides a good controllability for the output voltage as well as the output current with two duty cycles, one on each pair of switches, S_{1T} , S_{1B} and S_{2T} , S_{2B} . The duty cycle has to be limited below 0.5 for the galvanic isolation to take place. In fact, the switches S_{1T} and S_{1B} can not conduct at the same time as S_{2T} and S_{2B} for it to happen. The current ripple to the battery can also be as low as needed by selecting a proper LC filter.

Another advantage on this topology is the high step-down gain, as it is composed by two cascaded DC-DC *Buck* converter, the gain for the whole converter is the multiplication of two single DC-DC *Buck* converter. This aspect is very important to various applications, battery charging included. If a single DC-DC *Buck* converter is to reach such gain, specially at high power rates, as 2kW, it could lead to elevated current peaks on the input supplying source.

As the topology is made by 2 cascaded *Buck* converter, they can be considered as two single converter for analyzing, which facilitates as the literature is plenty on a variety of subject on the converter. More detailed feature on the proposed topology are presented and exploited next on the Operation Steps and the Design chapter.

Different from a regular DC-DC *Buck* converter, on this topology the switch is replaced by a switch-diode set, as S_{1T} with the diode D_{1T} . This is done so the current flows only in one direction and can be blocked by the switch. This feature allows the converter to comply with the IEC 60950-1 standard test of electric strength. If there was only a switch, without the diode, a voltage applied for the test, going from the output to the input, would make a current circulate through the switch's internal diode, and cause a short circuit disapproving the test.

4 CONVERTER OPERATION

This chapter elucidates the converter functioning process based on the proposed topology showing the operation steps for it and then, show how the touch current flows through the converter.

4.1 OPERATION STEPS

On the proposed converter, the switches S_{1T} and S_{2T} operate as the main switches of two regular DC-DC *Buck* converter and S_{1B} , S_{2B} are added on the negative rail for granting galvanic isolation. The converter operates with 4 steps and each *Buck* stage will be conducting on one.

The operating conditions for this analysis includes the constant input voltage V_i and the voltage on both capacitors, C_1 and C_2 , although the voltage on C_1 does have a ripple due to the pulsed current drained by the second stage *Buck* converter, and C_2 a small 1% ripple. These ripple are presented by the dashed lines on the Figure 21. Also, both converter steps are operating at Continuous Conduction Mode (CCM) and no common-mode current is considered on this analysis, as presented on the next section it would change the voltage distribution on the components.

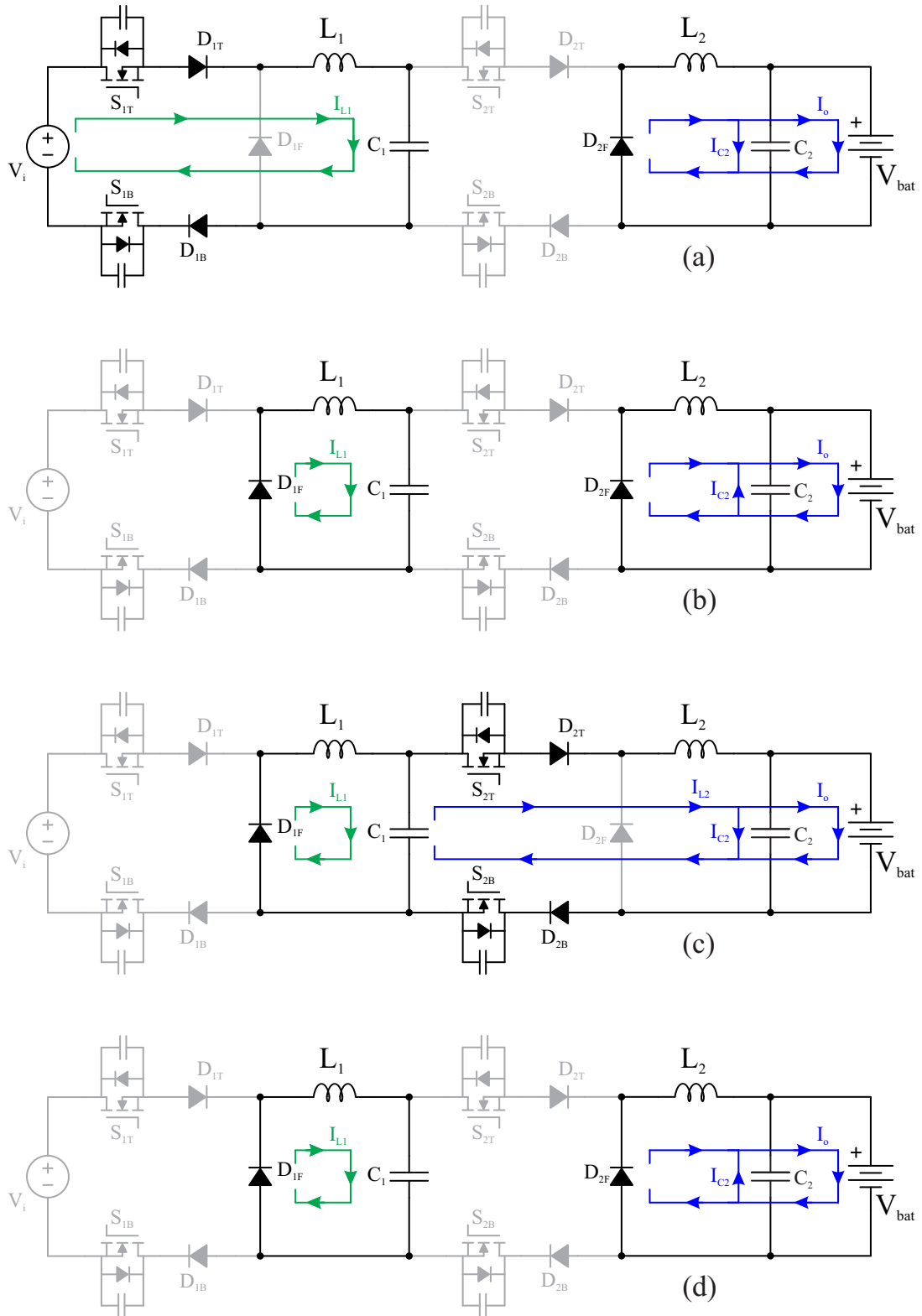
The analysis made at (KAZIMIERCZUK, 2008) considers a classic DC-DC *Buck* converter, where a constant current I_o is drained on the converter's output, thus, by the Kirchhoff's current law, the ripple at the inductor goes to the capacitor presenting a waveform like on C_2 . Something different happens on C_1 , as there is no constant current at the first stage *Buck* converter's output, a discontinuous step from the positive (charging the capacitor) i_{L1} to a negative (discharging the capacitor) $i_{L1} - i_{L2}$ occur when S_{2T} and S_{2B} start conducting. This characteristic also leads to a higher voltage ripple, as the voltage is consequence of the charge.

- **First step ($0 \rightarrow D_1 \cdot T/2$):** The switches S_{1T} and S_{1B} will be conducting along with D_{1T} and D_{1B} , so there is energy flow from V_i to be stored on C_1 through a limiting inductor L_1 , which allows voltage regulation on C_1 according to duty cycle D_1 . The switches S_{2T} and S_{2B} will be blocked along with D_{2T} and D_{2B} isolating C_2 from C_1 . As both *Buck* stages are designed to operate in CCM, L_2 still have current flowing through D_{2F} and C_2 holds on the output voltage to supply the load. This step is shown at Figure 20 (a).
- **Second step ($D_1 \cdot T/2 \rightarrow T/2$):** All of the switches S_{1T} , S_{1B} , S_{2T} and S_{2B} are blocked. Given the CCM on the converter, L_1 and L_2 still have current flowing through D_{1F} and D_{2F} , respectively, while C_2 holds on the output voltage to supply the load. This step is shown at Figure 20 (b).
- **Third step ($T/2 \rightarrow D_2 \cdot T/2 + T/2$):** The switches S_{2T} and S_{2B} will be conducting along with D_{2T} and D_{2B} , so there is energy flow from C_1 to C_2 and the load through a limiting inductor L_2 , which allows voltage regulation on the output according to duty

cycle D_2 . The switches S_{1T} and S_{1B} will be blocked along with D_{1T} and D_{1B} isolating C_1 from the input source. Given the CCM operation, L_1 still have current flowing through D_{1F} . This step is shown at Figure 20 (c).

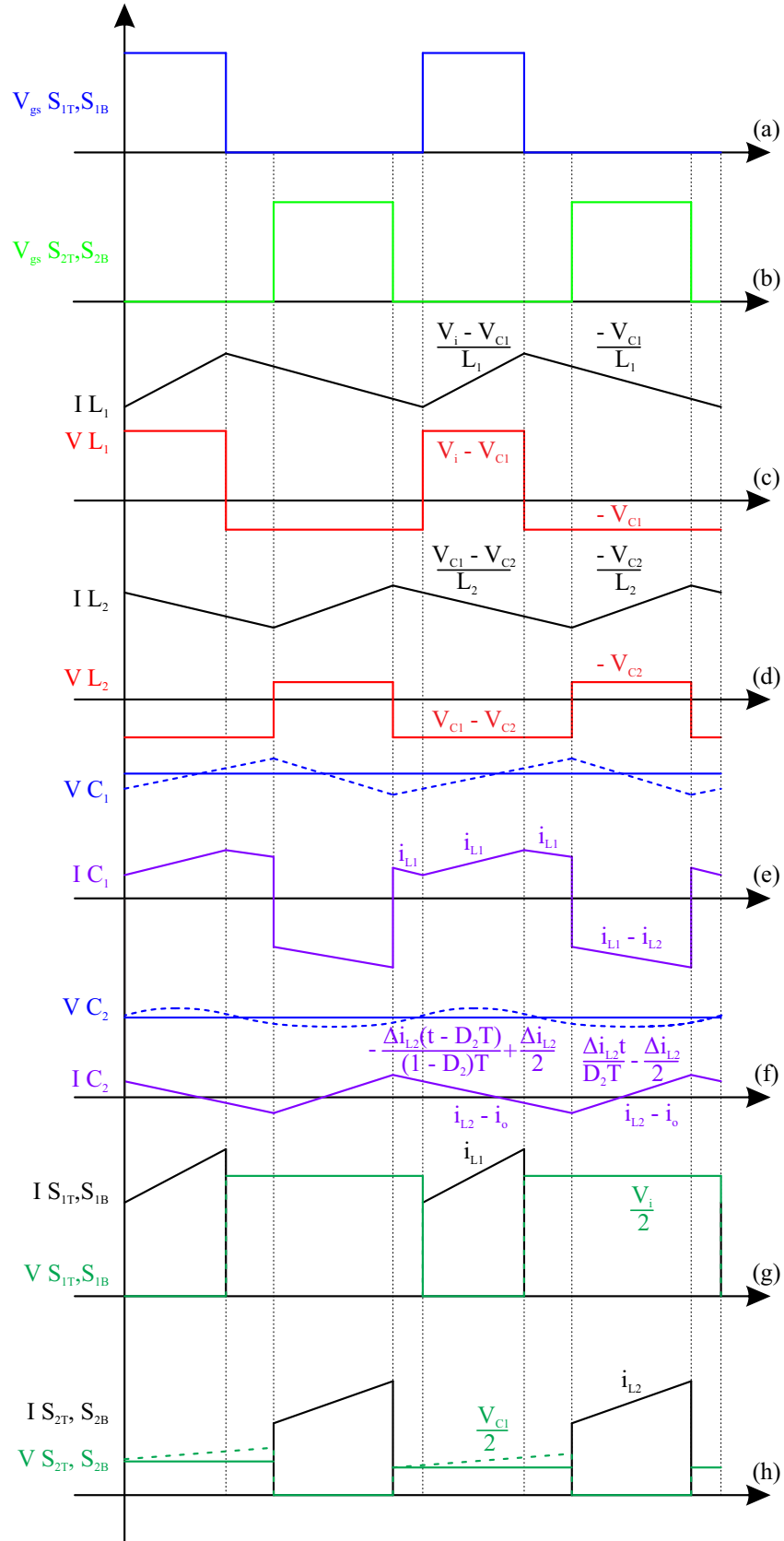
- **Fourth step ($D_2 \cdot T/2 + T/2 \rightarrow T$):** As on the second step, all of the switches S_{1T} , S_{1B} , S_{2T} and S_{2B} are blocked. Given the CCM on the converter, L_1 and L_2 still have current flowing through D_{1F} and D_{2F} , respectively, while C_2 holds on the output voltage to supply the load. This step is shown at Figure 20 (d).

Figure 20 – Operation steps on the proposed converter. (a) First operation step. (b) Second operation step. (c) Third operation step. (d) Fourth operation step.



Source: Made by the author (2023).

Figure 21 – Operation waveforms: (a) Signal on S_{1T} and S_{1B} gates; (b) Signal on S_{2T} and S_{2B} gates; (c) Voltage and current on L_1 ; (d) Voltage and current on L_2 ; (e) Voltage and current on C_1 ; (f) Voltage and current on C_2 ; (g) Voltage and current on S_{1T} and S_{1B} ; (h) Voltage and current on S_{2T} and S_{2B} ;



Source: Made by the author (2023).

4.2 TOUCH CURRENT

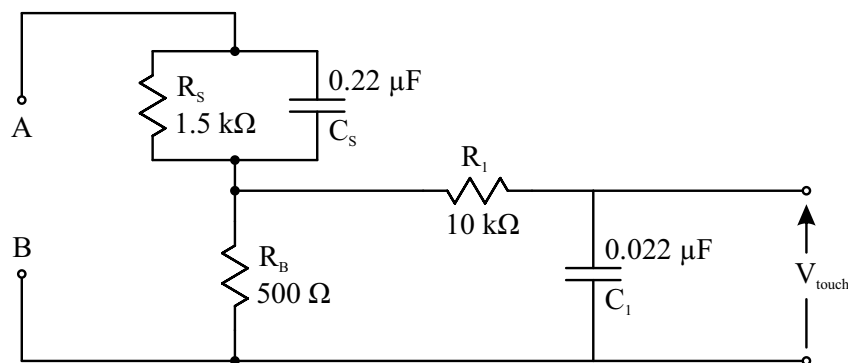
As the proposed topology has an inductor and a freewheeling diode besides the basic SGI cell, the touch current assumes a different flow than the presented on (YAO et al., 2020). Another different aspect is the input power source, as the DC-DC conversion stage is the focus on this work, it is considered a DC input power source for the touch current analysis, with the IEC 60950-1 human body impedance simulation network R_{touch} , illustrated on the Figure 22, connected through its negative rail and the DC output, either positive or negative.

The following analysis, presented by the Figure 23 and 24, is done with the human body impedance simulation network R_{touch} connected through the DC input power source and the negative rail of the DC output. On those figures, the blue highlighted circuit components are on a blocking state, the red current flow is the Common-mode (CM) touch current, the green is the Differential-mode (DM) current, magenta is the DM current parcel of the switch discharging its capacitance on the circuit and the cyan is the switch capacitance discharging current inside itself.

The current flow presented on Figure 23 and 24 occur right after the switching state change on a fast transient, either it being a switch closing or blocking. The direct current direction on the capacitors may change along the step duration.

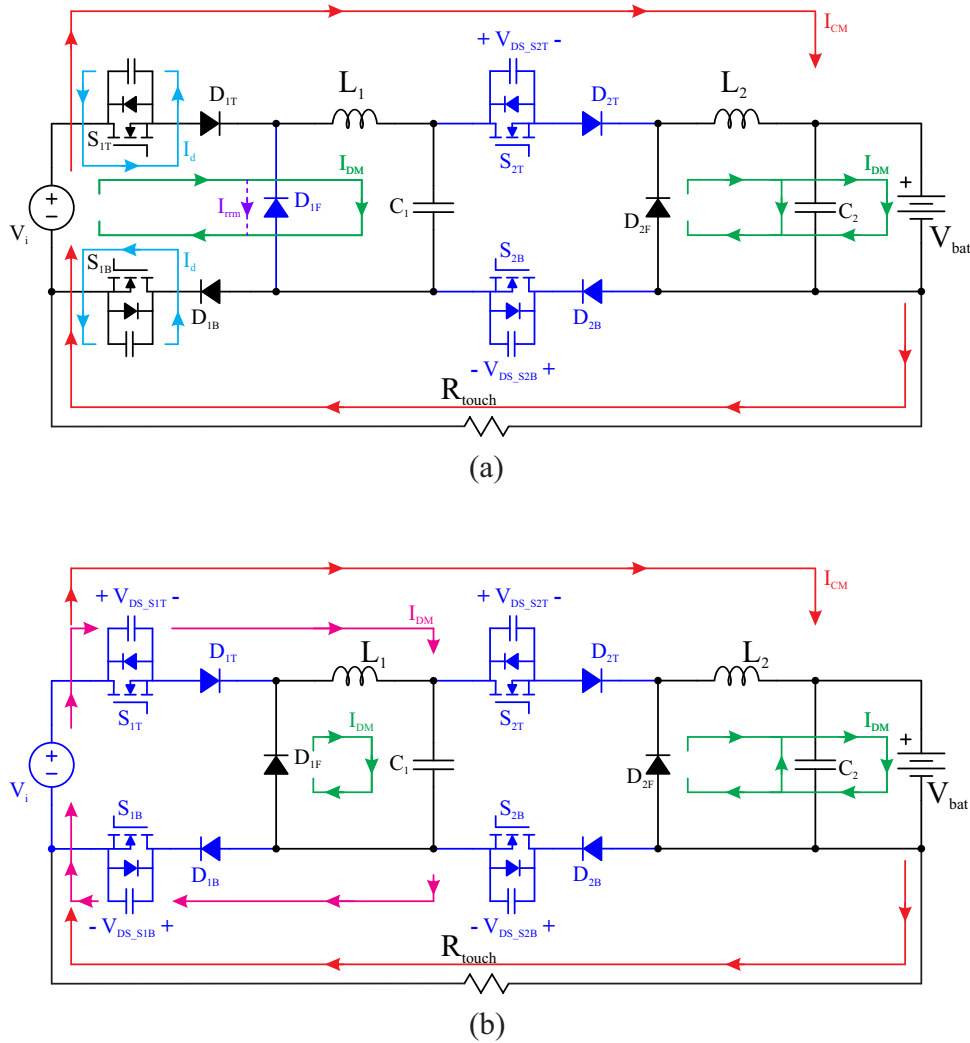
- **First step ($0 \rightarrow D_1 \cdot T/2$):** Before this step, all switches are in a blocked state and charged, thus when this step begins, the switches S_{1T} and S_{1B} will get closed, and their output capacitance will be discharged through the drain-source rail. The freewheeling diode D_{1F} gets blocked when S_{1T} and S_{1B} start conducting, which changes the voltage distribution on the CM loop through R_{touch} , raising the voltage across S_{2T} , causing a CM current flow till S_{2T} drain-source capacitance is charged to the increased voltage value. This step is shown at Figure 23 (a).
- **Second step ($D_1 \cdot T/2 \rightarrow T/2$):** At the beginning of this step, S_{1T} and S_{1B} will get blocked and their output capacitance needs to be charged. The current needed to charge it will come from V_i , and most of it is a DM parcel, will flow through L_1 and C_1 . But a

Figure 22 – Human Body Impedance Simulation Network.



Source: Made by the author (2023), adapted from IEC 60950-1.

Figure 23 – Touch current over the operation steps: (a) First step, (b) Second step.

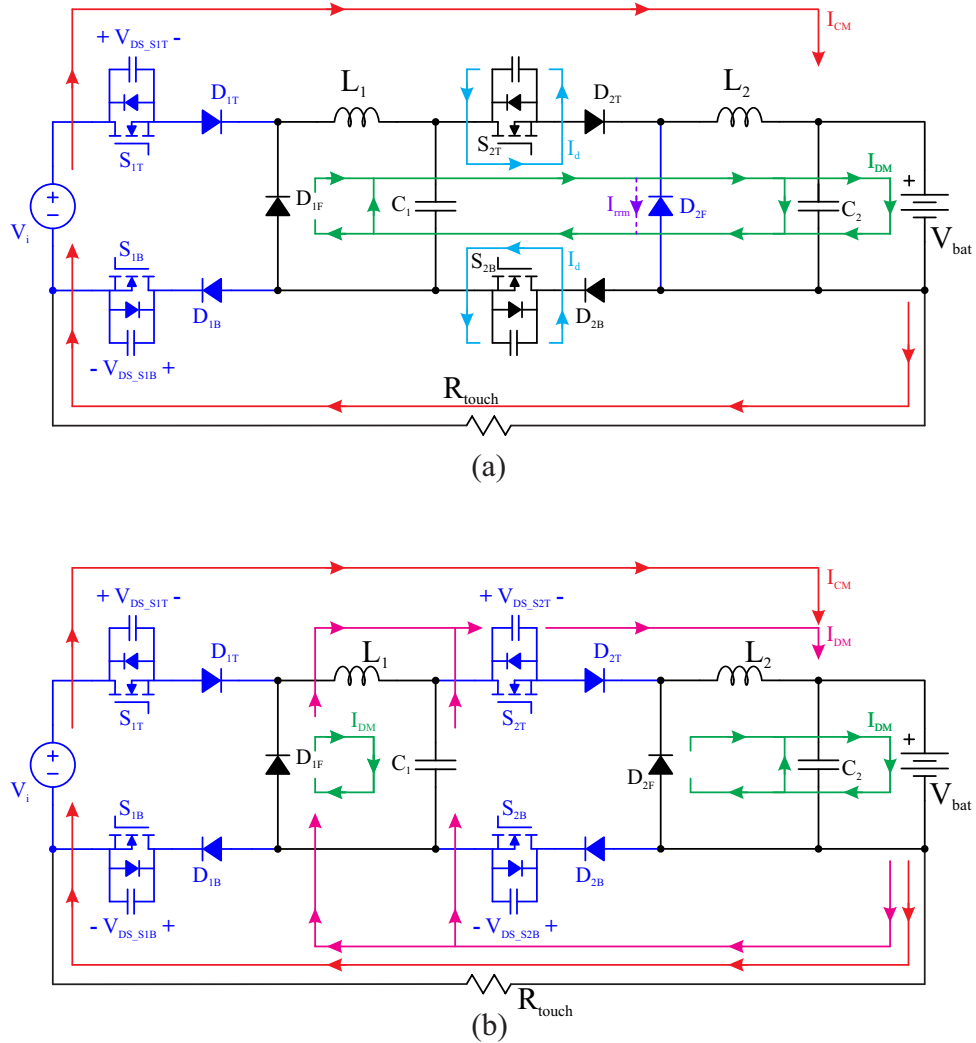


Source: Made by the author (2023).

small parcel will flow as CM through R_{touch} contributing for the touch current. It happens by the consequence of the freewheeling diode D_{1F} starting conducting and changing the voltage distribution on the CM loop. At this step, both S_{1T} and S_{2T} get their voltage increased. This step is shown at Figure 23 (b).

- **Third step ($T/2 \rightarrow D_2 \cdot T/2 + T/2$):** At this step, the switches S_{2T} and S_{2B} will start conducting, and their output capacitance will be discharged through the drain-source rail. The freewheeling diode D_{2F} gets blocked, which changes the voltage distribution on the CM loop through R_{touch} , raising the voltage across S_{1T} , causing a CM current flow till S_{1T} drain-source capacitance is charged to the increased voltage value. This step is shown at Figure 24 (a).
- **Fourth step ($D_2 \cdot T/2 + T/2 \rightarrow T$):** Here, S_{2T} and S_{2B} will get blocked and their output capacitance needs to be charged. The current needed to charge it will come from C_1 and L_1 , and most of it is a DM parcel, will flow through L_2 , C_2 and the load. But a small

Figure 24 – Touch current over the operation steps: (a) Third step, (b) Fourth step.



Source: Made by the author (2023).

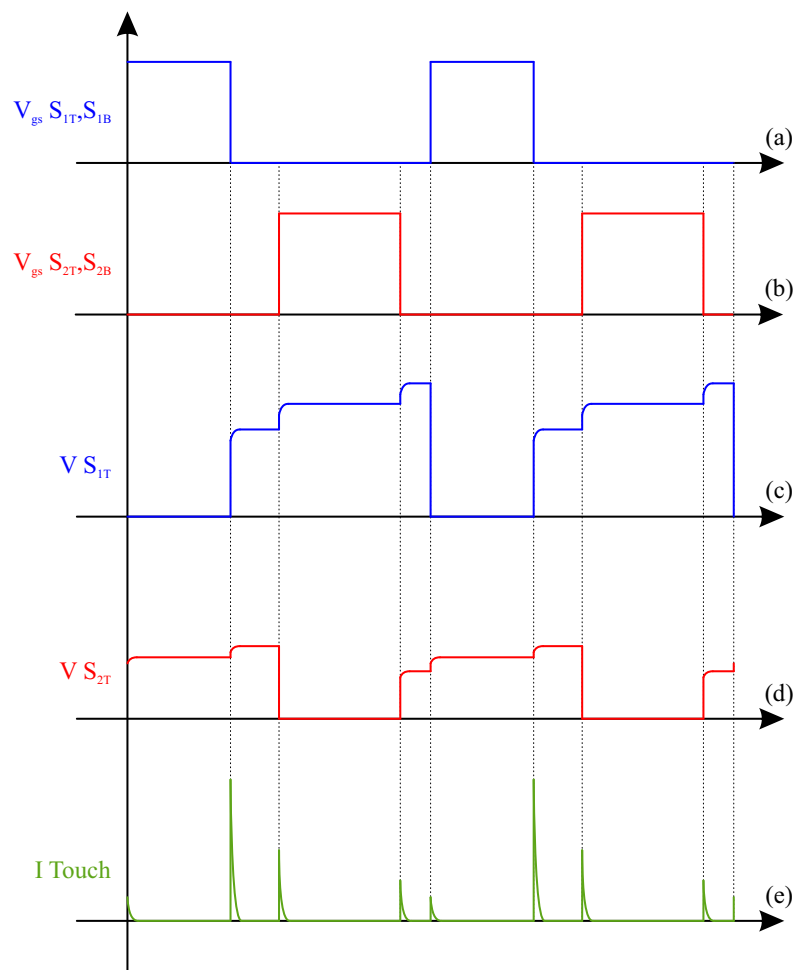
parcel will flow as CM through R_{touch} contributing for the touch current. It happens by the consequence of the freewheeling diode D_{2F} starting conducting and changing the voltage distribution on the CM loop. At this step, both S_{1T} and S_{2T} get their voltage increased. This step is shown at Figure 24 (b).

The Figure 25 shows the touch current waveform along with the gate signal and the drain-source voltage on the switches. Its possible to observe that the CM touch current peak is proportional to the sum of the positive voltage variation on the switches.

Even though the touch current mechanism is different, it has its similarities with the basic SGI cell and the touch current suppression method presented at (YAO et al., 2020) would also be effective in this topology.

On the Figure 23 and 24 also is referenced as I_{rrm} , in purple, the diode reverse recovery current, which is a differential mode current provided to blocking the diode.

Figure 25 – Touch current over the operation steps waveform: (a) Signal on S_{1T} and S_{1B} gates, $V_{gs}S_{1T}, S_{1B}$; (b) Signal on S_{2T} and S_{2B} gates, $V_{gs}S_{2T}, S_{2B}$; (c) Voltage on S_{1T} , $V_{S_{1T}}$; (d) Voltage on S_{2T} , $V_{S_{2T}}$; (e) Touch current, I_{Touch} .



Source: Made by the author (2023).

5 CONVERTER DESIGN

Independent of the input of the battery charger, the second stage DC-DC converter is designed with a DC nominal input of 400 V.

The proposed converter is designed in this chapter considering it as two single *Buck* converter as the SGI feature does not interfere on the basic operation of the converter. The analysis made for the classic *Buck* converter is still valid. The analysis used here is based on the content stated in (KAZIMIERCZUK, 2008).

The initial considerations for the converter concern the application, a battery charger also capable of supplying DC power to a generic load. The converter is designed to charge four 12 V_{DC} lead-acid batteries connected in series, so their nominal voltage would be 48 V_{DC} . This is the reference voltage when the battery is supplying the load, thus discharging. For charging the battery, a higher voltage is needed. The value of 13.60 V_{DC} is generally used as the floating voltage per battery, and can be used as a slow charging cycle or for maintaining the battery charged. A value of 14.70 V_{DC} per battery can be used for an equalizing charge. From these values the nominal converter output voltage and maximum output voltage are defined on the Equation 2 and 3, respectively.

$$V_o = 4 \cdot 13.60 V_{DC} = 54.40 V_{DC} \quad (2)$$

$$V_{o,max} = 4 \cdot 14.70 V_{DC} = 58.80 V_{DC} \quad (3)$$

When discharging, each battery is expected to be used down to 10.50 V_{DC} , as usually recommended by manufacturers, thus, the minimum value the converter needs to operate is defined on the Equation 4.

$$V_{o,min} = 4 \cdot 10.50 V_{DC} = 42 V_{DC} \quad (4)$$

The power of 2 kW is considered as it is commonly used for commercial modular rectifier modules, so the nominal output current is calculated at Equation 5.

$$I_o = \frac{P_o}{V_o} = 36.76 A \quad (5)$$

Considering the primary *Buck* converter power source is a PFC *Boost* rectifier connected to a AC utility, with nominal value of 220 V_{AC} on the University laboratory location, defining its nominal input voltage value as $V_{i1} = 400 V_{DC}$. The minimum input for this first *Buck* converter stage, according to the Equation 6, uses the minimum value of the universal AC input range and consider a multiplying factor so the maximum duty cycle D_2 is 0.49, not exceeding the limit of 0.50, allowing the isolation.

$$V_{i1,min} = V_{g,min} \cdot \sqrt{3} \cdot 1.70 = 85 V_{AC} \cdot \sqrt{3} \cdot 1.70 = 250.28 V_{DC} \quad (6)$$

The maximum input voltage value for the first *Buck* converter stage consider the maximum value of the universal AC input peak and a multiplying factor of 1.15, which deems a *Boost* rectifier gain.

$$V_{i1,max} = V_{g,max} \cdot \sqrt{3} \cdot 1.15 = 264 V_{AC} \cdot \sqrt{3} \cdot 1.15 = 525.85 V_{DC} \quad (7)$$

As the converter has two separated duty cycle, one for each converter stage, a rating between them is used to match the calculation between the two parts, this rating is shown at Equation 8, and it is selected iteratively to reduce the needed inductance for L_1 . The chosen value allowed a reasonable value of inductance on L_1 and the use of an already assembled inductor.

$$\alpha_{D1D2} = \frac{D_1}{D_2} = 0.85 \quad (8)$$

With it, the reference duty cycle could be defined as its minimum and maximum from the Equation 9 to 14.

$$D_{2,nom} = \sqrt{\frac{1}{\alpha_{D1D2}} \cdot \frac{V_o}{V_{i1}}} = 0.40 \quad (9)$$

$$D_{2,min} = \sqrt{\frac{1}{\alpha_{D1D2}} \cdot \frac{V_{o,min}}{V_{i1,max}}} = 0.31 \quad (10)$$

$$D_{2,max} = 0.49 \quad (11)$$

$$D_{1,nom} = D_{2,nom} \cdot \alpha_{D1D2} = 0.34 \quad (12)$$

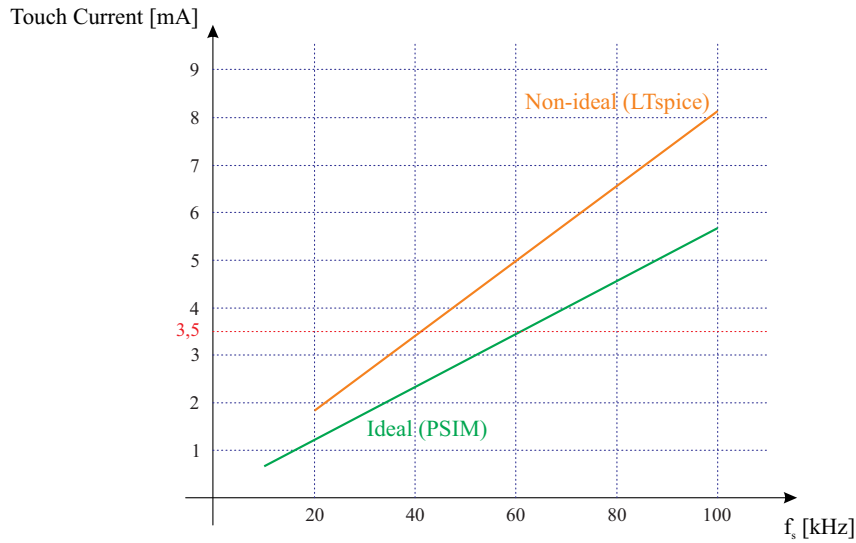
$$D_{1,min} = D_{2,min} \cdot \alpha_{D1D2} = 0.26 \quad (13)$$

$$D_{1,max} = \frac{1}{D_{2,max}} \cdot \frac{V_{o,max}}{V_{i1,min}} = 0.48 \quad (14)$$

It is expected that the converter will have high efficiency. Therefore, an efficiency factor of 99% is considered for calculations, as shown in Equation 15. Additionally, a safety margin is incorporated to account for stress on components. Thus, even if the actual efficiency is lower than anticipated, the calculated values should still meet expectations.

$$\eta_1 = 0.99 \quad \eta_2 = 0.99 \quad (15)$$

Figure 26 – Touch current according to the switching frequency.



Source: Made by the author (2023).

The switching frequency is selected as on the Equation 16. Although a higher frequency can cause a reduction in the size of inductors and capacitors, which is desirable for cost reduction, it also impacts the touch current. Reducing the switching frequency can also reduce the touch current, so, this value is strategically selected to comply with the standards on the touch current.

$$f_s = 40 \text{ kHz} \quad (16)$$

A Parameter Sweep simulation was conducted using the Altair® PSIM™ software to examine the frequency's impact on touch current. An ideal simulation was performed, incorporating additional features of the switches such as forward resistance and output capacitance, as long as the switch's reverse biased diode forward resistance and forward voltage, to analyze touch current. However, since some practical circuit features were not considered, a non-ideal simulation was also conducted using Analog Devices LTspice® software. The results of these simulations are presented in Figure 26. It can be observed that at 40kHz, both simulations comply with the relevant standards, namely IEC 60950-1 and Anatel's Act No. 930, dated February 8, 2018. The limit is highlighted in red in Figure 26.

5.1 MAGNETIC DESIGN

In this section the magnetic components, L_1 and L_2 are designed, also with the analysis made on (KAZIMIERCZUK, 2008).

L_1 Design

As stated in (KAZIMIERCZUK, 2008), the first step to define the inductance value is to define the maximum resistance, or minimum load, that the converter would start operating in

CCM. Here is defined that from 10% of the nominal load, 200 W, the converter is to be operating at CCM, so the Equation 17 sets the maximum resistance for CCM.

$$R_{L1,max} = \frac{(V_{i1,max} \cdot D_{1,min})^2}{200 \text{ W}} = 93.86 \Omega \quad (17)$$

Then, the minimum inductance value to ensure that the primary *Buck* converter operates in CCM mode, can be defined as the Equation 18.

$$L_{1,min} = \frac{R_{L1,max} \cdot (\frac{1}{\eta_1} - D_{1,min})}{2 \cdot f_s} = 879.44 \mu\text{H} \quad (18)$$

L_2 Design

The second inductor follows the same steps, also considering the converter is to be operating at CCM with 200 W or more. So the maximum resistance is defined at Equation 19, and the inductance at Equation 20.

$$R_{L2,max} = \frac{V_{o,min}^2}{200 \text{ W}} = 8.82 \Omega \quad (19)$$

$$L_{2,min} = \frac{R_{L2,max} \cdot (\frac{1}{\eta_2} - D_{2,min})}{2 \cdot f_s} = 77.57 \mu\text{H} \quad (20)$$

5.2 CAPACITOR DESIGN

In this section the capacitors, C_1 and C_2 are designed.

C_1 Design

The capacitor C_1 is designed so the voltage output of this converter stage has 1% of oscillation on nominal condition. The Equation 21 defines what is expected for the output voltage on this stage, and the Equation 23 sets the minimum capacitance for granting it.

$$V_{o1,nom} = V_{i1} \cdot D_{1,nom} = 136 \text{ V} \quad (21)$$

$$\Delta V_{o1} = 0.01 \cdot V_{o1,nom} = 1.36 \text{ V} \quad (22)$$

$$C_{1,min} = \frac{(1 - D_{1,min}) \cdot V_{o1}}{8 \cdot f_s^2 \cdot L_1 \cdot \Delta V_{o1}} = 5.79 \mu\text{F} \quad (23)$$

The L_1 considered at the Equation 23 is the further selected value on the Section 5.5, not the minimum value calculated, with it, the value would be as on the Equation 24, this value is used for simulation purposes.

$$C_{1,min} = \frac{(1 - D_{1,min}) \cdot V_{o1}}{8 \cdot f_s^2 \cdot L_{1,min} \cdot \Delta V_{o1}} = 6.57 \mu\text{F} \quad (24)$$

This value is calculated so the first stage *Buck* converter could have the ripple as shown in the Equation 22, but as it is connected to a second stage *Buck* converter, the Section 4.1 shows the reason for not getting the 1% on this stage's output. Although it is a sufficient value for an intermediary voltage on the converter, as a restrict ripple is not required there. This calculation gives the range value for the capacitor to act with the inductor.

C₂ Design

The capacitor C_2 is also designed for 1% but now for the converter output voltage, shown at the Equation 25, and the Equation 26 defines the minimum capacitance for granting it.

$$\Delta V_o = 0.01 \cdot V_o = 0.54 \text{ V} \quad (25)$$

$$C_{2,min} = \frac{(1 - D_{2,min}) \cdot V_o}{8 \cdot f_s^2 \cdot L_2 \cdot \Delta V_o} = 31.78 \mu\text{F} \quad (26)$$

Also, the L_2 considered at the Equation 26 is the further selected value on the Section 5.5, not the minimum value calculated, with it, the value would be as on the Equation 27.

$$C_{2,min} = \frac{(1 - D_{2,min}) \cdot V_o}{8 \cdot f_s^2 \cdot L_{2,min} \cdot \Delta V_o} = 69.84 \mu\text{F} \quad (27)$$

5.3 PRIMARY BUCK CONVERTER STRESSES

Before selecting the components to build the converter, it is needed to estimate the stresses they need to operate normally with no damage. This section estimate these stresses.

5.3.1 Inductor Current Stresses

On a *Buck* converter, for CCM, the inductor current will have a DC parcel which corresponds to the output average current plus a ripple parcel from the switches commutation, so, the peak current on the inductor is

$$I_{L1,Pk} = I_{o1,avg,max} + \frac{\Delta I_{L1}}{2} \quad (28)$$

Where the ΔI_{L1} value corresponds to the peak-to-peak ripple current on the inductor L_1 , calculated at the Equation 29.

$$\Delta I_{L1} = \frac{V_{o1} \cdot (1 - D_{1,nom})}{f_s \cdot L_1} = 2.25 \text{ A} \quad (29)$$

The maximum value for the average output current on the first *Buck* converter ($I_{o1,avg,max}$) will occur at nominal power on its lowest output voltage, hence, on its lowest input voltage with applied $D_{1,max}$ plus the half of the L_1 inductor's ripple current, also deducted in (KAZIMIER-CZUK, 2008).

$$I_{L1,pk} = \frac{P_o}{V_{i1,min} \cdot D_{1,max}} + \frac{V_{i1,min} \cdot D_{1,max}(1 - D_{1,max})}{2 \cdot f_s \cdot L_1} = 17.45 \text{ A} \quad (30)$$

As for the maximum average current on the inductor L_1 , it will be the same as the maximum average output current on the primary *Buck* converter.

$$I_{L1,avg,max} = \frac{P_o}{V_{o1,min}} = 16.67 \text{ A} \quad (31)$$

5.3.2 Switch Voltage Stresses

On the primary *Buck* converter the highest voltage stress on the switches S_{1T} and S_{1B} will occur when they are open. At that moment, the input voltage will be shared with both switches. Thus, the maximum voltage stress on the switches happens at maximum input voltage with the value given by Eq. (32).

$$V_{S1,max} = \frac{V_{i1,max}}{2} = 262.92 \text{ V} \quad (32)$$

Both series diodes D_{1T} and D_{1B} will be direct polarized, being the switches open or conducting, so they won't have voltage stresses.

5.3.3 Switch Current Stresses

The peak current on the switches S_{1T} , S_{1B} and on the series diodes D_{1T} and D_{1B} will be the same as on the inductor L_1 .

$$I_{S1,pk} = I_{D1,pk} = I_{L1,pk} = 17.45 \text{ A} \quad (33)$$

The maximum average current for the switches and series diodes on the primary *Buck* will be the maximum average current on its output weighted by $D_{1,max}$.

$$I_{S1,avg,max} = I_{D1,avg,max} = \frac{P_o}{V_{o1,min}} \cdot D_{1,max} = 7.99 \text{ A} \quad (34)$$

5.3.4 Freewheeling Diode Voltage Stresses

When both switches S_{1T} and S_{1B} are conducting, the input voltage will be applied to the freewheeling diode D_{1F} , hence, the maximum input voltage will be the maximum voltage stress at the freewheeling diode.

$$V_{D1F,max} = V_{i1,max} = 525.85 \text{ V} \quad (35)$$

5.3.5 Freewheeling Diode Current Stresses

The peak current on the freewheeling diode will be the same as on the switches and on the inductor L_1 .

$$I_{D1F,Pk} = I_{S1,Pk} = I_{L1,Pk} = 17.45 \text{ A} \quad (36)$$

As the current on the freewheeling diode D_{1F} is complementary to the current on the switches S_{1T} and S_{1B} , the maximum average current for the freewheeling diode on the primary *Buck* will be the average current on its output weighted by $1 - D_{1,min}$, as it conducts when the switches are open.

$$I_{D1F,avg,max} = \frac{P_o}{V_{o1,max}} \cdot (1 - D_{1,min}) = 10.79 \text{ A} \quad (37)$$

5.3.6 Capacitor Voltage Stresses

The capacitor maximum voltage stress on the primary *Buck* will be its maximum output voltage which happens on its highest input voltage with applied $D_{1,min}$.

$$V_{C1,max} = V_{i1,max} D_{1,min} = 137.01 \text{ V} \quad (38)$$

5.4 SECONDARY BUCK CONVERTER STRESSES

5.4.1 Inductor Current Stresses

On the secondary *Buck* converter, the inductor peak current can be calculated similarly to the Equation 28 with ΔI_{L2} (calculated on the Equation 40) corresponding to the peak-to-peak ripple current on the inductor L_2 and $I_{o,avg,max}$ to the maximum average output current on the converter.

$$I_{L2,Pk} = I_{o,avg,max} + \frac{\Delta I_{L2}}{2} \quad (39)$$

$$\Delta I_{L2} = \frac{V_o \cdot (1 - D_{2,nom})}{f_s \cdot L_2} = 4.79 \text{ A} \quad (40)$$

Equivalently, the condition for the peak inductor L_2 current will be on nominal power and the lowest output voltage of the converter.

$$I_{L2,Pk} = \frac{P_o}{V_{o,min}} + \frac{V_{o,min}(1 - D_{2,min})}{2f_s L_1} = 49.75 \text{ A} \quad (41)$$

The maximum average current on the inductor L_2 will be the same as the output maximum average current for the converter.

$$I_{L2,avg,max} = \frac{P_o}{V_{o,min}} = 47.62 \text{ A} \quad (42)$$

5.4.2 Switch Voltage Stresses

The voltage stress on the switches S_{2T} and S_{2B} will be the half of the input voltage on the secondary *Buck* converter, so, the highest voltage stress will occur on the highest output voltage on the primary *Buck*, hence, at maximum input voltage with applied $D_{1,min}$.

$$V_{S2,max} = \frac{V_{i1,max}D_{1,min}}{2} = 68.51 \text{ V} \quad (43)$$

Both series diodes D_{2T} and D_{2B} also wont have voltage stresses as D_{1T} and D_{1B} .

5.4.3 Switch Current Stresses

The peak current on the switches S_{2T} , S_{2B} and on the series diodes D_{2T} and D_{2B} will be the same as on the inductor L_2 .

$$I_{S2,Pk} = I_{D2,Pk} = I_{L2,Pk} = 49.75 \text{ A} \quad (44)$$

The maximum average current for the switches and series diodes on the secondary *Buck* will be the maximum average current on its output weighted by $D_{2,nom}$.

$$I_{S2,avg,max} = I_{D2,avg,max} = \frac{P_o}{V_{o,min}} D_{2,nom} = 19.05 \text{ A} \quad (45)$$

5.4.4 Freewheeling Diode Voltage Stresses

The maximum input voltage on the secondary *Buck* will be the maximum voltage stress on its freewheeling diode.

$$V_{D2F,max} = V_{i1,max}D_{1min} = 137.01 \text{ V} \quad (46)$$

5.4.5 Freewheeling Diode Current Stresses

The peak current on the freewheeling diode will be the same as on the switches and on the inductor L_2 .

$$I_{D2F,Pk} = I_{S2,Pk} = I_{L2,Pk} = 49.75 \text{ A} \quad (47)$$

The maximum average current for the freewheeling diode on the secondary *Buck* will be the maximum average current on its output weighted by $1 - D_{2,nom}$.

$$I_{D2F,avg,max} = \frac{P_o}{V_{o,min}} \cdot (1 - D_{2,nom}) = 28.57 \text{ A} \quad (48)$$

5.4.6 Capacitor Voltage Stresses

The capacitor C_2 maximum voltage stress will be the maximum output voltage on the converter.

$$V_{C2,max} = V_{o,max} = 58.80 \text{ V} \quad (49)$$

5.5 COMPONENT SELECTION

In this section the components were selected according to the application specifics, the design exposed in section 5.1 and 5.2, and the estimated voltage and current stress, presented in sections above.

Selecting S_1

Despite the voltage stress on the S_1 switch pair, S_{1T} and S_{1B} , would not require a high voltage rating switch, the SGI brings that need, as a transformer is not used, and a electric strength test is required to comply with commercial product standards, IEC 60950-1 and Anatel's Act No. 930, of February 8, 2018. Thus, the regular converter components have to withstand the voltage demanded for the test, and the switches are included in it.

As the reference standard, IEC 60950-1, requires 1500V peak or DC, given by the Table 5B Part 1, the same value as item 5.13.1 on Anatel's Act No. 930, of February 8, 2018, on the voltage withstand test, the voltage distribution on each component is analyzed. As shown in Figure 27, and using the Kirchhoff's loop rule, there is two significant loop to analyze, where the voltage stress will be the highest, as presented on Equation 50 and 51. As the voltage across the inductors L_1 and L_2 are not significant for this case, the group of switches and diodes: S_{1T} , D_{1T} , S_{2T} and D_{2T} will have to withstand the test voltage as same as the group S_{1B} , D_{1B} , S_{2B} and D_{2B} .

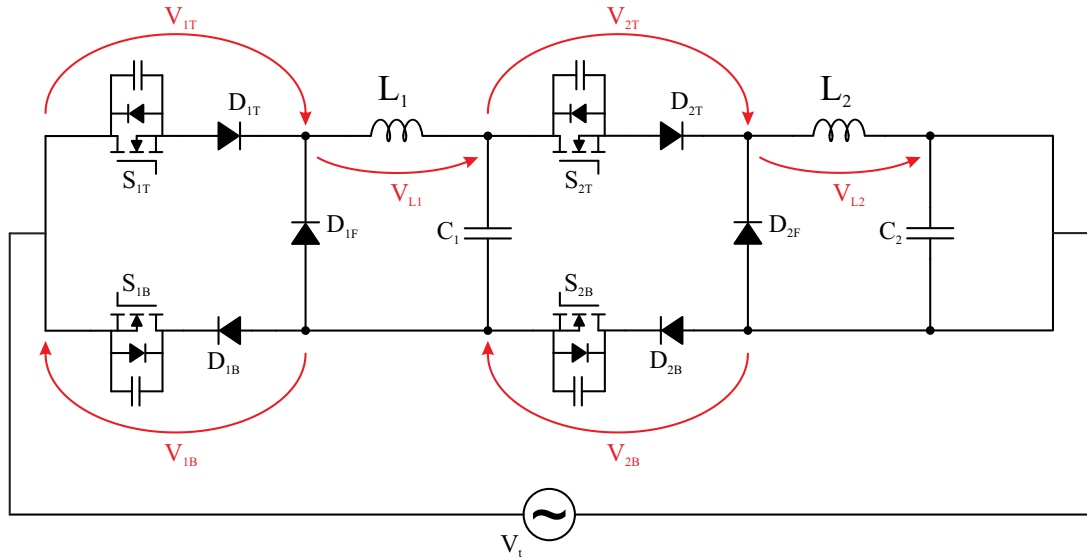


Figure 27 – Voltage distribution on a withstand test for the proposed topology.

$$V_{1T} + V_{L1} + V_{2T} + V_{L2} + V_t = 0 \quad \Rightarrow \quad V_{1T} + V_{2T} = -V_t \quad (50)$$

$$V_{1B} + V_{2B} + V_t = 0 \quad \Rightarrow \quad V_{1B} + V_{2B} = -V_t \quad (51)$$

Each pair composed by a diode and a switch, as in S_{1T} and D_{1T} , is connected in anti-series on the voltage blocking context, thus, each pair component will be blocking the voltage on a different time than the other in a complementary way. It means the group S_{1T} and S_{2T} will have to withstand the test voltage if it is positive from the input to output as same as the group D_{1B} and D_{2B} . But the group D_{1T} and D_{2T} has to withstand the test voltage if it is negative as same as the group S_{1B} and S_{2B} .

Thus, each diode or switch has to withstand at least more than half of the test voltage of 750 V. But, as the voltage distribution depends on some characteristics of the component, as the output capacitance, that can vary from one piece to another, the voltage generally is not divided equally, thus a margin is needed to assure the test realization.

A second aspect must be considered on the switch selection is the touch current, that circulates through the drain-source capacitance, so, the lower this capacitance, the better for the SGI application.

Considering these aspects, the CREE Silicon Carbide Power MOSFET C3M0032120K is selected for S_{1T} and S_{1B} . It can withstand 1200 V and a continuous drain current of 63 A. The drain-source capacitance is typically 121 pF. It fulfills the requisites with a good margin.

Selecting S_2

The switches S_{2T} and S_{2B} have a higher current rating than S_{1T} and S_{1B} , as calculated in Equation 45 and 44, but a lower voltage rating as in Equation 43, however, the standard electric strength test depends on these switches also, therefore, the voltage rating needs to be the same as in S_{1T} and S_{1B} .

As the C3M0032120K supports both the current and voltage stresses for S_{2T} and S_{2B} , it is also selected for them. Selecting the same component tends to help in some aspects on a product manufacture, as in the purchasing a large amount for reducing the price.

Selecting D_1

Both diodes D_{1T} and D_{1B} also need a higher voltage rating to comply with the electric strength standard. So the 20ETS12 is picked to fulfill all the aforementioned characteristics. It also has a 1200 V rating and supports 20 A.

The diodes D_{1T} , D_{1B} , D_{2T} and D_{2B} , do not need to be a fast recovery diode because the switch will block the current, so they can be regular power diodes.

Selecting D_2

The diodes D_{2T} and D_{2B} also should comply with the electric strength standard, so the 40EPS12 is selected for having 1200 V rating and supporting 40 A.

Selecting D_{1F}

Aside from the current rating calculated on the Equation 37 and 36 and the voltage rating, on the Equation 35, the diode D_{1F} needs to be a fast recovery diode. As it is a freewheeling diode, it needs to block the current by itself when reverse polarized, thus it needs a lower reverse recovery time.

The diode BYT30P-1000 is selected for fulfilling those characteristics, though the MUR3060 can be used alternatively. They have a voltage rating of 1000 V and 600 V respectively, and a current rating of 30 A.

Selecting D_{2F}

As D_{2F} is also a freewheeling diode, it also needs to be a fast recovery diode, so the MBR40250-TG is selected with a voltage rating of 250 V respectively, and a current rating of 40 A.

The forward voltage was also considered on the semiconductor picking, as it impacts on the converter efficiency.

Selecting L_1

Given the minimum inductance calculated by Equation 18 and the current stress by Equation 30 and 31, for convenience, two already assembled inductor, that had already been used in another converter, of 499 μH were selected to operate in series compounding the needed inductance in Equation 52.

$$L_1 = 2 \cdot 499 \mu\text{H} = 998 \mu\text{H} \quad (52)$$

Both selected inductors are identical, each constructed with two stacked units of sendust toroid cores and 43 coils of 14 AWG two-wire configuration.

With this selected inductance, the expected oscillating current at the inductor L_1 is calculated on the Equation 53 and 54.

$$\Delta I_{L_1} = \frac{V_{o1} \cdot (1 - D_{1,nom})}{f_s \cdot L_1} = 2.25 \text{ A} \quad (53)$$

$$\frac{\Delta I_{L_1}}{I_{o1}} = 0.15 = 15.29\% \quad (54)$$

Selecting L_2

For the L_2 , the minimum inductance is calculated on the Equation 20 and the current stress by Equation 41 and 42, for convenience, two already assembled inductor of 341 μH were selected to operate in parallel compounding the needed inductance in Equation 55.

$$L_2 = \frac{341 \mu\text{H}}{2} = 170.50 \mu\text{H} \quad (55)$$

Both selected inductors are identical, each constructed with three stacked units of sendust toroid cores and 29 coils of 12 AWG two-wire configuration.

With this selected inductance, the expected oscillating current at the inductor L_2 is calculated on the Equation 56 and 57.

$$\Delta I_{L_2} = \frac{V_o \cdot (1 - D_{2,nom})}{f_s \cdot L_2} = 4.79 \text{ A} \quad (56)$$

$$\frac{\Delta I_{L_2}}{I_o} = 0.13 = 13.02\% \quad (57)$$

Selecting C_1

With the minimum value defined at Equation 23, two commercial polyester capacitors of $3.30 \mu\text{F}$, 250 V rated, were selected to be connected in parallel on the output of the first *Buck* converter stage. One capacitor of Topmay TMCFO3 series is used as the reference part number.

$$C_1 = 2 \cdot 3.30 \mu\text{F} = 6.60 \mu\text{F} \quad (58)$$

Selecting C_2

As the value for the minimum C_2 capacitance, defined on the Equation 26, is high enough that a matching commercial polyester capacitor is hard to find, so, an electrolytic capacitor is selected, but its Equivalent Series Resistance (ESR) is significant for the output voltage ripple. If a value close to the calculated one is selected, then the ripple would increase to a significantly higher value than 1%.

On an electrolytic capacitor, the higher is the capacitance, the lower is the ESR, so, the solution for the output voltage ripple is to select a higher capacitance value. Thus, two capacitors with $820 \mu\text{F}$ (as in Equation 59), 100 V rated, were selected with the Capxon KM821M100K355A as reference part number. Although this amount of capacitance is not necessary, the ESR present in this capacitor technology causes it to increase.

$$C_1 = 2 \cdot 820 \mu\text{F} = 1640 \mu\text{F} \quad (59)$$

5.6 ESTIMATION OF POWER LOSSES

In this section, an estimation of the power losses is made for the proposed converter based on the analysis on (KAZIMIERCZUK, 2008). The losses are estimated for each component based on their characteristics and their employment on the converter, then, the sum of the losses of each component results on the estimated losses on the converter, thus, it is possible to estimate the efficiency.

For the estimation, each converter stage is considered as a independent DC-DC *Buck*.

Table 3 – Internal capacitances on the SiC Power MOSFET C3M0032120K.

Datasheet	
C_{iss}	3357 pF
C_{oss}	129 pF
C_{rss}	8 pF

Source: Made by the author (2023), with data provided on C3M0032120K datasheet.

5.6.1 Initial Considerations for the Estimation

Before estimating the power losses, some considerations are taken about the components. Starting by the switches, S_{1T} , S_{1B} , S_{2T} and S_{2B} , the datasheet of its part C3M0032120K provides the input capacitance (C_{iss}), output capacitance (C_{oss}) and the Reverse Transfer Capacitance (C_{rss}), with the values displayed at Table 3. Therefore, to obtain the capacitance between each of switch's terminals, the Equation 60, 61 and 62 are used.

$$C_{iss} = C_{gd} + C_{gs} \quad (60)$$

$$C_{oss} = C_{ds} + C_{gd} \quad (61)$$

$$C_{rss} = C_{gd} \quad (62)$$

With it, one can simply reach the Equation 63, 64 and 65 and calculate the capacitance between the switch's terminals, presented in the Table 4. This will be further used on the losses calculation.

$$C_{gd} = C_{rss} \quad (63)$$

$$C_{ds} = C_{oss} - C_{rss} \quad (64)$$

$$C_{gs} = C_{iss} - C_{rss} \quad (65)$$

Each piece compounding the inductor L_1 has a resistance of 19.90 mΩ, estimated by the cooper area and length. As two pieces are used in series, the resistance of L_1 is calculated on the Equation 66. As for L_2 , also two pieces are used, but connected in parallel, and the resistance of each is 20 mΩ, so the Equation 67 calculates its equivalent resistance.

Table 4 – Calculated terminal capacitances on the SiC Power MOSFET C3M0032120K.

Calculated according to Datasheet

C_{gd}	8 pF
C_{gs}	3349 pF
C_{ds}	121 pF

Source: Made by the author (2023).

Table 5 – Diodes forward voltage and resistance observed at their datasheet.

Diode data, according to Datasheet

$V_{F,D1}$	1.10 V
$R_{F,D1}$	10.40 mΩ
$V_{F,D2}$	1.10 V
$R_{F,D2}$	7.16 mΩ
$V_{F,D1F}$	1.85 V
$V_{F,D2F}$	0.86 V

Source: Made by the author (2023).

$$r_{L1} = 2 \cdot 19.90 \text{ m}\Omega = 39.80 \text{ m}\Omega \quad (66)$$

$$r_{L2} = \frac{20 \text{ m}\Omega}{2} = 10 \text{ m}\Omega \quad (67)$$

The Table 5 brings the diodes forward voltage and resistance observed at their datasheet.

As the forward resistances on both D_{1F} and D_{2F} were not specified on the datasheet, a value for them were approximated by the forward voltage x forward current ($V_F \times I_F$) characteristic graph, as, $R_{F,D1F} = 10 \text{ m}\Omega$ and $R_{F,D2F} = 18 \text{ m}\Omega$, so their conduction losses could be estimated.

The capacitor's ESR varies with some factors, as frequency and temperature, thus, the value presented on the datasheet was pondered so it could get closer to the application's circumstances. The parallel association was also considered on the Equation 68 and 69.

$$r_{c1} = \frac{1.20 \text{ m}\Omega}{2} = 0.60 \text{ m}\Omega \quad (68)$$

$$r_{c2} = \frac{200 \text{ m}\Omega}{2} = 100 \text{ m}\Omega \quad (69)$$

The load resistance on nominal condition for the first *Buck* converter is needed and calculated on the Equation 70.

$$R_{o1} = \frac{V_{o1}^2}{P_o} = 9.25 \Omega \quad (70)$$

While the load resistance on nominal condition for the second *Buck* converter is shown at the Equation 71.

$$R_{o2} = \frac{V_o^2}{P_o} = 1.48 \Omega \quad (71)$$

A weighting, also defined at (KAZIMIERCZUK, 2008), is used to include the inductor peak-to-peak current ripple on the power loss estimation. It is stated at Equation 72 for the first stage *Buck* converter. And the inductor current ripple according to D_1 is defined at Equation 73, as needed for this weighting.

$$P_{\Delta IL1}(D_1) = 1 + \frac{1}{12} \cdot \left[\frac{\Delta i_{L1}(D_1)}{\frac{V_{i1} \cdot D_1}{R_{o1}}} \right]^2 \quad (72)$$

$$\Delta i_{L1}(D_1) = \frac{(V_{i1} \cdot D_1) \cdot (1 - D_1)}{f_s \cdot L_1} \quad (73)$$

The same weighting can be done for the peak-to-peak current ripple on L_2 with the Equation 74 while the inductor current ripple according to D_2 is defined at Equation 75.

$$P_{\Delta IL2}(D_2) = 1 + \frac{1}{12} \cdot \left[\frac{\Delta i_{L2}(D_2)}{\frac{V_{o1} \cdot D_2}{R_{o2}}} \right]^2 \quad (74)$$

$$\Delta i_{L2}(D_2) = \frac{(V_{o1} \cdot D_2) \cdot (1 - D_2)}{f_s \cdot L_2} \quad (75)$$

5.6.2 Losses on the First Stage Buck Converter

On this section the power losses on the first stage *Buck* converter are estimated based on the analysis at (KAZIMIERCZUK, 2008).

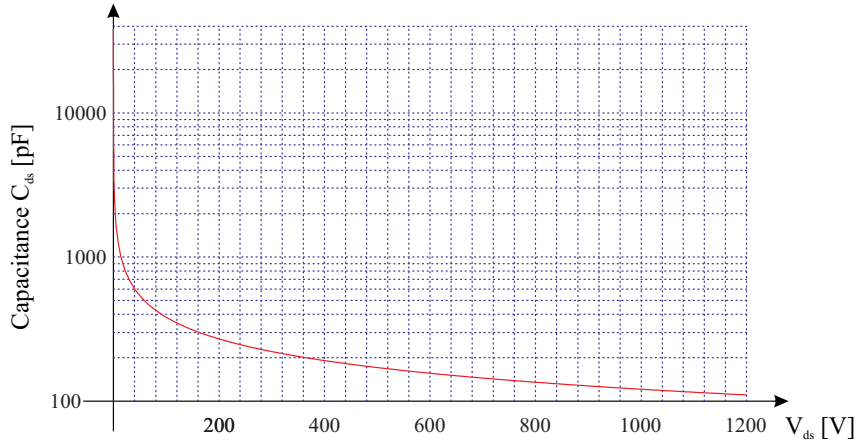
Losses on S_{1T} and S_{1B}

The switches S_{1T} and S_{1B} have losses both on switching and conduction. The switching power losses, estimated by the Equation 77, vary according with the drain-to-source capacitance, which also have a non-linear variation according to the voltage applied to it. The capacitance could be verified at the switch's datasheet if a graph is provided, or approximated by the Equation 76 and shown in Figure 28, where, in this case, the datasheet's presented capacitance is given considering a test with $V_{ds} = 1000 \text{ V}$.

$$C_{ds,v}(V_{ds}) = \frac{\sqrt{1000} \cdot C_{ds1000}}{\sqrt{V_{ds}}} \quad (76)$$

Although the common-mode touch current causes changes on the voltage distribution, which also causes a different capacitance C_{ds} on the switch, the converter is expected to operate

Figure 28 – Switch drain-to-source capacitance approximation.



Source: Made by the author (2023).

without it on a regular situation, so, in these circumstances, both S_{1T} and S_{1B} will have half of the input voltage, hence, the capacitance used on the calculation is the $C_{ds,200V}$, which is the capacitance applied when the switch has 200 V on it.

$$P_{sw1} = \frac{2}{3} \cdot f_s \cdot C_{ds,200V} \cdot \left(\frac{V_{o1}}{2} \right)^2 = 0.29 \text{ W} \quad (77)$$

As for the conducting power losses on the switches S_{1T} and S_{1B} , they are estimated on the Equation 78. On the datasheet, the switch's r_{DS} is given as 32 mΩ typically.

$$P_{rDS1} = \frac{r_{DS} \cdot D_{1,nom}}{R_{o1}} \cdot P_{\Delta IL1}(D_{1,nom}) \cdot P_o = 2.36 \text{ W} \quad (78)$$

Losses on D_{1T} and D_{1B}

The diodes D_{1T} and D_{1B} will have their power losses on the forward voltage across them and on their conducting resistance. The parcel on the conducting resistance is displayed at the Equation 79.

$$P_{RD1} = \frac{R_{F,D1} \cdot D_{1,nom}}{R_{o1}} \cdot P_{\Delta IL1}(D_{1,nom}) \cdot P_o = 0.77 \text{ W} \quad (79)$$

While the parcel on the forward voltage is estimated at the Equation 80.

$$P_{VD1} = \frac{V_{F,D1} \cdot D_{1,nom}}{V_{i1} \cdot D_{1,nom}} \cdot P_o = 5.50 \text{ W} \quad (80)$$

Losses on D_{1F}

The same occurs on D_{1F} , with the conducting resistance parcel at the Equation 81.

$$P_{RF1} = \frac{R_{F,D1F} \cdot (1 - D_{1,nom})}{R_{o1}} \cdot P_{\Delta IL1}(D_{1,nom}) \cdot P_o = 1.43 \text{ W} \quad (81)$$

And the forward voltage parcel at Equation 82.

$$P_{VF1} = \frac{V_{F,D1F} \cdot (1 - D_{1,nom})}{V_{i1} \cdot D_{1,nom}} \cdot P_o = 17.96 \text{ W} \quad (82)$$

Losses on L_1

The power loss on the inductor is caused by the copper resistance and estimated on the Equation 83.

$$P_{rL1} = \frac{r_{L1}}{R_{o1}} \cdot P_{\Delta IL1}(D_{1,nom}) \cdot P_o = 8.62 \text{ W} \quad (83)$$

Losses on C_1

The power losses on the capacitors are attributed to their ESR, and for C_1 , estimated by the Equation 84.

$$P_{rC1} = \frac{r_{C1} \cdot R_{o1} \cdot (1 - D_{1,nom})^2}{12 \cdot f_s^2 \cdot L_1^2} \cdot P_o = 0.25 \text{ mW} \quad (84)$$

Summarizing the Power Losses on the First Stage Buck Converter

At the Table 6 is summarized the power loss for the first stage *Buck* converter estimated previously, with P_{Loss1} being the total power loss, calculated at Equation 85, considering also the duplicated component losses, as P_{sw1} , which is duplicated by occurring at S_{1T} and S_{1B} .

$$P_{Loss1} = 2 \cdot (P_{sw1} + P_{rDS1} + P_{rD1} + P_{VD1}) + P_{RF1} + P_{VF1} + P_{rL1} + P_{rC1} = 45.83 \text{ W} \quad (85)$$

With it, the estimated efficiency on the first stage *Buck* converter is 97.71% for the nominal condition operation.

Besides the nominal condition operation point, the Figure 29 shows the total losses on the first stage *Buck* converter according to the converter's output power.

Besides the power loss increases while the output power is increasing, the power delivered on the converter output increases in a significantly higher rate, thus, the efficiency chart for the first stage *Buck* converter have a different behavior, shown at Figure 30.

5.6.3 Losses on the Second Stage Buck Converter

On this section the power losses on the second stage *Buck* converter are estimated.

Table 6 – Summarized power losses on the first stage *Buck* converter.

Power Losses: First Stage <i>Buck</i> Converter	
P_{sw1}	0.29 W
P_{rDS1}	2.36 W
$P_{total\ on\ S1}$	2.65 W
P_{RD1}	0.77 W
P_{VD1}	5.50 W
$P_{total\ on\ D1}$	6.27 W
P_{RF1}	1.43 W
P_{VF1}	17.96 W
$P_{total\ on\ D1F}$	19.39 W
P_{rL1}	8.62 W
P_{rC1}	0.25 mW
P_{Loss1}	45.83 W

Source: Made by the author (2023).

Losses on S_{1T} and S_{1B}

The same way as on the first stage *Buck* converter, the switches on the second stage S_{2T} and S_{2B} also have losses both on switching and conduction. The switching power losses, estimated by the Equation 86.

Although the common-mode touch current also cause changes on the voltage distribution on the second stage converter, causing also a different capacitance C_{ds} on the switch, the converter is expected to operate without it on a regular situation, so, in this circumstances, both S_{2T} and S_{2B} have half of the input voltage, or the output voltage of the first stage converter, hence, the capacitance used on the calculus is the $C_{ds,68V}$, which is the capacitance applied when the switch have 68 V on it.

$$P_{sw2} = \frac{2}{3} \cdot f_s \cdot C_{ds,68V} \cdot \left(\frac{V_{o1}}{2} \right)^2 = 0.06 \text{ W} \quad (86)$$

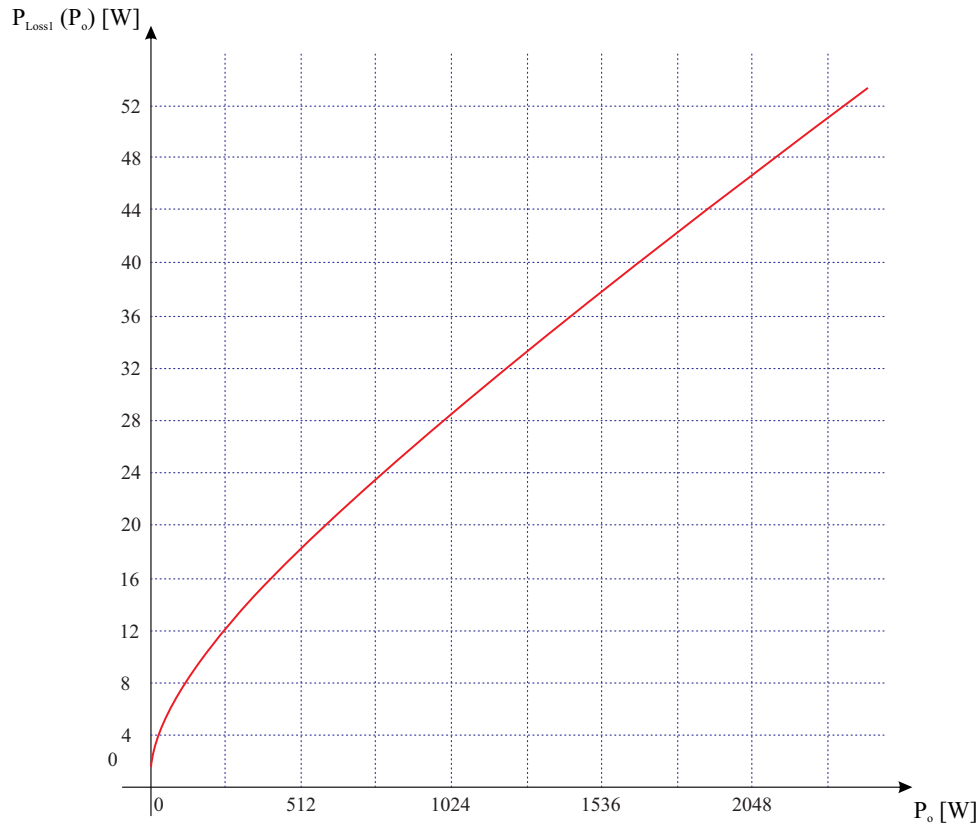
As for the conducting power losses on the switches S_{2T} and S_{2B} , they are estimated on the Equation 87.

$$P_{rDS2} = \frac{r_{DS} \cdot D_{2,nom}}{R_{o2}} \cdot P_{\Delta IL2}(D_{2,nom}) \cdot P_o = 17.33 \text{ W} \quad (87)$$

Losses on D_{2T} and D_{2B}

Equivalent as on the first stage *Buck* converter, the diodes D_{1T} and D_{1B} will have their power losses on the forward voltage across them and on their conducting resistance. The parcel on the conducting resistance is displayed at the Equation 88.

Figure 29 – Losses on the first stage *Buck* converter according to the converter's output power.



Source: Made by the author (2023) using SMATH Solver.

$$P_{RD2} = \frac{R_{F,D2} \cdot D_{2,nom}}{R_{o2}} \cdot P_{\Delta IL2}(D_{2,nom}) \cdot P_o = 3.88 \text{ W} \quad (88)$$

While the parcel on the forward voltage is estimated at the Equation 89.

$$P_{VD2} = \frac{V_{F,D2} \cdot D_{2,nom}}{V_{o1} \cdot D_{2,nom}} \cdot P_o = 16.18 \text{ W} \quad (89)$$

Losses on D_{2F}

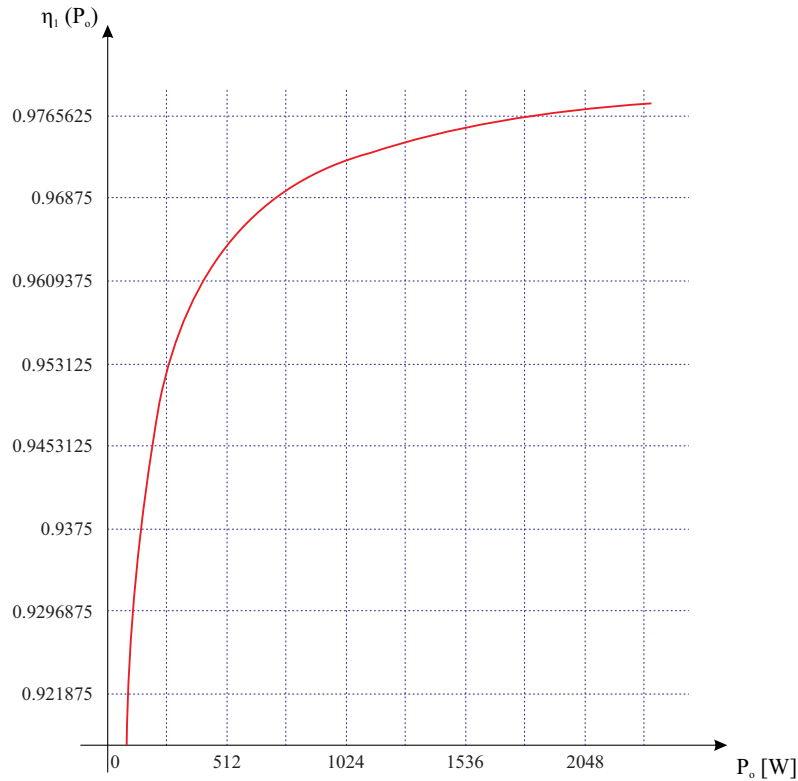
The same occurs on the freewheeling diode D_{2F} , with the conducting resistance parcel at the Equation 90.

$$P_{RF2} = \frac{R_{F,D2F} \cdot (1 - D_{2,nom})}{R_{o2}} \cdot P_{\Delta IL2}(D_{2,nom}) \cdot P_o = 14.62 \text{ W} \quad (90)$$

And the forward voltage parcel at Equation 91.

$$P_{VF2} = \frac{V_{F,D2F} \cdot (1 - D_{2,nom})}{V_{o1} \cdot D_{2,nom}} \cdot P_o = 18.97 \text{ W} \quad (91)$$

Figure 30 – Efficiency on the first stage *Buck* converter according to the converter's output power.



Source: Made by the author (2023) using SMATH Solver.

Losses on L_2

The power loss on the inductor is caused by the copper resistance and estimated on the Equation 92.

$$P_{rL2} = \frac{r_{L2}}{R_{o2}} \cdot P_{\Delta L2}(D_{2,nom}) \cdot P_o = 13.54 \text{ W} \quad (92)$$

Losses on C_2

The power losses on the capacitors are attributed to their ESR, and for C_2 , estimated by the Equation 93.

$$P_{rC2} = \frac{r_{C2} \cdot R_{o2} \cdot (1 - D_{2,nom})^2}{12 \cdot f_s^2 \cdot L_2^2} \cdot P_o = 0.19 \text{ W} \quad (93)$$

Summarizing the Power Losses on the Second Stage Buck Converter

At the Table 7 is summarized the power loss for the second stage *Buck* converter estimated previously, with P_{Loss2} being the total power loss, calculated at Equation 94, considering also the duplicated component losses.

$$P_{Loss2} = 2 \cdot (P_{sw2} + P_{rDS2} + P_{RD2} + P_{VD2}) + P_{RF2} + P_{VF2} + P_{rL2} + P_{rC2} = 122.19 \text{ W} \quad (94)$$

Table 7 – Summarized power losses on the second stage *Buck* converter.

Power Losses: Second Stage <i>Buck</i> Converter	
P_{sw2}	0.06 W
P_{rDS2}	17.33 W
$P_{total\ on\ S2}$	17.38 W
P_{RD2}	3.88 W
P_{VD2}	16.18 W
$P_{total\ on\ D2}$	20.05 W
P_{RF2}	14.62 W
P_{VF2}	18.97 W
$P_{total\ on\ D2F}$	33.59 W
P_{rL2}	13.54 W
P_{rC2}	0.19 W
P_{Loss2}	122.19 W

Source: Made by the author (2023).

With it, the estimated efficiency on the second stage *Buck* converter is 93.89% for the nominal condition operation.

In addition to the nominal condition operation point, where $P_o = 2\text{ kW}$, the Figure 31 shows the total losses on the second stage *Buck* converter according to the converter's output power.

On the second stage *Buck* converter, also, the power loss increase while the output power is increasing, but the power delivered on the converter output increases in a significantly higher rate, thus, the efficiency has a different behavior, shown at Figure 32.

5.6.4 Losses on the Whole Converter

After estimating the power losses for both first and second stage *Buck* converter, the sum of their losses will be the whole proposed converter's loss, shown at Equation 95.

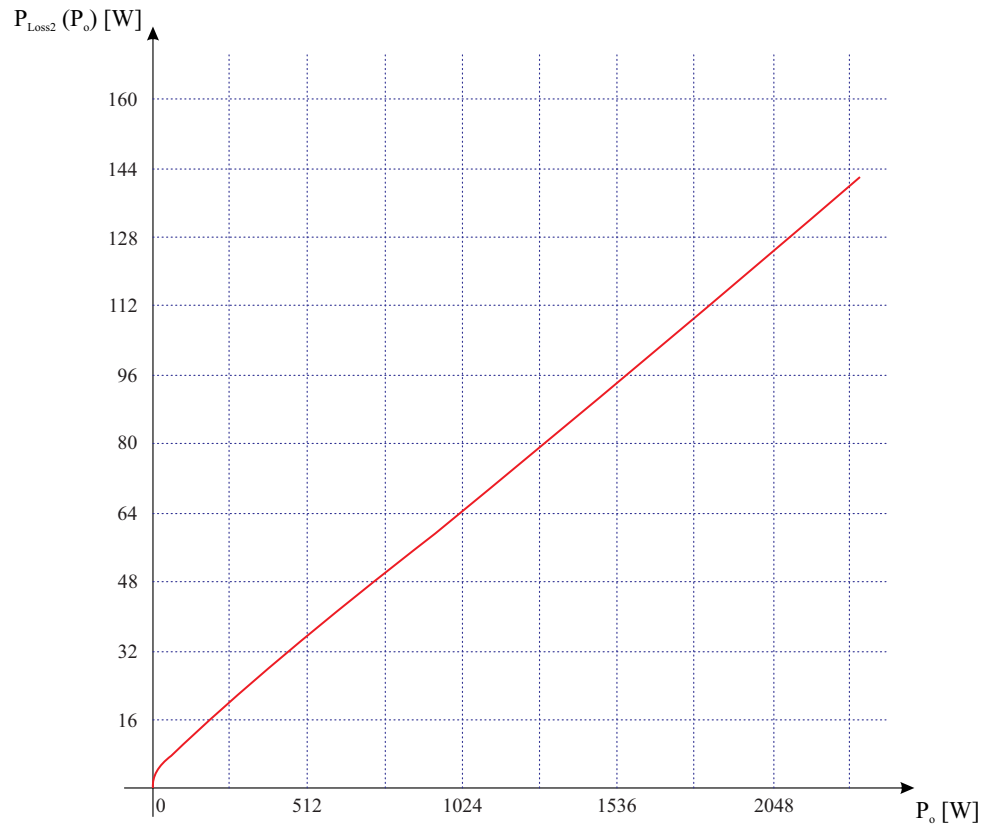
$$P_{LossT} = P_{Loss1} + P_{Loss2} = 168.02\text{ W} \quad (95)$$

So, the estimated efficiency on proposed converter is 91.60% for the nominal condition operation.

Other than the nominal condition operation point, the Figure 33 shows the total losses on the proposed converter according to the converter's output power.

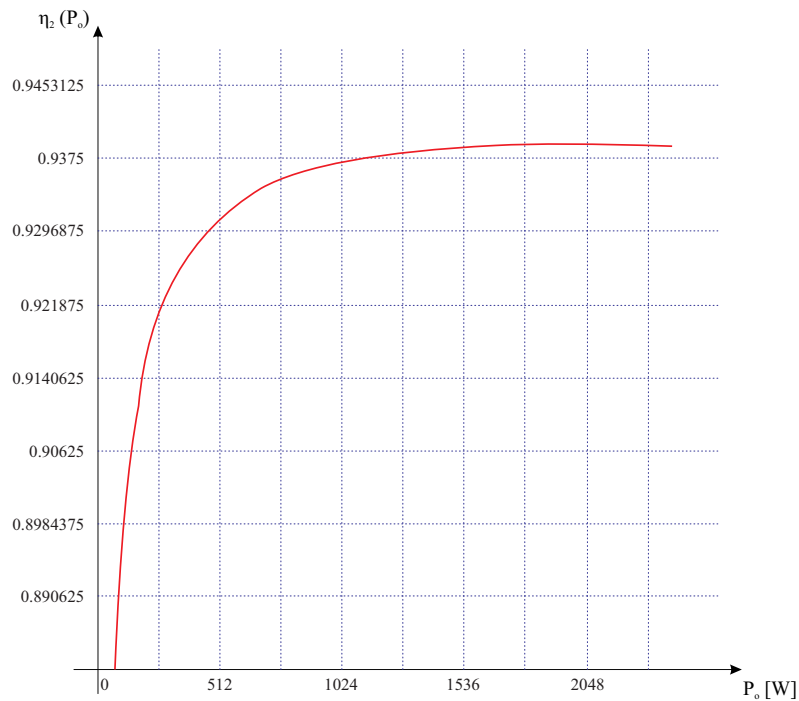
For the whole converter, the estimated efficiency chart is presented at Figure 34.

Figure 31 – Losses on the second stage *Buck* converter according to the converter's output power.



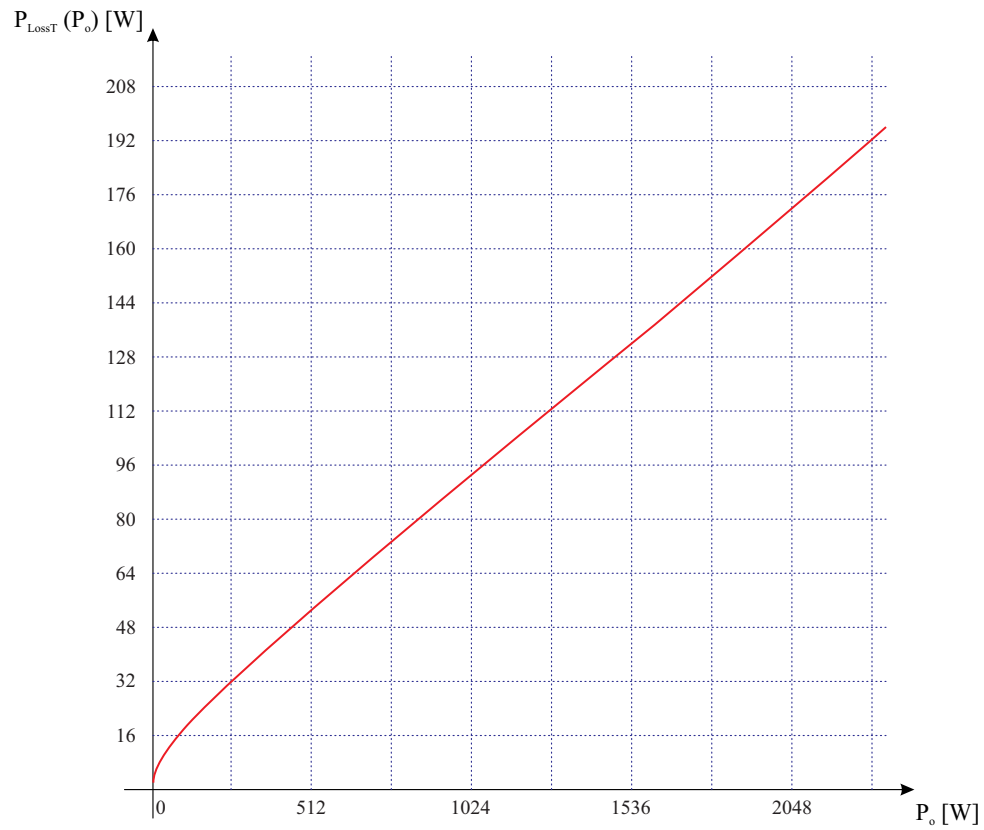
Source: Made by the author (2023) using SMATH Solver.

Figure 32 – Efficiency on the second stage *Buck* converter according to the converter's output power.



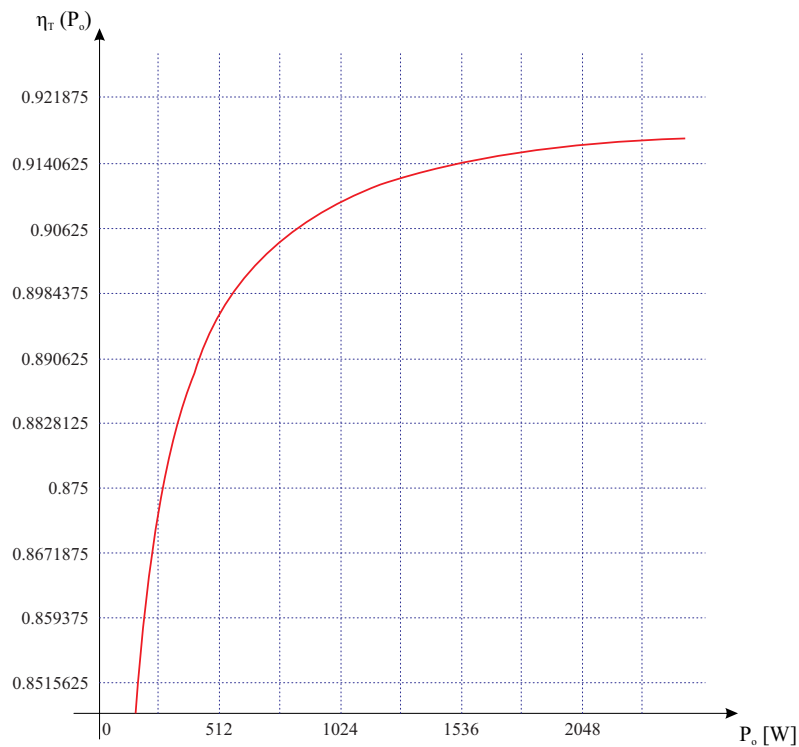
Source: Made by the author (2023) using SMATH Solver.

Figure 33 – Losses on the proposed converter according to the converter's output power.



Source: Made by the author (2023) using SMATH Solver.

Figure 34 – Efficiency on the proposed converter according to the converter's output power.



Source: Made by the author (2023) using SMATH Solver.

5.7 DISCUSSIONS ON THE HEATSINK

On the regular operation, the aforementioned power losses will turn into heat on the components. Some of them, as the inductors have a good dissipation area and can keep themselves on a acceptable temperature, a fan can be used otherwise. And the capacitors have not a significant power loss to get high temperatures.

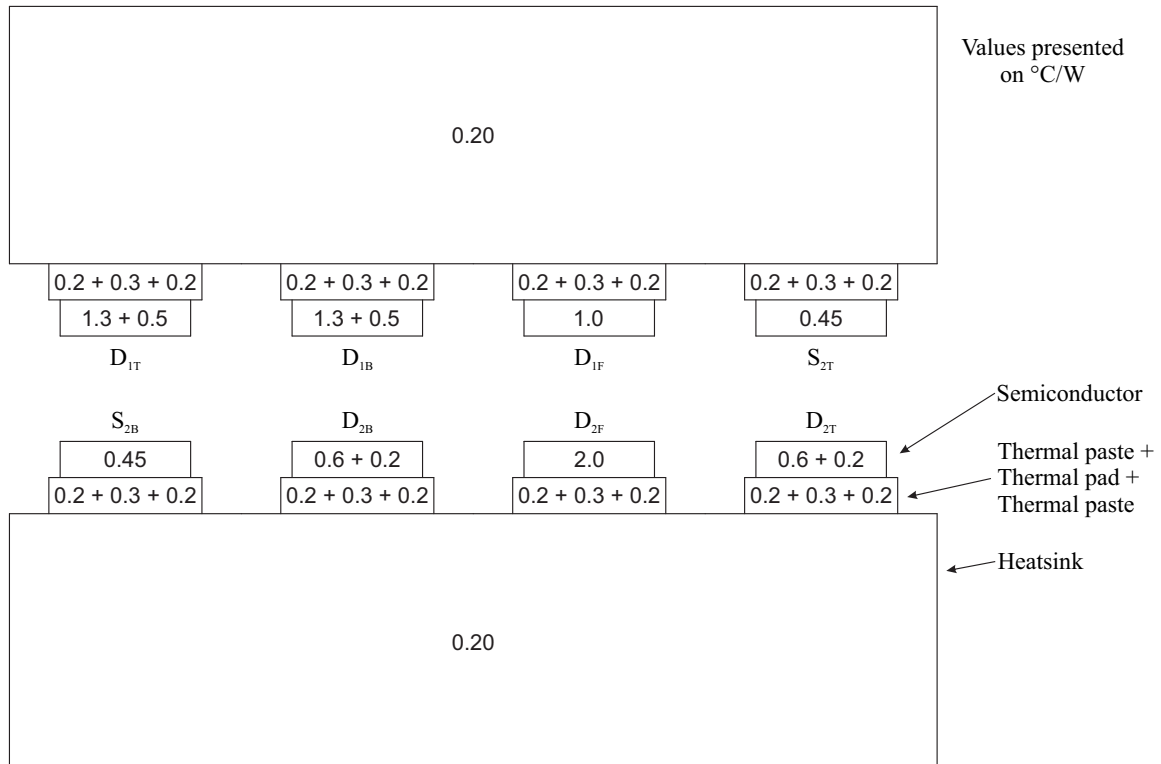
But, on the other hand, the semiconductor components dispose from a small dissipation area, so they usually need a heatsink to dissipate the heat from their power losses. This section brings a discussion on the selected heatsinks.

Two aluminium heatsinks with 104mm x 58mm x 53.50mm were selected to be the main heatsinks on the converter, but they are manufactured to accommodate four semiconductors, so, two of them need another option. This heatsink model is rated with a thermal resistance of $0.20^{\circ}\text{C}/\text{W}$ at the examined situation, with a 3.40m/s wind speed fan.

As verified on the previous section, the switches S_{1T} and S_{1B} are estimated with the smaller power loss among the semiconductors, thus, they can operate with a smaller heatsink, which was selected for them, each one with their own independent heatsink.

The disposition of the semiconductors on both bigger heatsinks is displayed at Figure 35. Internal to the blocks are displayed their thermal resistance. The block close to the semiconductor's name is its representation, followed by the next block, which is a set with switch-side thermal paste + ceramic thermal pad + heatsink-side thermal paste, and then comes the heatsink.

Figure 35 – Disposition of the semiconductors on the heatsink with thermal resistances.



Source: Made by the author (2023).

Table 8 – Semiconductors thermal resistances according to their datasheet.

	R_{jc}	R_{cs}	R_{ja}
C3M0032120K	0.45 °C/W		40 °C/W
VS-20ETS12	1.30 °C/W	0.50 °C/W	
VS-40EPS12	0.60 °C/W	0.20 °C/W	40 °C/W
MBR40250	2.00 °C/W		60 °C/W
BYT30P-1000	1.00 °C/W		

Source: Made by the author (2023).

The Table 8 shows the thermal resistances on each semiconductor according to their datasheet, which are used for the model of the Figure 35 and later for the thermal simulation. The values for R_{cs} and R_{ja} are missing on some datasheets, so they are not took into account because of their low significance on the final temperature by the reason they have lower thermal resistances.

Another aspect of the model presented on the Figure 35, is that each group formed by a semiconductor + ceramic thermal pad + heatsink will form a capacitor, thus they can affect the circulating touch current through the converter, so the semiconductor disposition on each heatsink is designed to have the smaller possible impact on the capacitance.

A estimation of the capacitance is made considering the greater contact area between the semiconductors, which is at the switches C3M0032120K. The Equation 96 is used to estimate the capacitance for simulation purposes, where $\epsilon_0 \approx 8.85 \text{ pF/m}$ is the Vacuum permittivity, $\epsilon_r = 5$ is the relative permittivity of the ceramic thermal pad considered, $A = 238 \text{ mm}^2$ is the switch approximated contact area and $d = 1 \text{ mm}$ is the thermal pad thickness.

$$C = \frac{\epsilon_r \cdot \epsilon_0 \cdot A}{d} = 21.10 \text{ pF} \quad (96)$$

A wider thickness would result in a lower capacitance, but, in counterpart, it brings a higher thermal resistance, dissipating less heat. Thus, the ideal scenario is with a separated heatsink, with no grounding, for every semiconductor.

6 SIMULATION RESULTS

With the proposed converter designed and discrete components selected, this chapter addresses the simulation and presents its results.

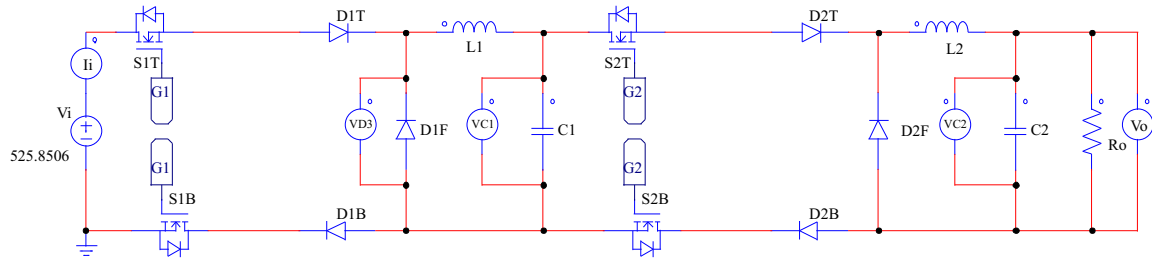
6.1 IDEAL SIMULATION

The project proceeds with a ideal component simulation using the software Altair® PSIM™, which has one of its focus on power electronics.

6.1.1 Critical Condition

The first simulation aims to validate the calculated values for the inductors and capacitors on the Design Chapter, section 5.1 and 5.2. The minimal values are calculated for the converter to operate at CCM with 200 W or more with the minimum duty cycle on each converter stage, and the maximum input voltage is applied on this situation. The parameters used on this simulation are displayed at Table 9 and simulated with the circuit on the Figure 36.

Figure 36 – Critical condition simulation circuit.



Source: Made by the author (2023) on PSIM.

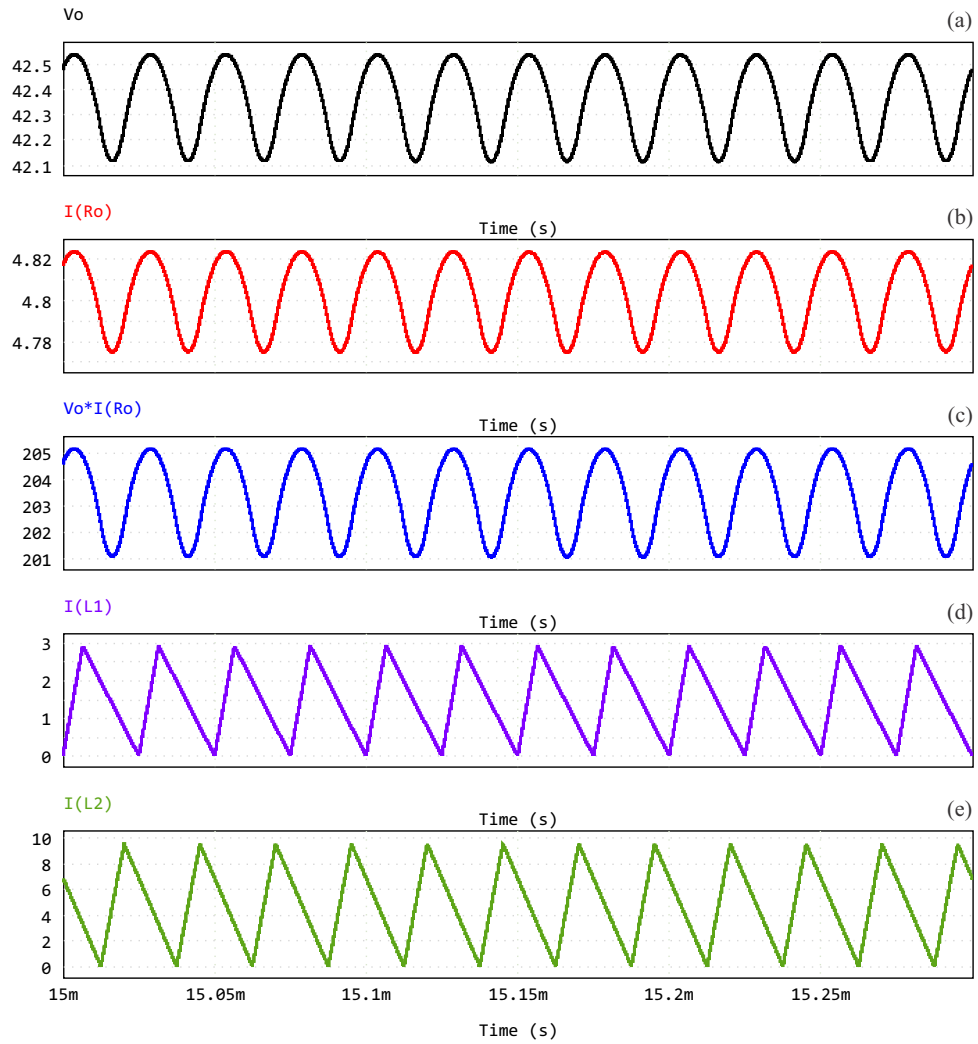
The simulation results are shown in the Figure 37 and the average values on the Table 10. As can be seen in both inductor current waveforms, they are operating in Critical Conduction Mode (CRM), as expected by the calculation of the minimum values of the inductance and capacitance. With higher values the converter should go to CCM and with lower values on Discontinuous Conduction Mode (DCM). This behavior shows that the calculations are correct.

Table 9 – Parameters considered on the critical condition simulation.

L_1	879.44 μ H
C_1	6.57 μ F
D_1	0.26
V_i	525.85 V
L_2	77.57 μ H
C_2	69.84 μ F
D_2	0.31

Source: Made by the author (2023).

Figure 37 – Critical condition simulation results: (a) Second-stage *Buck* converter output voltage, V_o ; (b) Load current, $I(R_o)$; (c) Converter output power, $V_o \cdot I(R_o)$; (d) Inductor L_1 current, $I(L_1)$; (e) Inductor L_2 current, $I(L_2)$.



Source: Made by the author (2023) on PSIM.

Table 10 – Calculated and simulated average values for critical condition mode.

	Calculated	Simulated
$\overline{V_o}$	42 V	42.36 V
$\overline{I_o}$	4.76 A	4.80 A
$\overline{P_o}$	200 W	203.41 W

Source: Made by the author (2023).

6.1.2 Nominal Condition

The same circuit on the Figure 36 is used for the nominal condition simulation, but now the inductors and capacitors have the value of the selected component on section 5.5, as displayed on the Table 11. The resulting waveforms can be seen in the Figure 38.

Table 11 – Parameters considered on the ideal nominal simulation.

L_1	998 μ H
C_1	6.60 μ F
D_1	0.34
V_i	400 V
L_2	170.50 μ H
C_2	1640 μ F
D_2	0.40

Source: Made by the author (2023).

As the capacitance, specially on the second converter stage, has increased significantly, the settling time also increased, thus, a small oscillation can be seen on a lower frequency than the switching frequency. The observed average values on the simulation reached close enough to the calculated values, as can also be seen in the Table 12. These values reveal a closed loop control would be sufficient to regulate the output voltage to a appropriate value. Another noticeable aspect is the CCM operation on both inductors, L_1 and L_2 .

Table 12 – Calculated and simulated average values for nominal condition.

	Calculated	Simulated
$\overline{V_o}$	54.40 V	54.70 V
$\overline{I_o}$	36.76 A	36.97 A
$\overline{P_o}$	2 kW	2.02 kW

Source: Made by the author (2023).

The values for the current ripple on the inductors L_1 and L_2 are depicted at the Figure 13, as can be seen the calculated and simulated values are very close.

Table 13 – Calculated and simulated current ripple values on inductors for nominal condition.

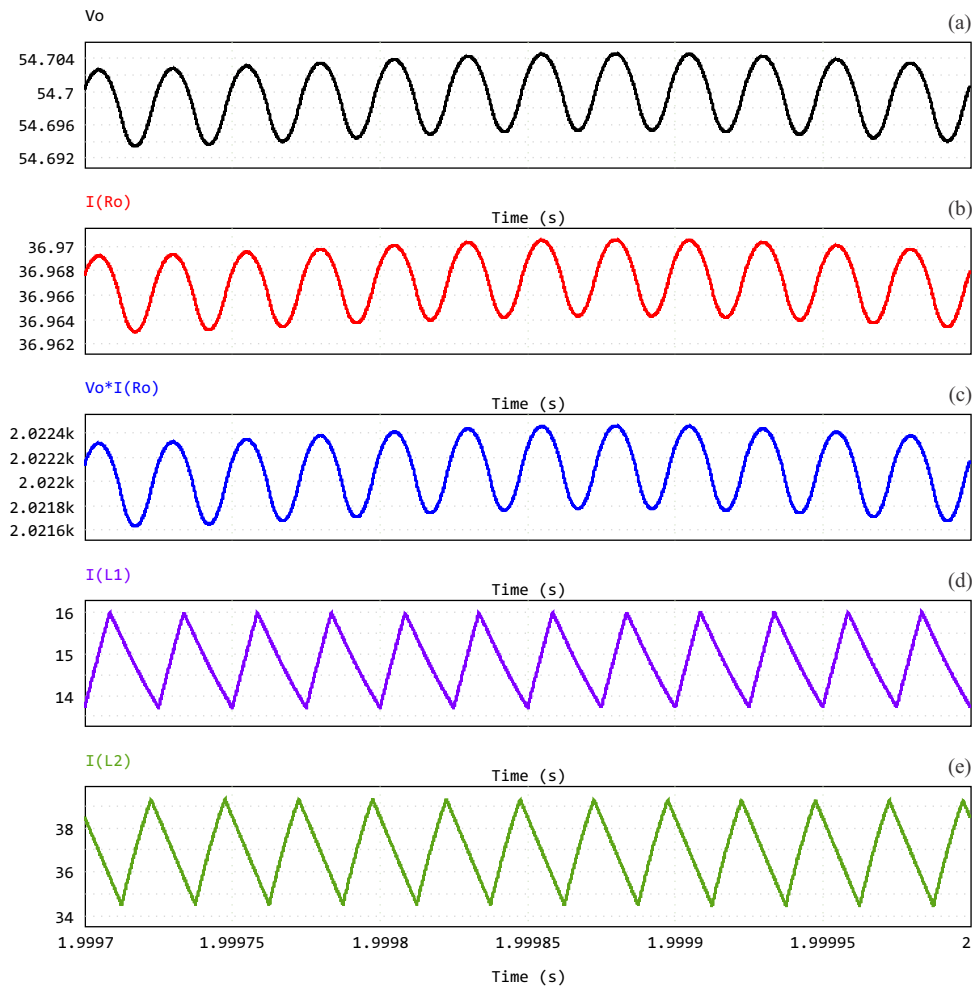
	Calculated	Simulated
$\overline{\Delta I_{L1}}$	2.29 A	2.25 A
$\overline{\Delta I_{L2}}$	4.81 A	4.79 A

Source: Made by the author (2023).

On the Figure 39 it is possible to verify the current on each inductor alongside with its voltage. The inductor current increase when the voltage across it is positive and decrease when negative. In addition to the switching steps, the voltage across the inductors also varies with the charging and discharging of capacitors C_1 and C_2 .

The Figure 40 displays the voltage on both top switches, S_{1T} and S_{2T} , along with their current. The bottom switches S_{1B} and S_{2B} will conduct at the same time with S_{1T} and S_{2T} ,

Figure 38 – Nominal condition simulation results: (a) Second-stage *Buck* converter output voltage, V_o ; (b) Load current, $I(R_o)$; (c) Converter output power, $V_o \cdot I(R_o)$; (d) Inductor L_1 current, $I(L_1)$; (e) Inductor L_2 current, $I(L_2)$.



Source: Made by the author (2023) on PSIM.

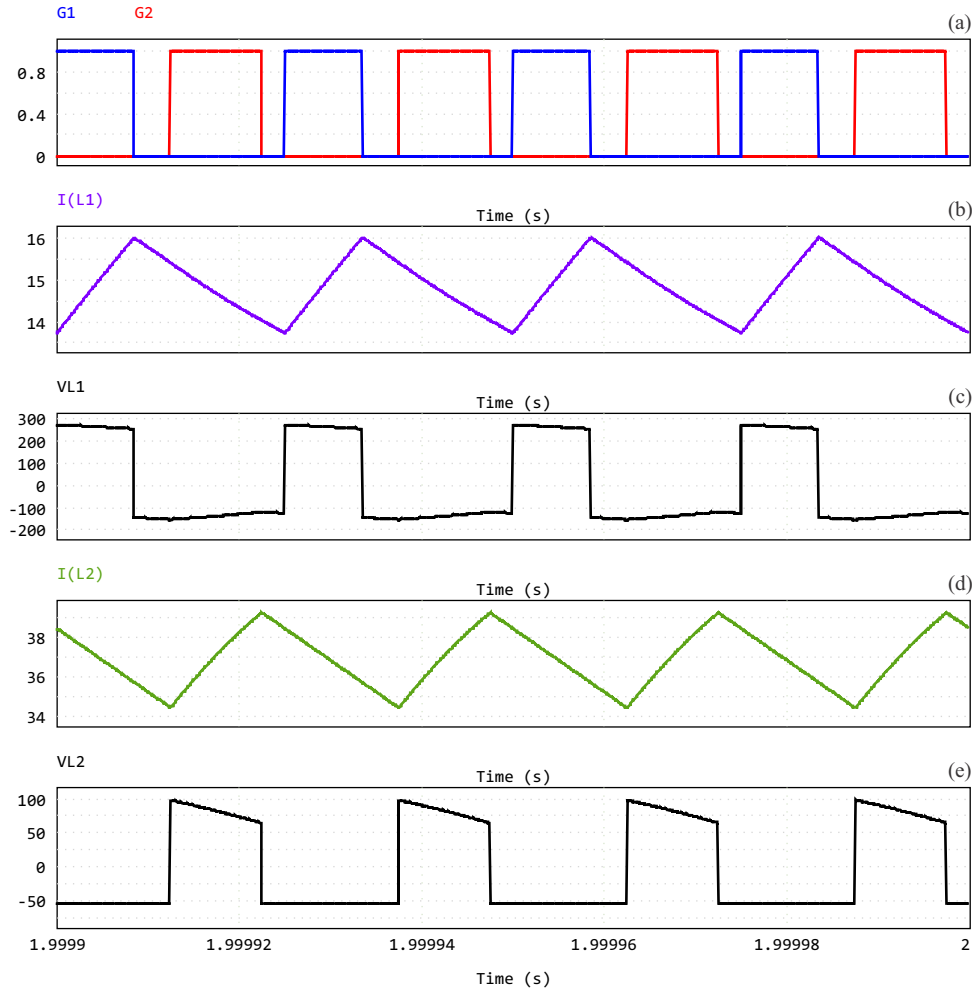
respectively, but the switches on the first converter stage are not to be conducting when the switches on the second stage are, as it is demonstrated on these waveforms.

Still on the Figure 40, one can see the waveform for the voltage on S_{2T} rising when it is closed. As this voltage is the half of the voltage on C_1 , it indicates a higher voltage ripple at C_1 , which was not considered in the previous analysis but is known to exist because of the pulsed current delivered to the second-stage *Buck* converter.

6.1.3 Touch Current

For the touch current analysis with ideal component, the circuit on the Figure 41 is simulated. Ideally the switches do not have a capacitance between drain and source, therefore an external one, of 121 pF, is added so the touch current can circulate through them. Although it is an unwanted feature of the switch, it exists, so, for analyzing with an ideal component, the external capacitance is needed. Furthermore, some PSIM measuring tools were removed from

Figure 39 – Nominal condition simulation results: (a) Signal on switches gates, G1 for S_{1T} and S_{1B} , and G2 for S_{2T} and S_{2B} ; (b) Current on the inductor L_1 , $I(L1)$; (c) Voltage on the inductor L_1 , VL1; (d) Current on the inductor L_2 , $I(L2)$; (e) Voltage on the inductor L_2 , VL2.



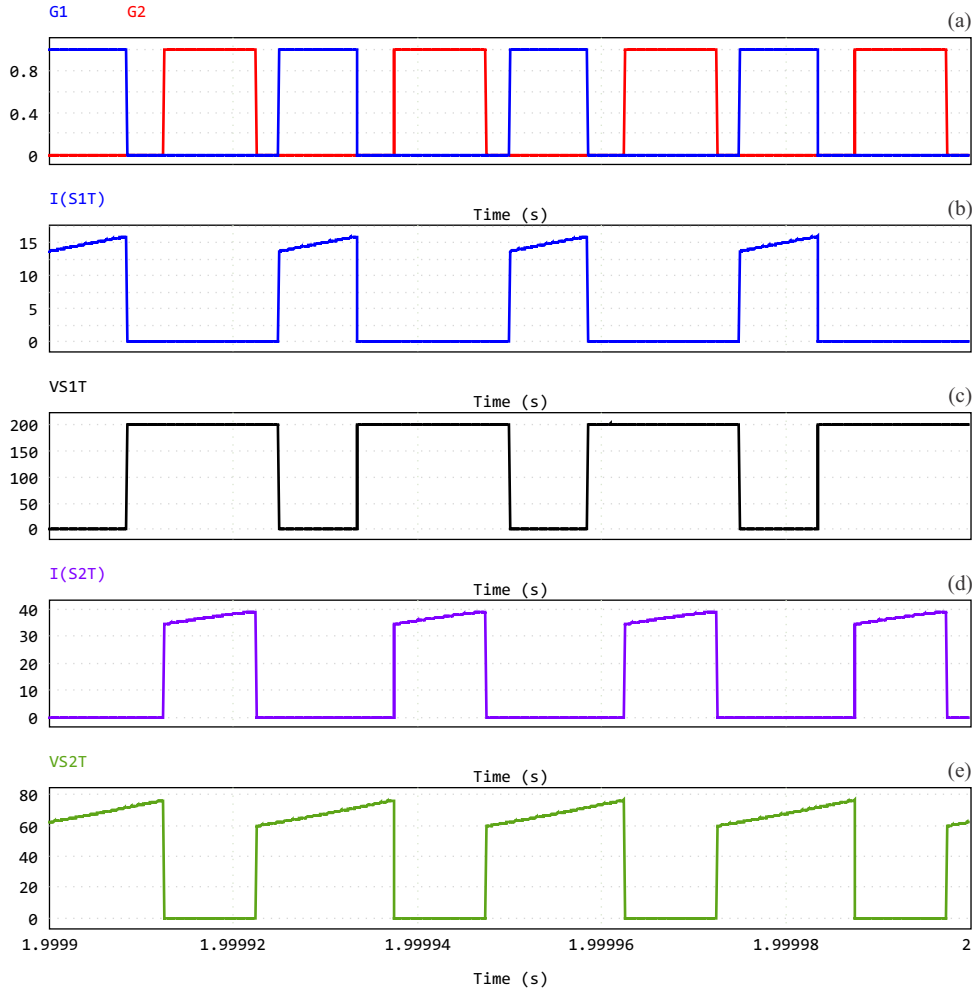
Source: Made by the author (2023) on PSIM.

the figure to make it cleaner and easier to be read.

The touch current circulates by current peaks on switches drain-source capacitance. These peaks are impulse-like current waveform, with high amplitude by a short period, in this case from 10^{-8} s to 10^{-7} s scale. Thus, for a better resolution, a fixed step of $1 \cdot 10^{-11}$ s is used, turning impracticable a long simulation, in fact, the converter settling time would require a simulation of hours and a plenty of space in the computer hard drive, not to mention that it would be costly to process so much data to compound the waveform. Hence, the simulation time is reduced to a sufficient amount, and initial voltage values are set on capacitors and initial current on inductors, it allowed to have adequate results.

On the Figure 42 is possible to see the peaks on the touch current waveform and also on the switch capacitances, on a higher amplitude scale. It happens because most part of the charging and discharging current on the capacitances would flow on the switch itself or on the

Figure 40 – Nominal condition simulation result: (a) Signal on switches gates, G1 for S_{1T} and S_{1B} , and G2 for S_{2T} and S_{2B} ; (b) Current on S_{1T} , $I(S_{1T})$; (c) Voltage on S_{1T} , VS_{1T} ; (d) Current on S_{2T} , $I(S_{2T})$; (e) Voltage on S_{2T} , VS_{2T} .



Source: Made by the author (2023) on PSIM.

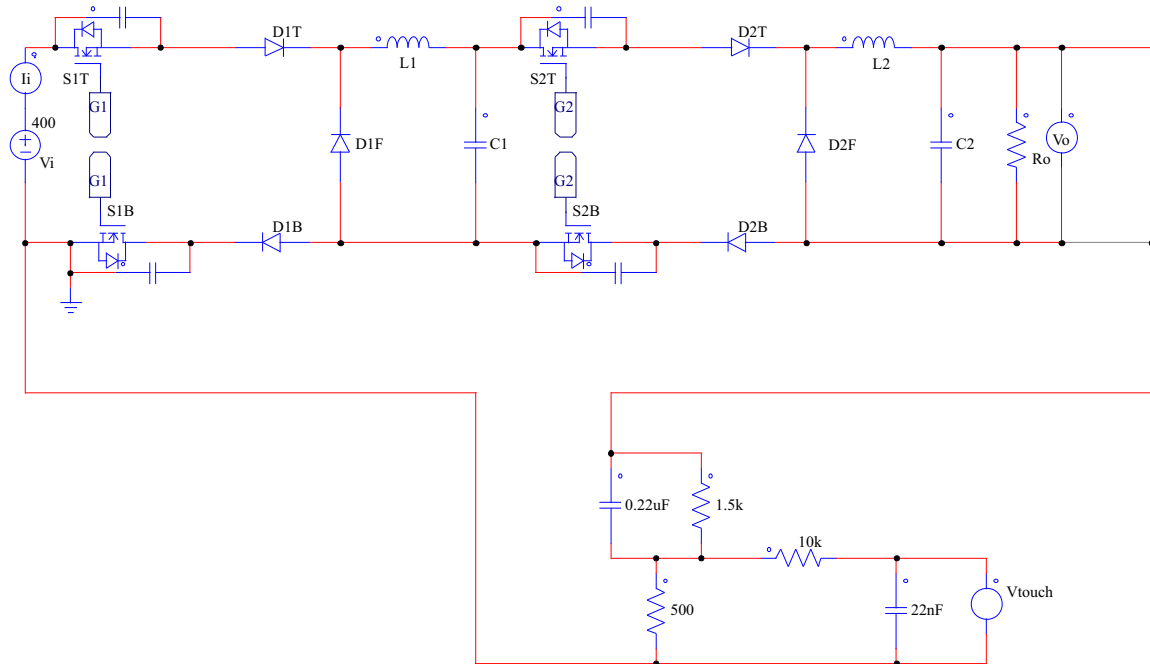
circuit by a DM current, while a small parcel circulate as a CM current. The voltage on the output of the standard human body impedance simulation network represents the measured touch current by the Equation 97 and have an average value of 1.66 mA complying with the IEC 60950-1 standard, which requires a current below 3.50 mA.

$$I_{touch} = \frac{V_{touch}}{500} \quad (97)$$

On the Figure 42 it is possible to check the current peaks on $I(S_{1T}C_{ds})$, $I(S_{2T}C_{ds})$, $I(S_{1B}C_{ds})$ and $I(S_{2B}C_{ds})$ have a high amplitude negative value, which are the I_d presented on the Figure 23 and 24 as the current flow on the switch itself discharging the switch capacitance. This current is limited only by the switch's $R_{DS(on)}$ rated on 32 mΩ typically on the used switch. As the amplitude is so high, it is barely possible to see the other current components.

A zoom is then done on the Figure 43 where the current peaks for charging the switch's drain-source capacitance can be seen. They are presented as the magenta I_{DM} on the Figure 23

Figure 41 – Touch current simulation circuit with ideal components.

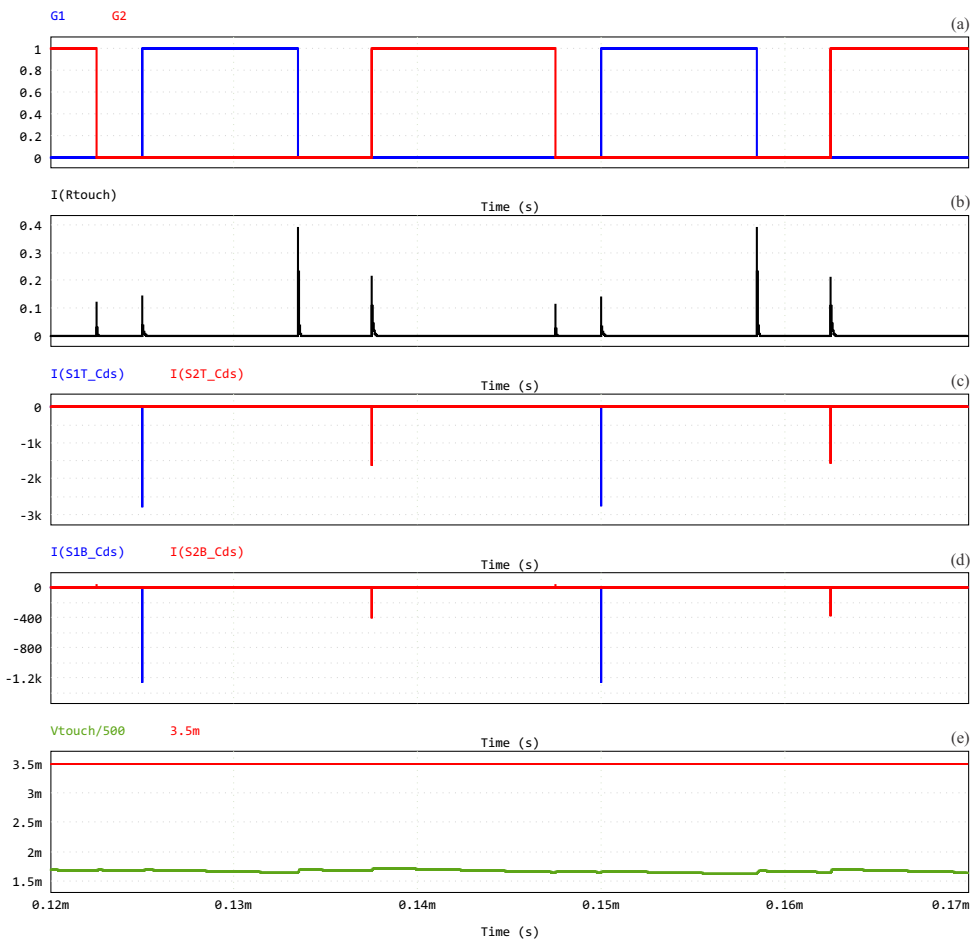


Source: Made by the author (2023) on PSIM.

and 24. Although the zoom, the touch current still can not be observed, as the simulated DM current peak for charging the switch's capacitance is in a order of 40 A and the touch current in a order of 0.40 A.

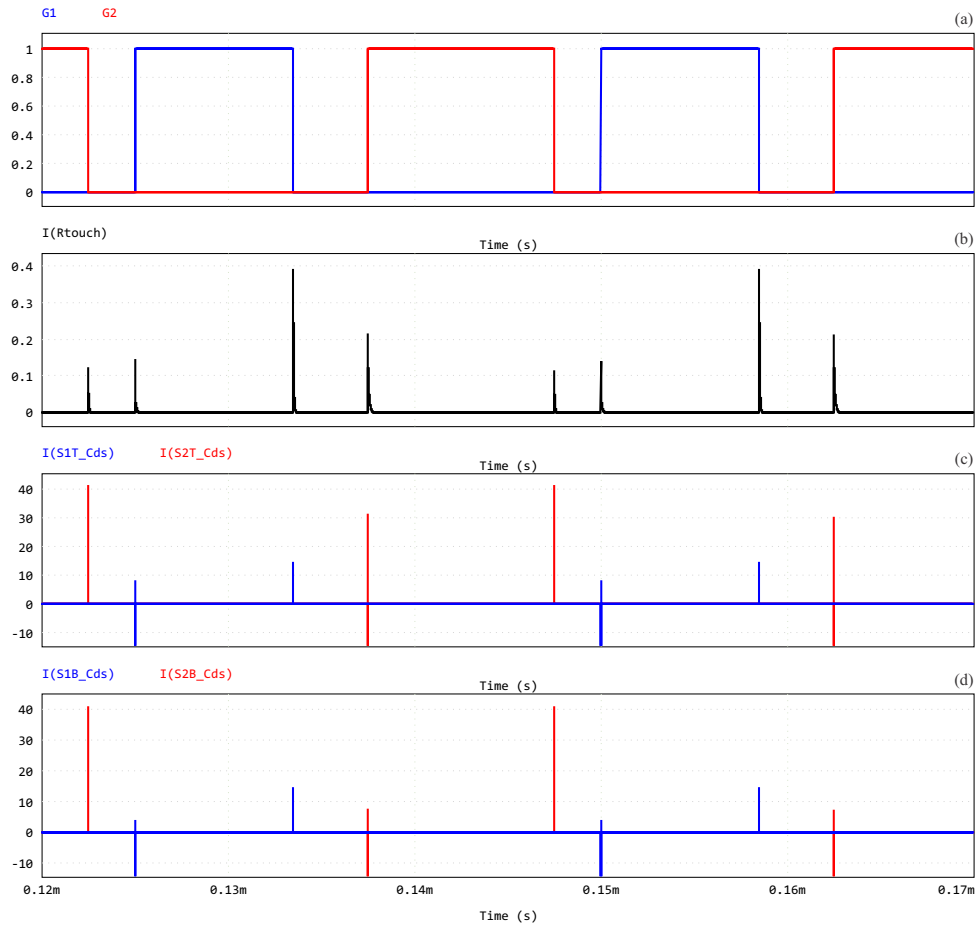
To see the touch current waveform on the switches capacitances, even more zoom is applied to its current waveform on the Figure 44. This way it is possible to check the matching current peaks on both human body impedance simulation network and switches capacitances. It is visible also the aspect of the peaks matching every increasing on the switches S_{1T} and S_{2T} voltage. Besides of that, the diodes D_{1B} and D_{2B} would block the voltage compensating the touch current loop.

Figure 42 – Touch current simulation result with ideal components and negative rail connected:
 (a) Signal on switches gates, G1 for S_{1T} and S_{1B} , and G2 for S_{2T} and S_{2B} ; (b) Touch current measured over the human body impedance simulation network, $I(R_{touch})$; (c) Current on the switches S_{1T} and S_{2T} drain-source capacitance, $I(S_{1T_Cds})$ and $I(S_{2T_Cds})$; (d) Current on the switches S_{1B} and S_{2B} drain-source capacitance, $I(S_{1B_Cds})$ and $I(S_{2B_Cds})$; (e) Touch current measured on the human body impedance simulation network output divided by 500, $V_{touch}/500$, and the IEC 60950-1 standard limit, $3.5m$.



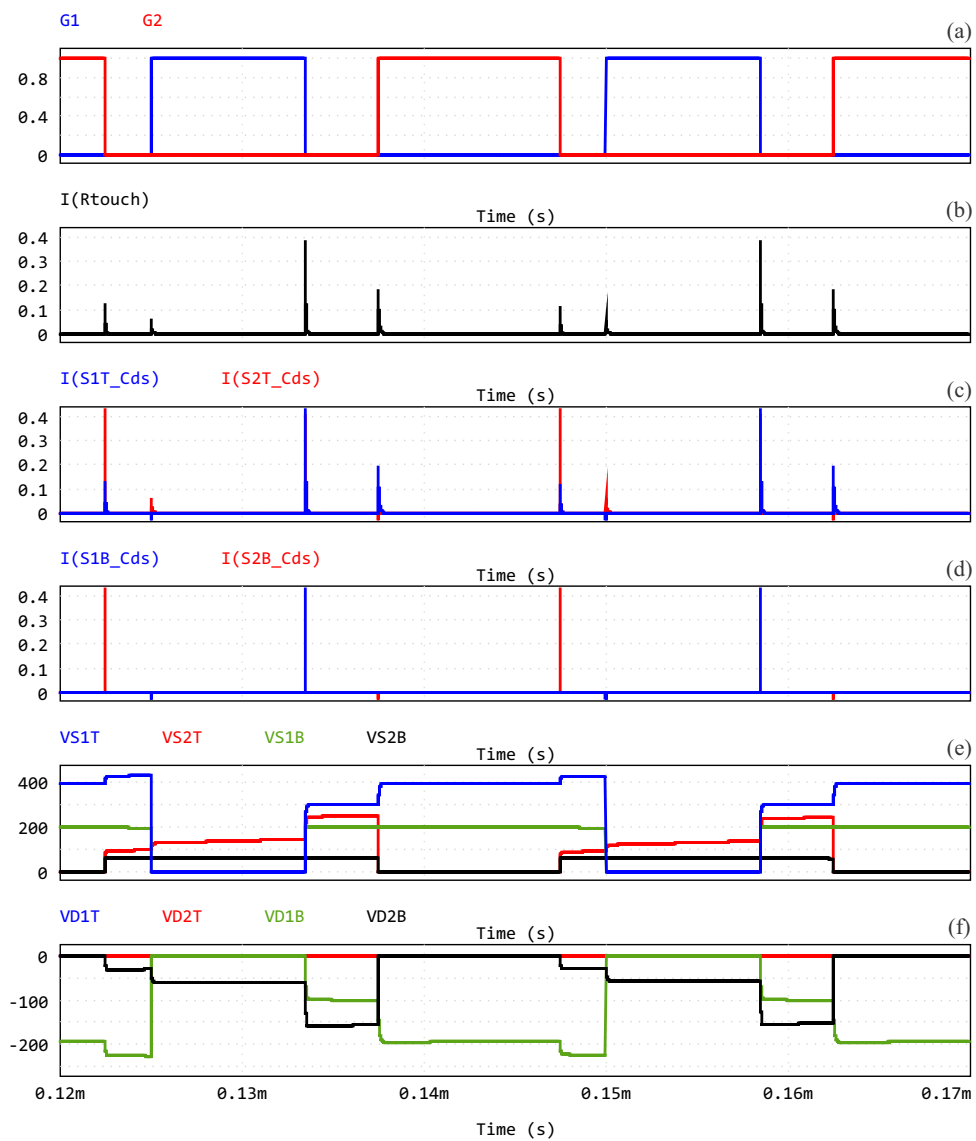
Source: Made by the author (2023) on PSIM.

Figure 43 – Touch current simulation result with ideal components and negative rail connected, zoomed on the I_{DM} : (a) Signal on switches gates, G1 for S_{1T} and S_{1B} , and G2 for S_{2T} and S_{2B} ; (b) Touch current measured over the human body impedance simulation network, $I(R_{touch})$; (c) Zoomed current on the switches S_{1T} and S_{2T} drain-source capacitance, $I(S_{1T_Cds})$ and $I(S_{2T_Cds})$; (d) Zoomed current on the switches S_{1B} and S_{2B} drain-source capacitance, $I(S_{1B_Cds})$ and $I(S_{2B_Cds})$.



Source: Made by the author (2023) on PSIM.

Figure 44 – Touch current simulation result with ideal components and negative rail connected, zoomed on the touch current on the switch's capacitance: (a) Signal on switches gates, G1 for S_{1T} and S_{1B} , and G2 for S_{2T} and S_{2B} ; (b) Touch current measured over the human body impedance simulation network, $I(R_{touch})$; (c) Zoomed current on the switches S_{1T} and S_{2T} drain-source capacitance, $I(S_{1T_Cds})$ and $I(S_{2T_Cds})$; (d) Zoomed current on the switches S_{1B} and S_{2B} drain-source capacitance, $I(S_{1B_Cds})$ and $I(S_{2B_Cds})$; (e) Voltage on the switches S_{1T} , S_{2T} , S_{1B} and S_{2B} , VS_{1T} , VS_{2T} , VS_{1B} and VS_{2B} ; (f) Voltage on the diodes D_{1T} , D_{2T} , D_{1B} and D_{2B} , VD_{1T} , VD_{2T} , VD_{1B} and VD_{2B} .



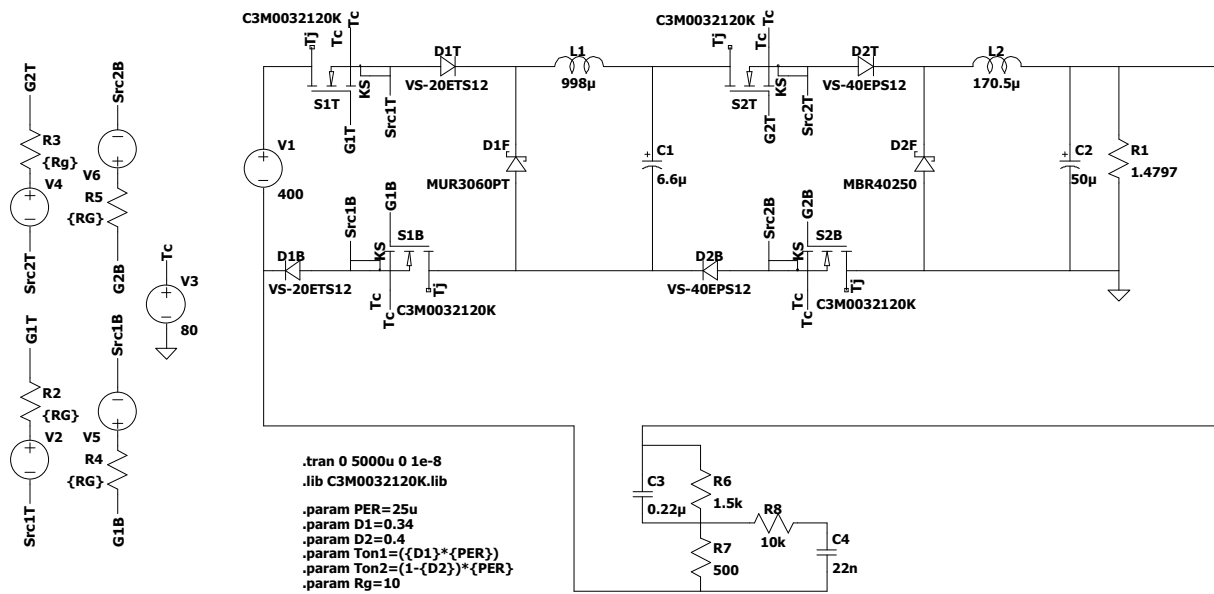
Source: Made by the author (2023) on PSIM.

6.2 NON-IDEAL SIMULATION

For the non-ideal simulation, the Analog Devices LTspice® software is used. As a SPICE simulator it brings non-idealities to the components.

In this simulator, a model of the real component can be get from the internet and included on the simulation bringing a series of aspects of its real counterpart. So a model for the components selected on the Design Chapter were downloaded from the manufacturer site on the internet and included on the simulation. For the capacitor and inductor a series resistance is included to a generic component to make it closer to the real component.

Figure 45 – Nominal condition simulation circuit on LTspice.



Source: Made by the author (2023) on LTspice.

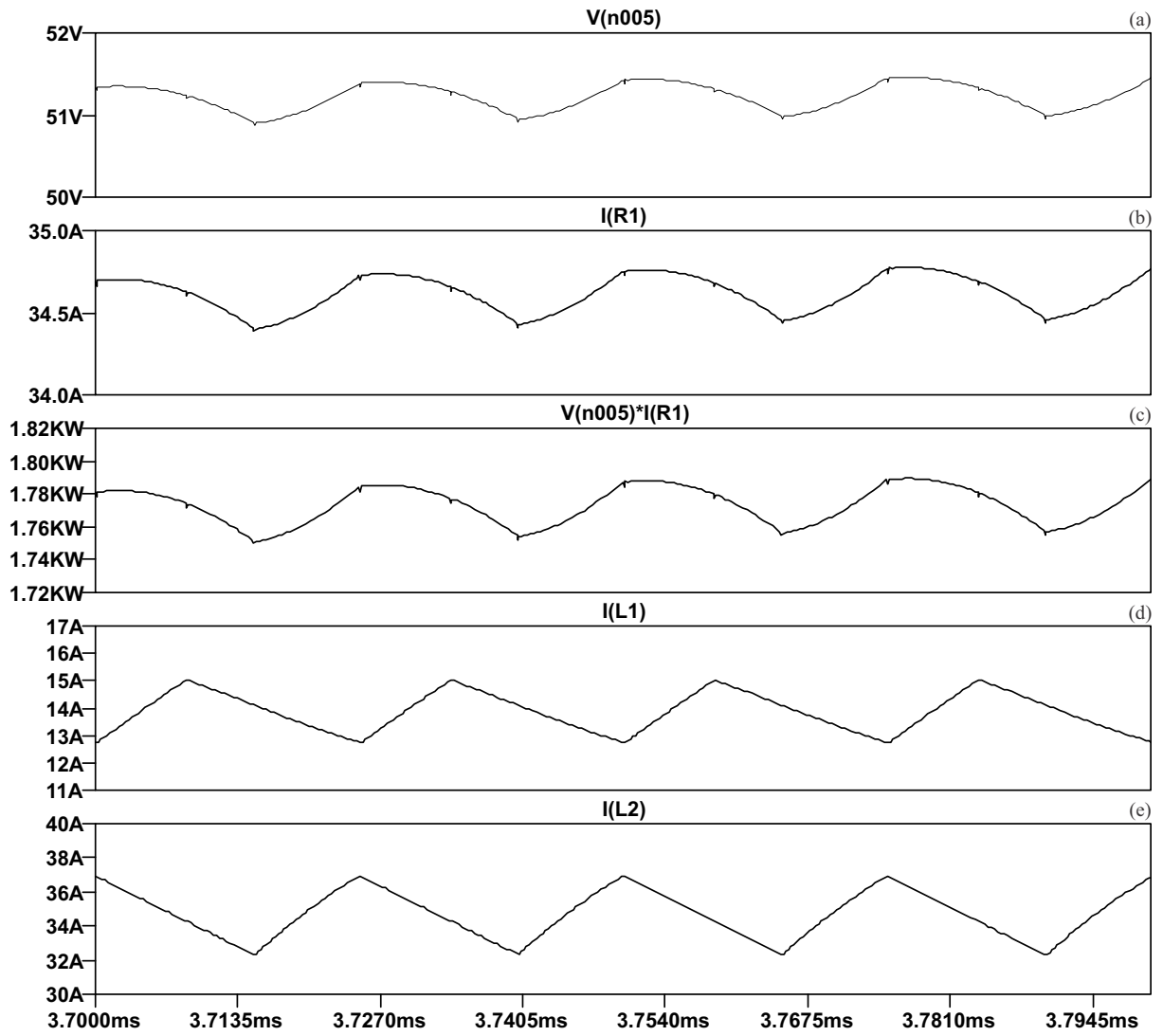
On the Figure 46, the simulation results are presented. The voltage and current a little below the expected shows that the converter would have lower efficiency than the considered 99% for the calculation. As the converter is in a open-loop control, with fixed duty cycles, higher losses means lower voltage and current, thus, lower power on the output. A closed-loop control could be implemented to solve this problem.

The Figure 46 also shows the CCM operation for both inductors L_1 and L_2 .

At the Figure 47, it is shown the results on the touch current for the non-ideal simulation. The average value could be observed being below the 3.50mA required by the standard. Here, also, the Equation 97 is used to convert the measured voltage into touch current.

(c) Touch current measured on the human body impedance simulation network output; By comparing the Figure 48 with the Figure 48 it is possible to see the difference on the touch current going from below 3.50mA when the switches S_{1T} and S_{1B} are switching complementarily with S_{2T} and S_{2B} , providing the SGI feature, to higher than 19mA when switches S_{1T} and S_{1B} are

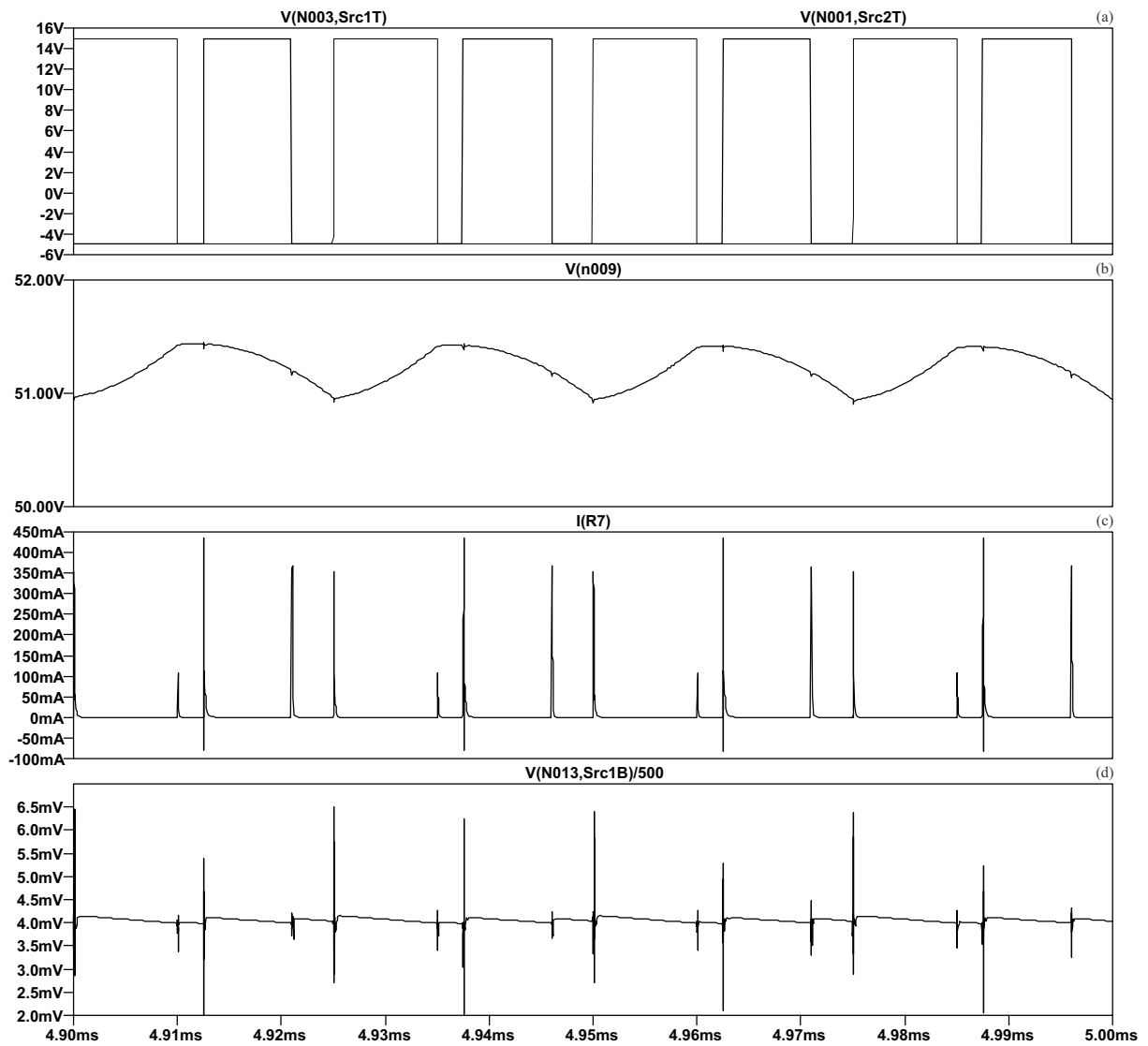
Figure 46 – Nominal condition simulation result on LTspice: (a) Second-stage *Buck* converter output voltage, $V(n005)$; (b) Load current, $I(R1)$; (c) Converter output power, $V(n005)*I(R1)$; (d) Inductor L_1 current, $I(L1)$; (e) Inductor L_2 current, $I(L2)$.



Source: Made by the author (2023) on LTspice.

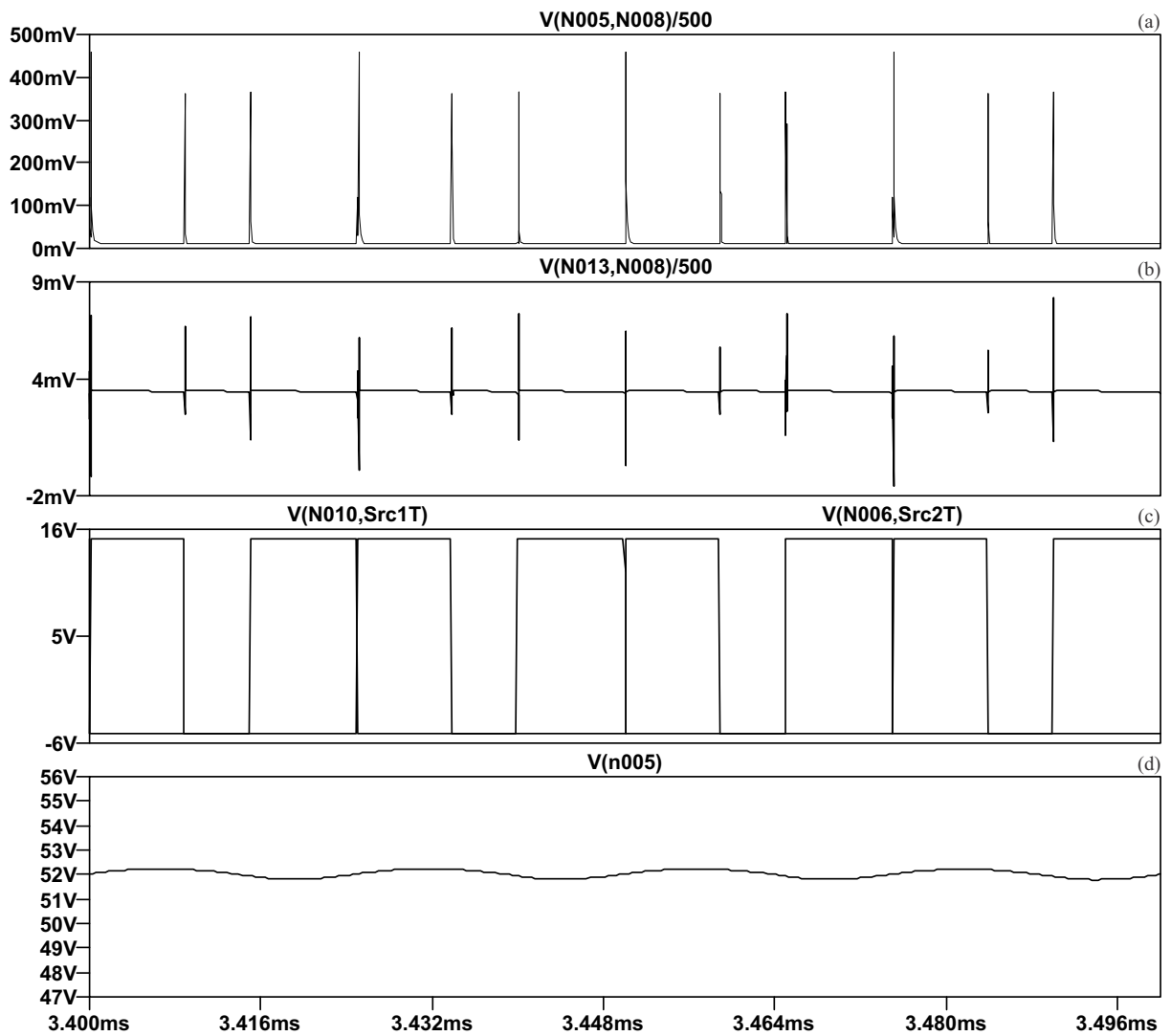
switching at the same time with S_{2T} and S_{2B} . At this condition the input circuit is put in contact with the output circuit, thus the thouch current increase and SGI feature is not present.

Figure 47 – Touch current simulation result on LTspice: (a) Signal on switches gates, $V(N003,Src1T)$ for S_{1T} and S_{1B} , and $V(N001,Src2T)$ for S_{2T} and S_{2B} ; (b) Second-stage *Buck* converter output voltage, $V(n009)$; (c) Touch current measured over the human body impedance simulation network, $I(R7)$; (d) Touch current measured on the human body impedance simulation network output divided by 500, $V(N013,Src1B)/500$.



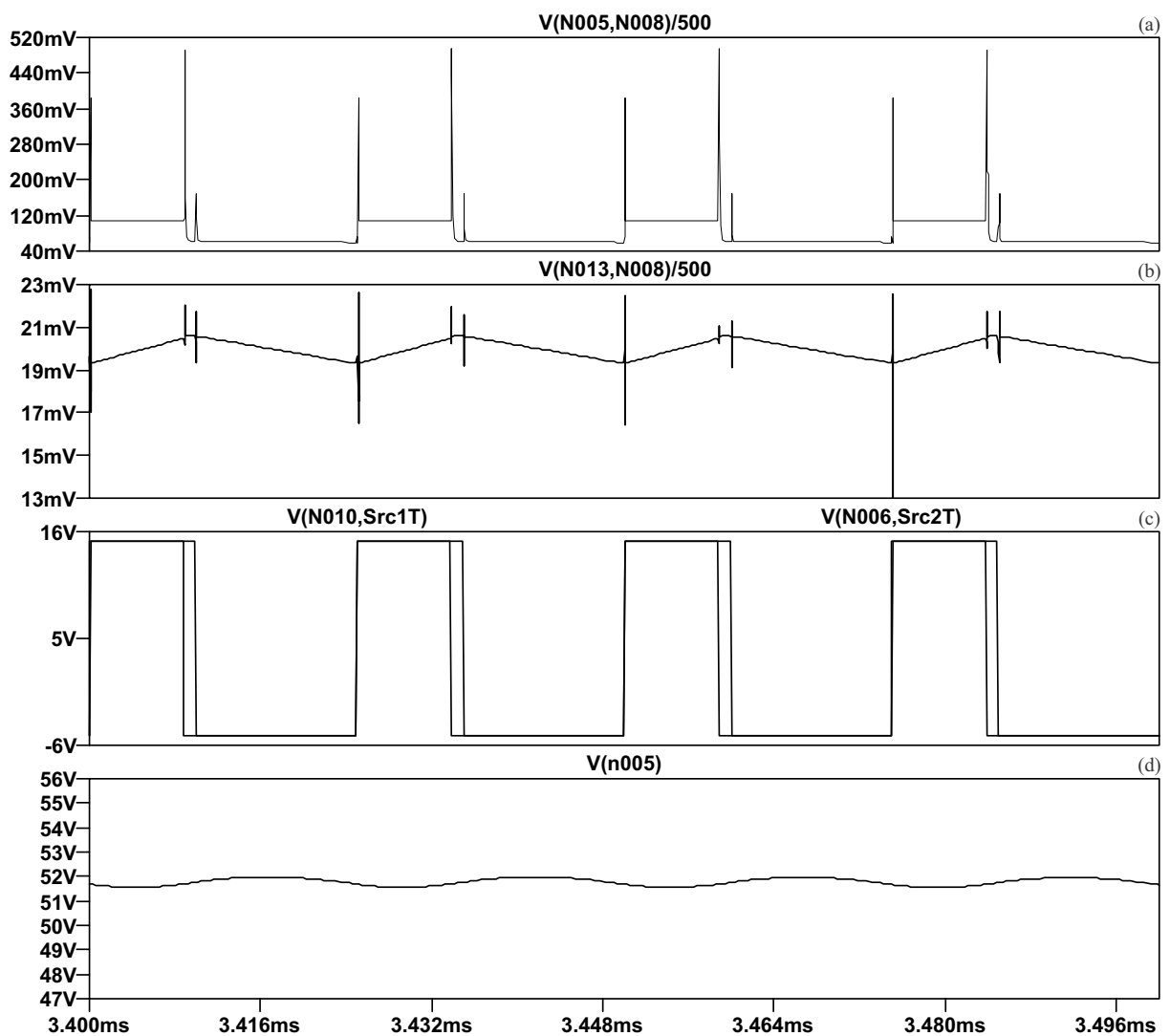
Source: Made by the author (2023) on LTspice.

Figure 48 – Touch current comparison on LTspice. Switches S_{1T} and S_{1B} switching complementarily with S_{2T} and S_{2B} : (a) Touch current measured over the human body impedance simulation network, $V(N005,N008)/500$, value in mA; (b) Touch current measured on the human body impedance simulation network output divided by 500, $V(N013,N008)/500$; (c) Signal on switches gates, $V(N010,Src1T)$ for S_{1T} and S_{1B} , and $V(N006,Src2T)$ for S_{2T} and S_{2B} ; (d) Second-stage *Buck* converter output voltage, $V(n005)$.



Source: Made by the author (2023) on LTspice.

Figure 49 – Touch current comparison on LTspice. Switches S_{1T} and S_{1B} switching at the same time with S_{2T} and S_{2B} : (a) Touch current measured over the human body impedance simulation network, $V(N005,N008)/500$, value in mA; (b) Touch current measured on the human body impedance simulation network output divided by 500, $V(N013,N008)/500$; (c) Signal on switches gates, $V(N010,Src1T)$ for S_{1T} and S_{1B} , and $V(N006,Src2T)$ for S_{2T} and S_{2B} ; (d) Second-stage *Buck* converter output voltage, $V(n005)$.



Source: Made by the author (2023) on LTspice.

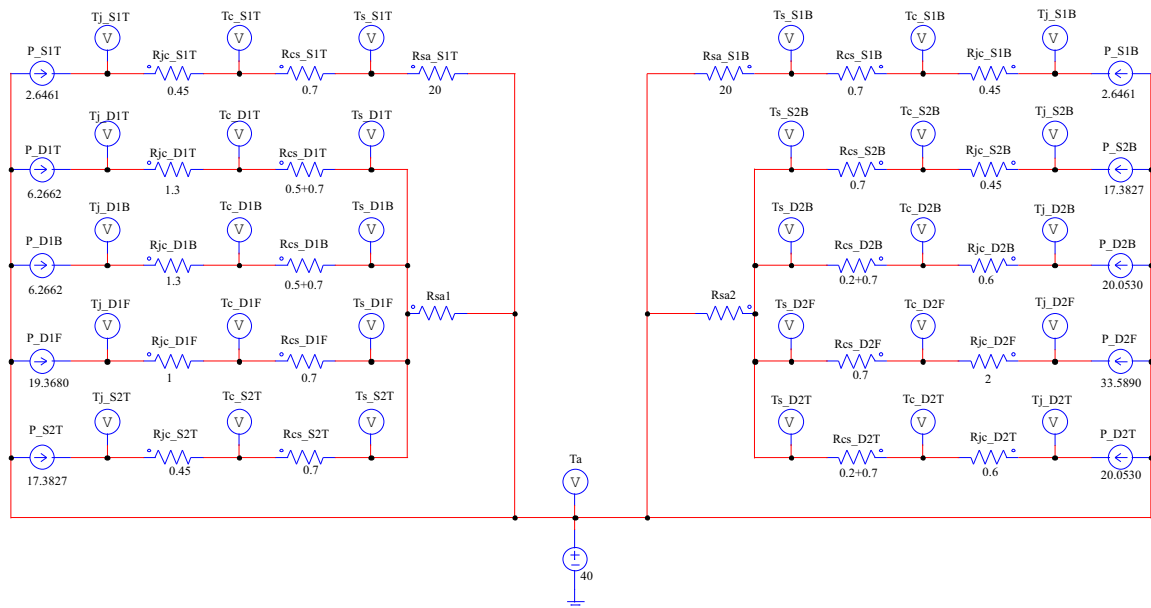
6.3 THERMAL SIMULATION

The power loss is another aspect to be taken care of on the project, as it manifests in the form of heat, it can overheat the converter and, thus, damage it.

With it, a thermal simulation is also made using the software Altair® PSIM™ with the circuit shown at the Figure 50 and the results at the Table 14. The simulation is made considering the power losses presented on Section 5.6 and the thermal resistances at the Section 5.7 to get as a result the temperature at the junction and capsule and also on the heatsink.

It is possible to observe at the Table 14 that the overall temperature on every semiconductor is inside their limitations. The highest observed temperature, on the junction of D_{2F} , is 148.91°C which is below the component maximum rating at 150°C . Although the operation of the converter at environment temperature of 40°C , as simulated, is not common, the small margin for the temperature on D_{2F} could require a substitution of this part for a more thermal efficient one or another heatsink.

Figure 50 – Thermal simulation circuit.



Source: Made by the author (2023) on PSIM.

Table 14 – Thermal simulation result.

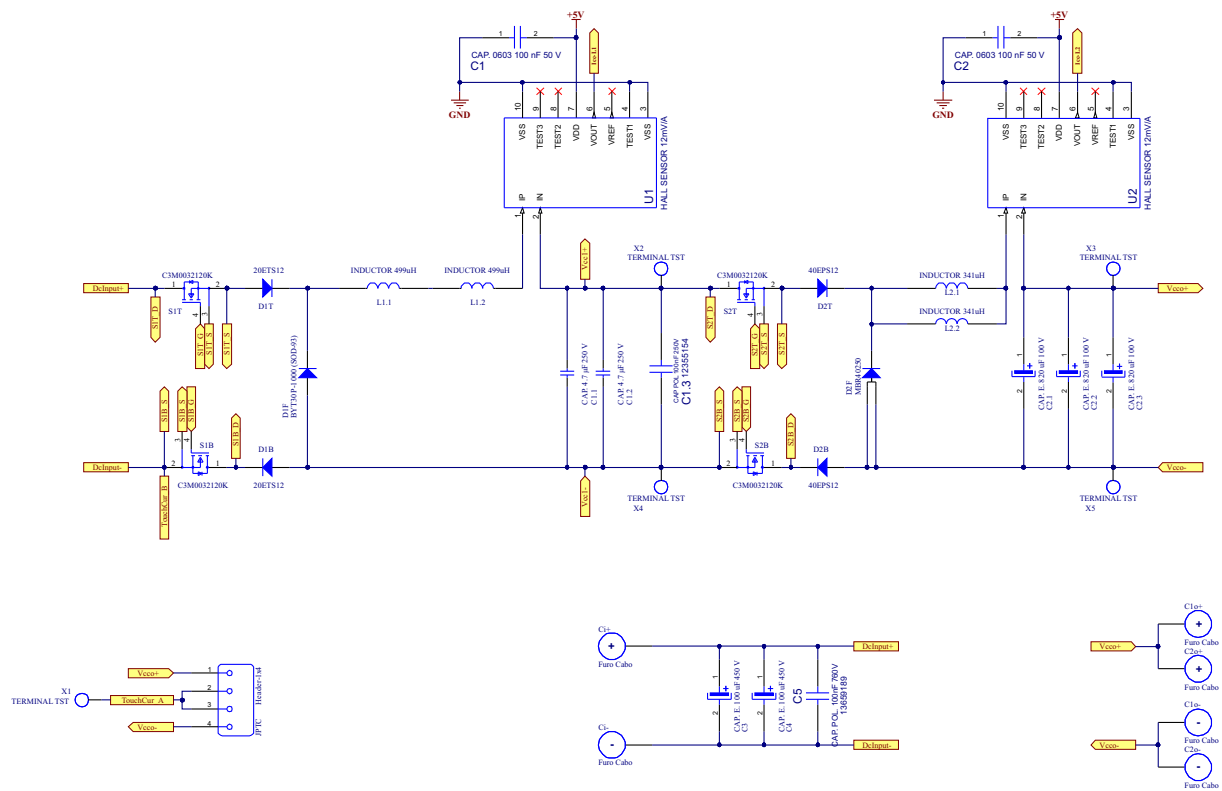
Measurement point	Semiconductor	Temperature [°C]
T_c	D_{1B}	57,376
	D_{1F}	63,414
	D_{1T}	57,376
	D_{2B}	76,263
	D_{2F}	81,728
	D_{2T}	76,263
	S_{1B}	94,774
	S_{1T}	94,774
	S_{2B}	70,383
	S_{2T}	62,025
T_j	D_{1B}	65,522
	D_{1F}	82,782
	D_{1T}	65,522
	D_{2B}	88,295
	D_{2F}	148,906
	D_{2T}	88,295
	S_{1B}	95,965
	S_{1T}	95,965
	S_{2B}	78,206
	S_{2T}	69,847
T_s	D_{1B}	49,857
	D_{1F}	49,857
	D_{1T}	49,857
	D_{2B}	58,216
	D_{2F}	58,216
	D_{2T}	58,216
	S_{1B}	92,922
	S_{1T}	92,922
	S_{2B}	58,216
	S_{2T}	49,857

Source: Made by the author (2023).

7 EXPERIMENTAL RESULTS

The software Altium Designer 23 was used to develop the schematic presented at the Figure 51, with it, on the same software, a new Printed Circuit Board (PCB) layout is designed containing the proposed converter power stage and auxiliary circuits, as the driver stage with the gate driver and gate driver source circuits. After the PCB manufacturing, the components, as selected earlier, were soldered to it and a firmware is developed to generate the modulation for the switches gates. The fully mounted converter is presented in three views on the Figure 52, 53 and 54.

Figure 51 – Board power schematic circuit.

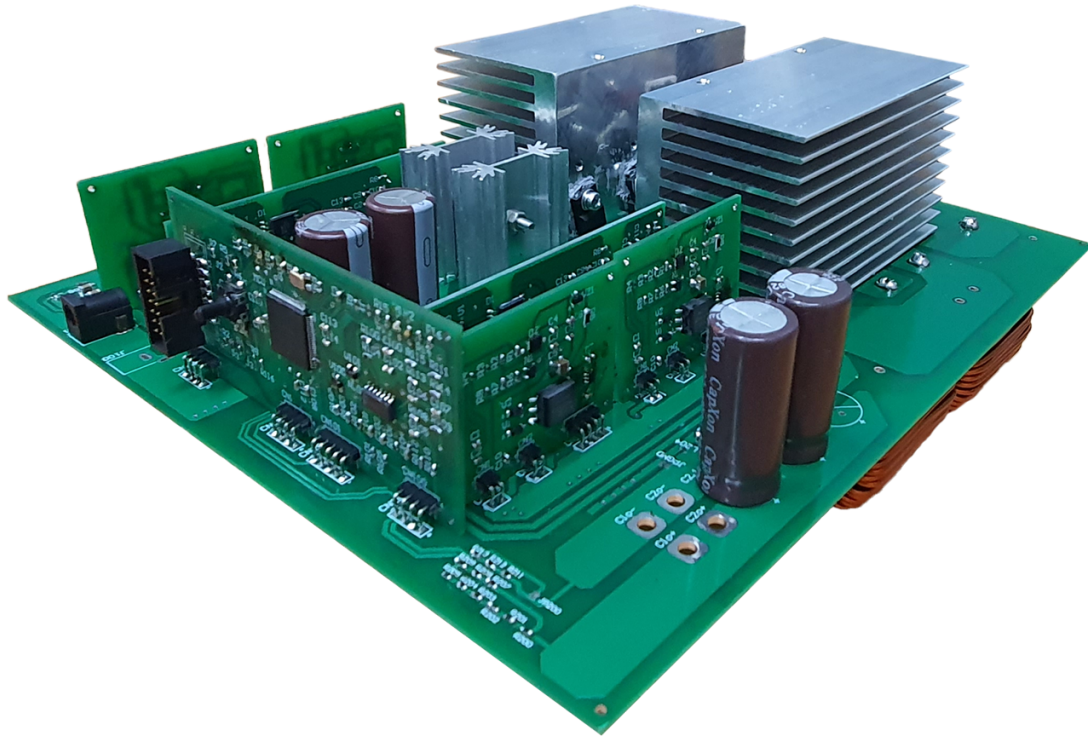


Source: Made by the author (2023) on Altium.

Next, at Figure 55 and Figure 56 the converter parts are identified as:

- (A) Heatsink with the diodes D_{1T} , D_{1B} , D_{1F} and the switch S_{2T} ;
- (B) Heatsink with the diodes D_{2T} , D_{2B} , D_{2F} and the switch S_{2B} ;
- (C) Two individual heatsink, one with the switch S_{1T} and another with S_{1B} ;
- (D) Gate driver source board;
- (E) Input Capacitors;
- (F) Gate driver board;

Figure 52 – Isometric view of the mounted converter board.



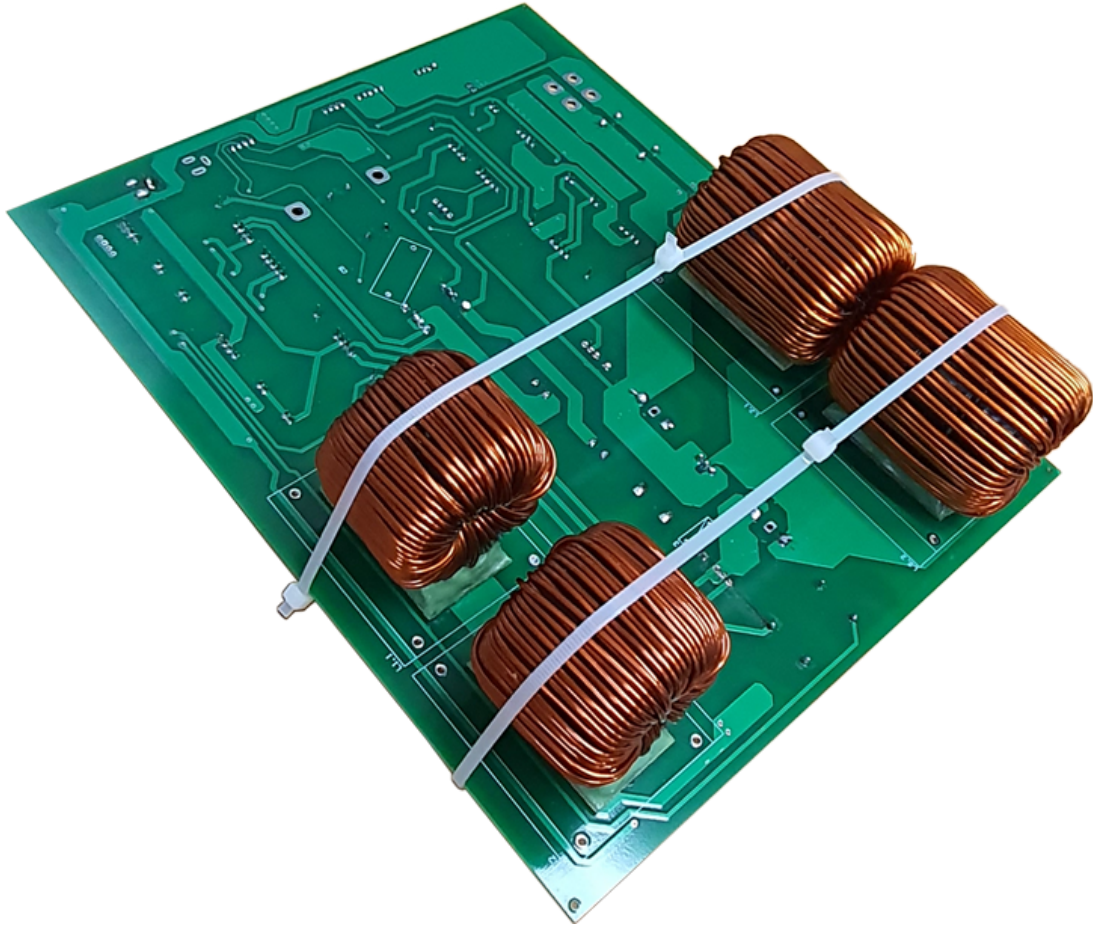
Source: Made by the author (2023).

- (G) Control board;
- (H) Output capacitors C_2 ;
- (I) Input power source;
- (J) Auxiliary input power;
- (K) Inductors L_2 ;
- (L) Converter output;
- (M) Inductors L_1 ;
- (N) Auxiliary circuit: current measuring on L_2 ;
- (O) First stage *Buck* converter output capacitors C_1 ;
- (P) Auxiliary circuit: current measuring on L_1 ;

The gate driver (F) and gate driver source (D) boards, displayed on Figure 56, are on a commercial footprint and Semikron or Supplier's boards can be used.

The functional testing started with a DC input voltage of 100 V and the output is regulated to 10.40 V by manually adjusting the duty cycle. The human body impedance simulation network

Figure 53 – Bottom view of the mounted converter board.



Source: Made by the author (2023).

is connected to the converter's negative rail and the output is connected to a resistive load with six $15\,\Omega$ parallel connected resistors, producing a equivalent resistor of $2.50\,\Omega$.

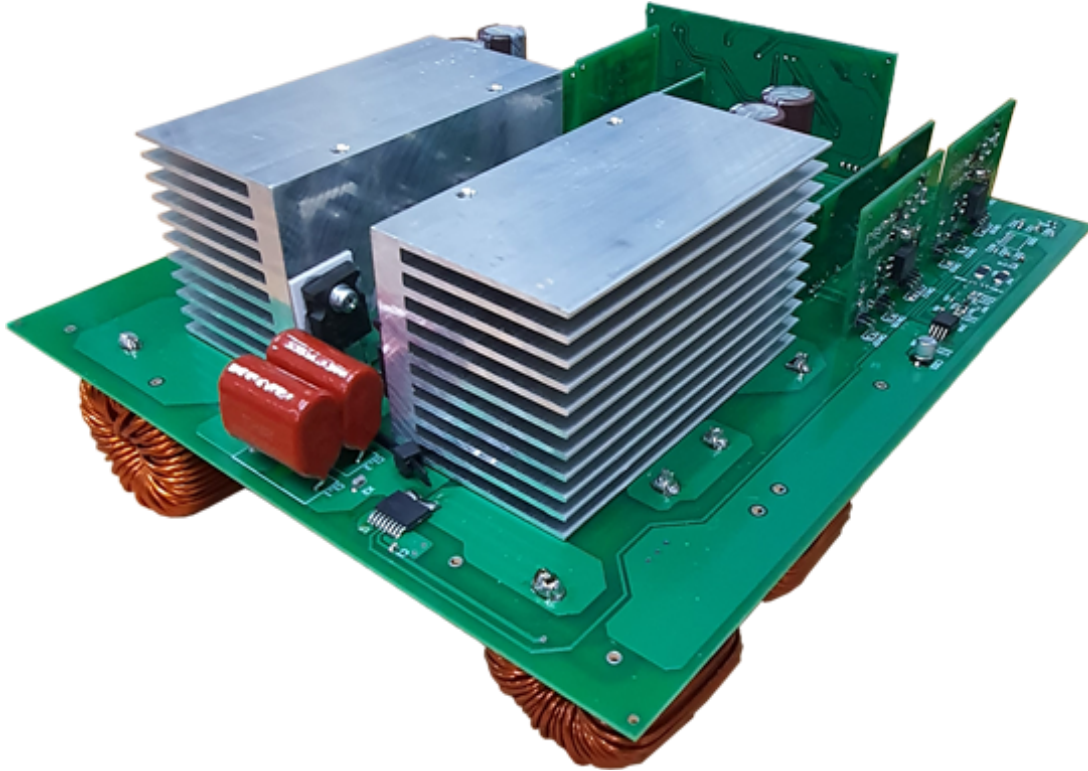
At the Figure 57, the voltage and current on L_1 can be observed, denoting the CCM operation on the first converter stage.

At the Figure 58, the voltage and current on L_2 can be observed, denoting the CCM operation on the second *Buck* converter stage as well.

At the test showed on the Figure 61, the converter is operating specifically with $10.39\,\text{V}$ on its output and $4.18\,\text{A}$ as well as $100\,\text{V}$ on its input with $0.57\,\text{A}$ resulting in an efficiency of 0.76 , under the nominal range, which was expected due to the lower input and output voltage and current. As the diodes forward voltage losses, the voltage will be the same no matter the voltage range on the input or output of the converter. But at lower voltage range, the forward voltage loss is more significant.

Table 15 presents the LTspice simulation results compared to the experimentally measured values. It is evident that the simulated efficiency of 0.89 is significantly higher than both the calculated value of 0.75 and the experimental result of 0.76 , with the latter two being very close. This suggests that the simulation, despite utilizing a real component model, does not account for

Figure 54 – Rear view of the mounted converter board.



Source: Made by the author (2023).

all sources of power loss.

Table 15 – Simulation and experimental average values comparison.

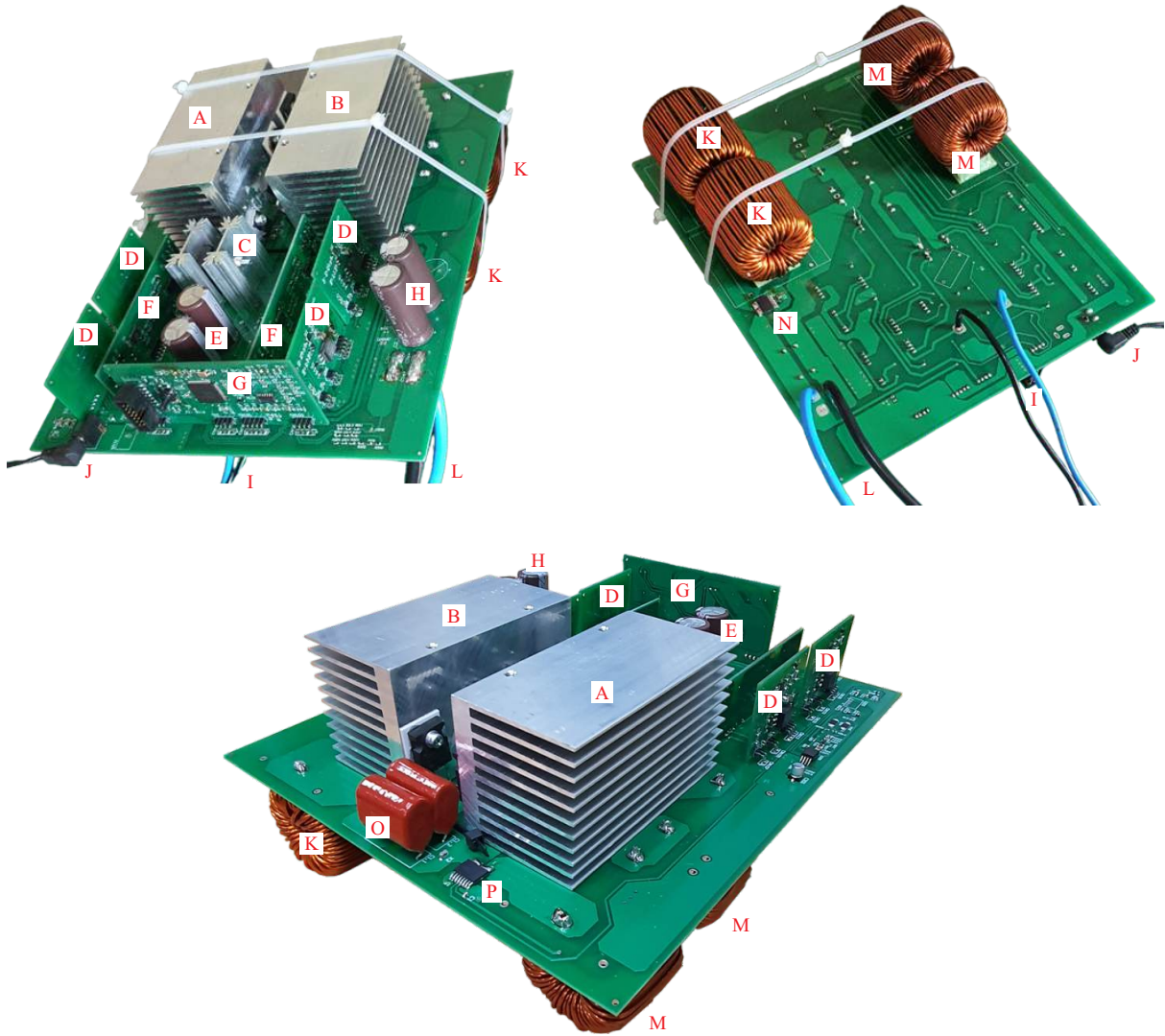
	Simulation	Experimental
$\overline{V}_i$	100 V	100 V
$\overline{V}_o$	10.38 V	10.39 V
$\overline{I}_i$	484.64 mA	570.00 mA
$\overline{I}_o$	4.15 A	4.18 A
$\overline{P}_i$	48.46 W	57.00 W
$\overline{P}_o$	43.08 kW	43.43 kW
η	0.89	0.76

Source: Made by the author (2023).

The Figure 59 and 60 shows the voltage across S_{1T} and S_{2T} , respectively, where it is visible voltage increasing matching when the touch current circulates on those switches.

On the Figure 61 is displayed the measured touch current. The magenta waveform is measured across the human body impedance simulation network and displays the raw touch current waveform circulating by the circuit. The peaks can be seen in the switching time, as expected. The cyan waveform brings the filtered voltage on the output of the human body

Figure 55 – Identification of converter parts.



Source: Made by the author (2023).

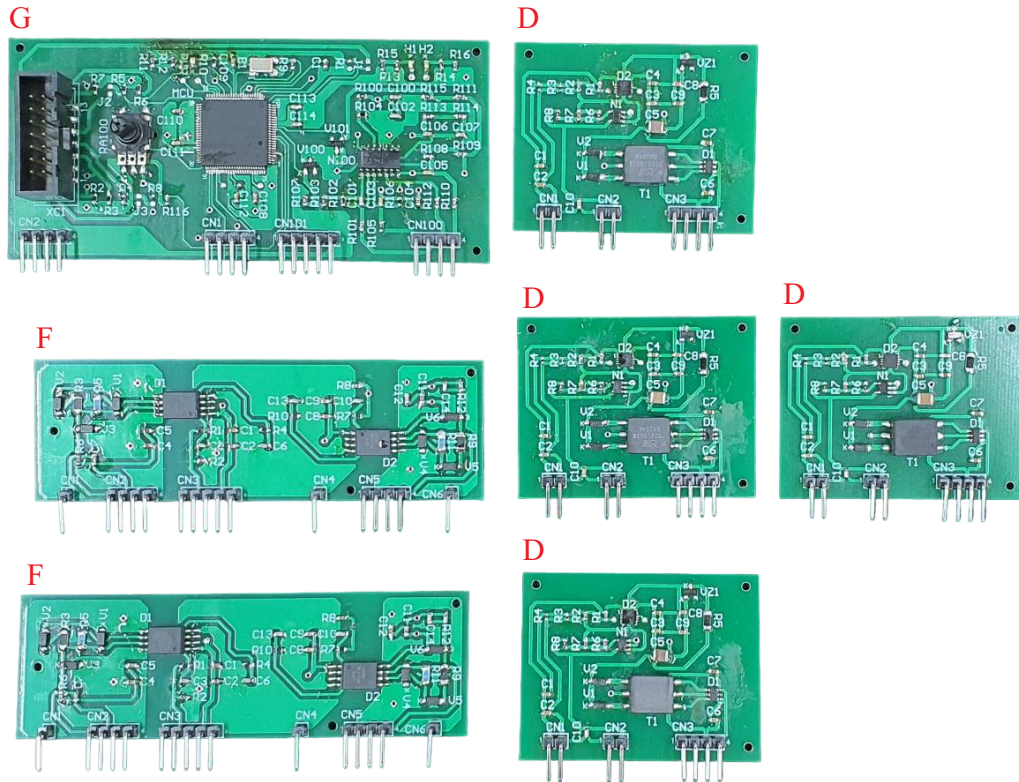
impedance simulation network, this value divided by 500 will result in the touch current value, calculated on the Equation 98, resulting in a higher current than expected.

$$I_{touch} = \frac{V_{touch}}{500} = \frac{3.16}{500} = 6.32 \text{ mA} \quad (98)$$

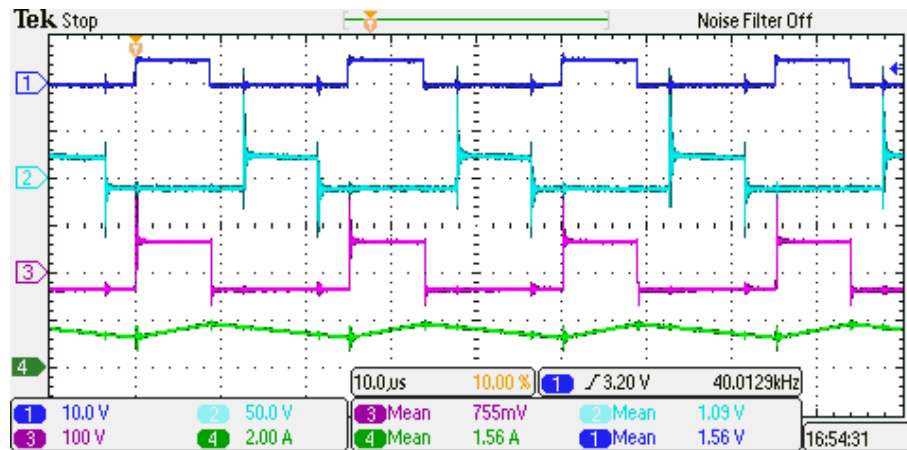
The Table 16 shows the comparison between simulated results and the experimental measured values for the touch current. The big difference between these values shows the discrepancy between the simulation, even it being with the real component models, and the converter prototype.

This result leads to an analysis of the switch's drain-to-source capacitance, which was initially considered variable according to the drain-to-source voltage in the switch's losses calculation. However, when analyzing the touch current, a fixed value from the datasheet was

Figure 56 – Control and driver circuit boards.



Source: Made by the author (2023).

Figure 57 – Functional test waveforms: (1.Blue) S_{1T} gate signal, (2.Cyan) Voltage on L_2 , (3.Magenta) Voltage on L_1 , (4.Green) Current on L_1 .

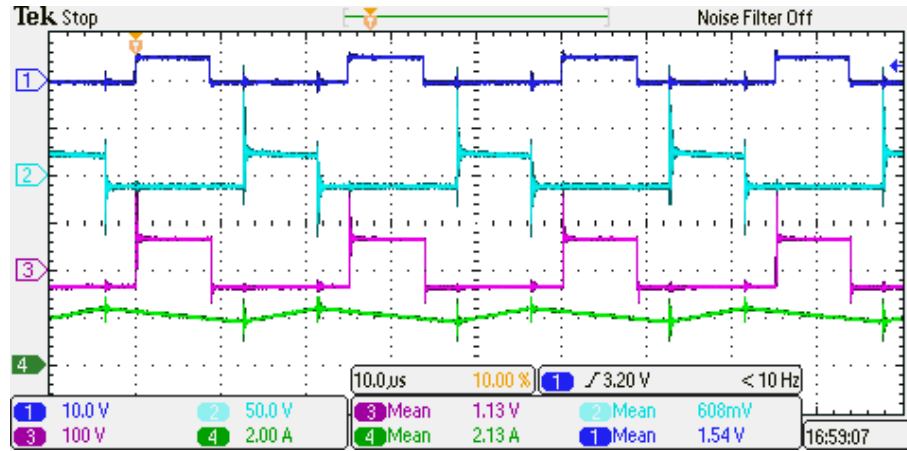
Source: Made by the author (2023).

Table 16 – Simulation and experimental touch current comparison.

	Simulation	Experimental
<i>TouchCurrent</i>	0.88 mA	6.32 mA

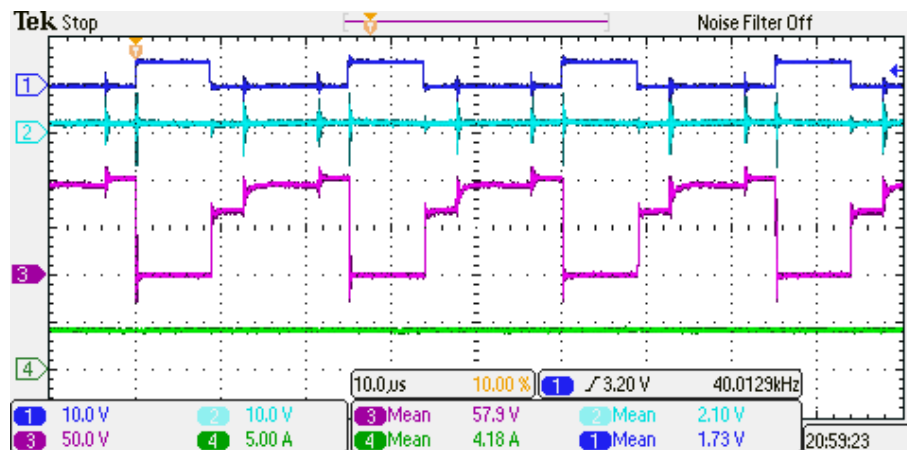
Source: Made by the author (2023).

Figure 58 – Functional test waveforms: (1.Blue) S_{1T} gate signal, (2.Cyan) Voltage on L_2 , (3.Magenta) Voltage on L_1 , (4.Green) Current on L_2 .



Source: Made by the author (2023).

Figure 59 – Functional test waveforms: (1.Blue) S_{1T} gate signal, (2.Cyan) Voltage on D_{1T} , (3.Magenta) Voltage on S_{1T} , (4.Green) Output current.



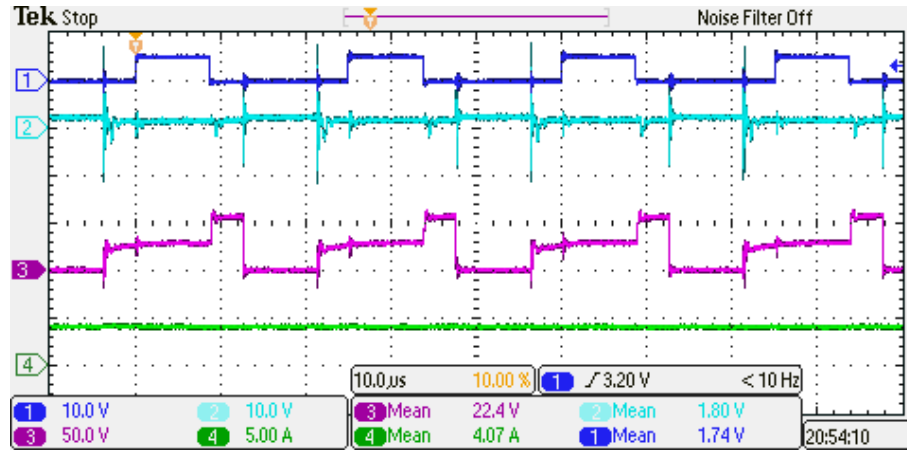
Source: Made by the author (2023).

used. This value considers a drain-to-source voltage of 1000 V, whereas the experimental test operates at 100 V for S_{1T} and 50 V on S_{2T} at their maximum. As a result, the switch's drain-to-source capacitance increased to approximately three times its $C_{sd,1000V}$ value, as indicated in Figure 62 presented on the switch's datasheet.

This raise on the switch's drain-to-source capacitance, added the generated capacitance between the heatsink and the semiconductors, and the intrinsic layout capacitance, led to a raise on the touch current to the experimental result value, thus, not complying with the IEC 60950-1 standard.

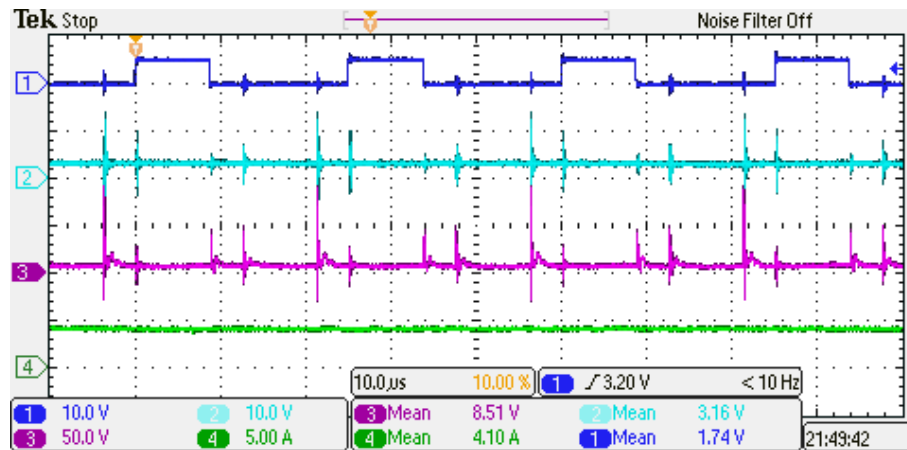
To investigate this discrepancy, various aspects were examined. Initially, the switch's output capacitance was measured using an RLC bridge, yielding a value of 3.25 nF. This value, measured with a 500mV offset, aligns with the datasheet specifications. However, measurements with a DC offset to verify capacitance at operating conditions were hindered by the limited

Figure 60 – Functional test waveforms: (1.Blue) S_{1T} gate signal, (2.Cyan) Voltage on D_{2T} , (3.Magenta) Voltage on S_{2T} , (4.Green) Output current.



Source: Made by the author (2023).

Figure 61 – Functional test waveforms: (1.Blue) S_{1T} gate signal, (2.Cyan) Filtered voltage on the output of the human body impedance simulation network, (3.Magenta) Voltage on the input of the human body impedance simulation network, (4.Green) Output current.



Source: Made by the author (2023).

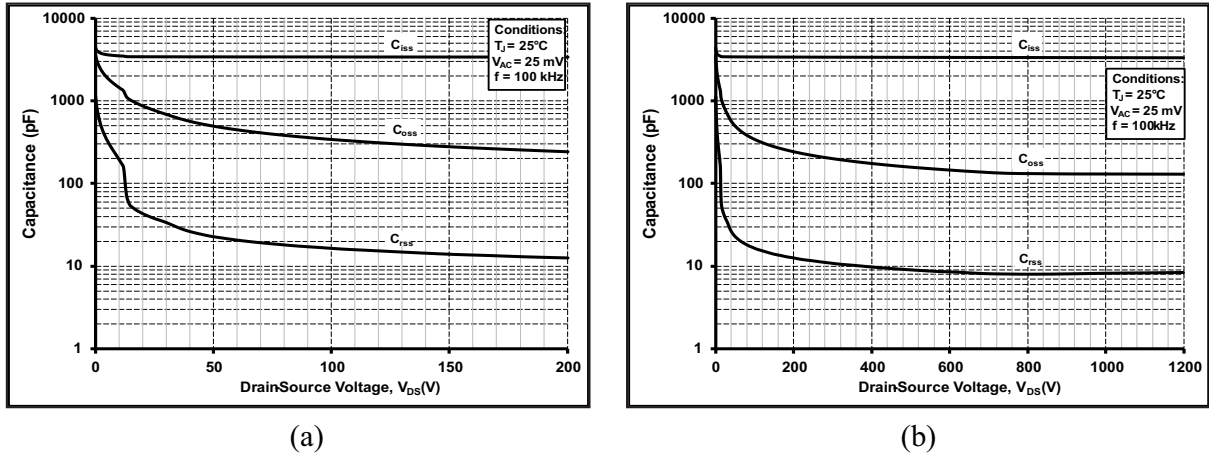
precision of the laboratory equipment, rendering the results inconclusive.

Although the nominal voltage is higher on both input and output, and consequently higher on the switch drain-to-source rails, it is insufficient to achieve a touch current within the desired 3.50 mA or lower range.

Another hypothesis considered the PCB layout and the heatsink, as shown in Figure 63. It was observed that the polygons beneath the heatsink could generate significant capacitances within the circuit. Measurements with the RLC bridge revealed capacitances exceeding 20 nF. If considered in simulations, these values would significantly increase the touch current.

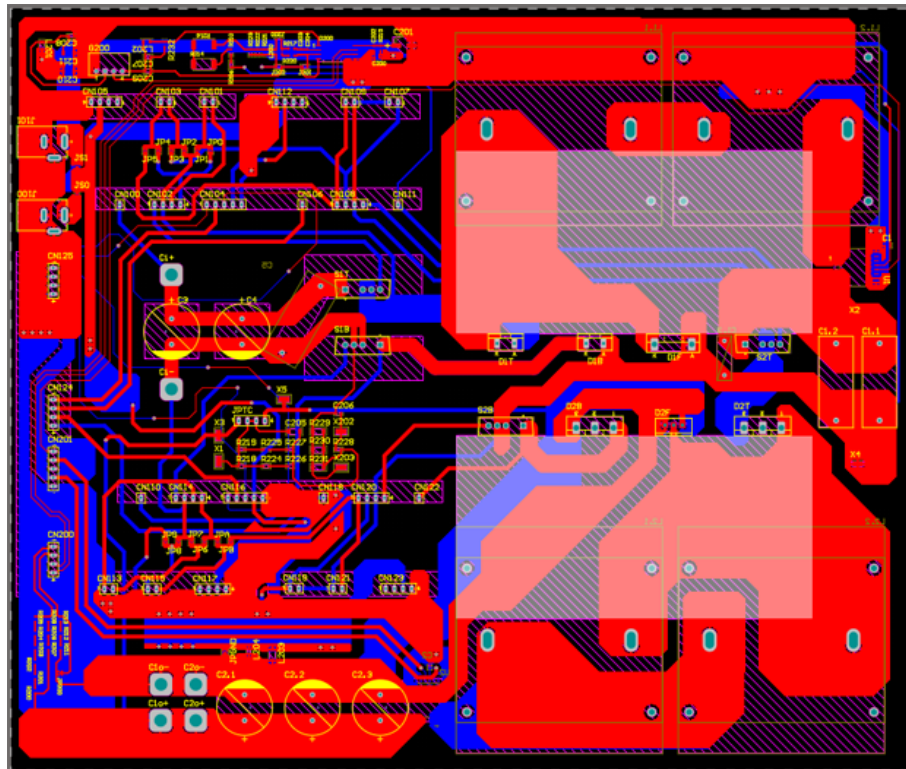
By removing both heatsinks, the setup shown in Figure 64 is configured to test this hypothesis. Although the touch current is reduced to 5.50 mA, but it still does not comply with the standard and has not been reduced enough to match the simulation results.

Figure 62 – Switch capacitance according to its drain-to-source voltage as on the datasheet. (a) From 0 to 200 V. (b) From 0 to 1200 V.



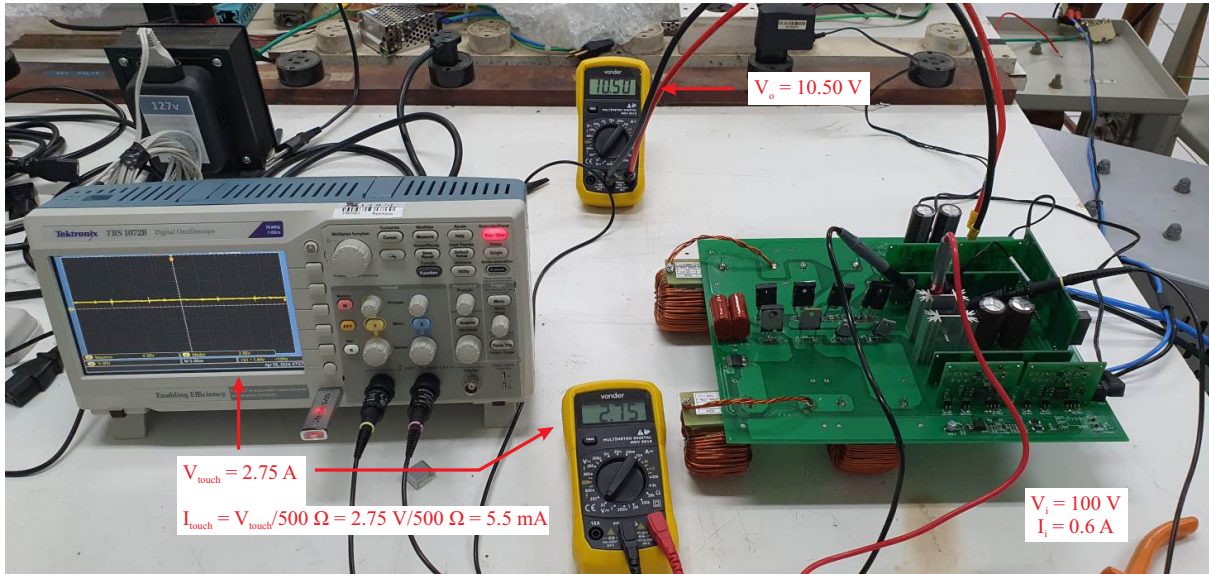
Source: Adapted from C3M0032120K datasheet.

Figure 63 – Converter layout highlighting the heatsink.



Source: Made by the author (2023) on Altium.

Figure 64 – Touch current testing without heatsink.



Source: Made by the author (2023).

Additional tests were conducted to assess the touch current at higher voltages. However, the simulation network for human body impedance was not designed to measure higher currents and experienced overheating, rendering it impractical to continue testing with higher touch currents.

A switch with a lower voltage rating within the same component family would exhibit a reduced drain-to-source capacitance, potentially lowering the touch current. However, this presents a trade-off with another IEC 60950-1 standard test: the Electric Strength feature, which requires a high voltage standing semiconductor. Thus, there exists a trade-off between the two tests and the voltage rating.

8 CONCLUSION

On this work, a dual stage DC-DC *Buck* converter with SGI is made aiming at the battery charging for industrial applications, with the main objective of obtaining knowledge on the SGI technology, which is a recently explored area, with a limited literature available, including (YAO, 2018), (YAO et al., 2020), (ZHANG et al., 2016), (ZHANG et al., 2018) and (ZHANG et al., 2014).

Throughout the development process, a group of topologies containing the SGI feature is analyzed and the most promising one is selected to be studied and tested with simulation and practically with an assembled converter board.

The proposed topology is then analyzed on various aspects, including the touch current. The design of every component is made considering its application, voltage and current stresses, power losses and thermal characteristics. Simulations were made with ideal and non-ideal components so the converter operation and designed values could be assured.

Finally, a layout for a new PCB is made and a practical converter is manufactured with the proposed topology and auxiliary circuits. This converter is tested to be functional although the touch current did not comply with the IEC 60950-1 standard as measured on the converter. One detail on the switch's drain-to-source assumed capacitance made it unviable.

After all, the SGI technology could be studied with all the design, simulation, and experimental results. The non-compliance with the standard was not expected, but it is a common problem addressed in the literature to be solved, so far, only with active touch current suppressing methods, this is to be one of the future proposed work for the converter. A separated heatsink for each component with reduced capacitance generated by the proximity with polygons and PCB tracks also can be tested to reduce the touch current.

The components used on the converter were selected on a local availability, thus, they are not optimized to the best of the market solutions. This optimization could contribute to improving the converter efficiency as well as reducing the touch current. A fast recovery diode with low forward voltage was not found for D_{1F} and D_{2F} , thus, a optimization of this component would increase the converter's efficiency. As for the switch, a lower drain-to-source capacitance would reduce the touch current. A switch that permits only unidirectional current flow, without an internal antiparallel diode, could also enhance efficiency by eliminating the need for a series reverse current blocking diode.

The inductors currently employed in the converter might not be ideal for board manufacturing, the transformer with a pin-through-hole package may pose challenges. Therefore, incorporating a planar inductor, as the example presented on (SOUZA, 2018), would enhance this aspect for future iterations of the project.

In conclusion, the SGI technology would require enhancements to become viable when compared to classical technologies utilizing transformers or coupled inductors. Key areas for improvement include efficiency and compliance with touch current regulations. However, the

advantage of not requiring magnetic components would primarily benefit manufacturability and component availability.

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