UNIVERSIDADE DO ESTADO DE SANTA CATARINA – UDESC
CENTRO DE CIÊNCIAS TECNOLÓGICAS – CCT
PROGRAMA DE PÓS-GRADUAÇÃO EM ENGENHARIA ELÉTRICA – PPGEEL

AUGUSTO MANFROI MEDEIROS

ASSESSMENT OF A CONVENTIONAL 4L DC-DC FLYING CAPACITOR TOPOLOGY TO OPERATE IN RESONANT MODE AND SOFT-SWITCHING CAPABILITY

JOINVILLE
2024

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Master's thesis presented to the Graduate Program in Electrical Engineering of the Santa Catarina State University, as requirement for obtention of the title of Master in Electrical Engineering, concentration area of Electronic Systems.

Supervisor: Yales Rômulo de Novaes, Dr.

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Ficha catalográfica elaborada pelo programa de geração automática da

Biblioteca Universitária Udesc,

com os dados fornecidos pelo(a) autor(a)

Manfroi Medeiros, Augusto
Assessment of a conventional 4L DC-DC Flying Capacitor Topology to operate in resonant mode and soft-switching capability / Augusto Manfroi Medeiros. -- 2024.
194 p.

Orientador: Yales Rômulo de Novaes
Dissertação (mestrado) -- Universidade do Estado de Santa Catarina, Centro de Ciências Tecnológicas, Programa de Pós-Graduação em Engenharia Elétrica, Joinville, 2024.

1. DC/DC Conversion. 2. Flying-Capacitor. 3. Multi-Resonant. 4. State-plane Trajectory. 5. WBG Devices. I. Rômulo de Novaes, Yales. II. Universidade do Estado de Santa Catarina, Centro de Ciências Tecnológicas, Programa de Pós-Graduação em Engenharia Elétrica. III. Título.

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Joinville, August 28th, 2024

I dedicate this work to my parents, Flavio Medeiros and Ana Lucia Manfroi, to my brother Gustavo Manfroi Medeiros, and to my great wife, Mariane Hans Alexandre, who has devoted tremendous patience during this process.

ACKNOWLEDGEMENTS

First of all, I would like to thank the State University of Santa Catarina (UDESC), the Electrical Engineering Graduation Program (PPGEEL) and the Núcleo de Processamento de Energia Elétrica (NPEE), for letting me be part of this program. Further, I would like to express my immense gratitude to my supervisor Yales for showing me the patience, resilience and the thoughtful discussions and advises not only professionally but also personally.

To my former employer, Volvo Car Corporation, and the staff, Riccardo Negri and Lars Johansson, who have encouraged me and let me pursue this path while reducing my working hours to dedicate to this project. Additionally, for the unconditional support and willingness to provide the lab infrastructure which was crucial for the validation and finalization of the project. Further, to my current Employer, OAK Amplifiers AB, and the staff, Mats and Sandra Otterdahl, who have been extremely supportive to my continuous education.

My parents, Flavio Augusto Jorge Medeiros and Ana Lucia Manfroi, who have guided me and provided for my wellness, without whom none if this would be possible. I extend this acknowledgment to my brother, Gustavo Manfroi Medeiros.

Lastly, I would like to express my gratitude, and appreciation, to my beloved wife, Mariane Hans Alexandre, who has accompanied me since before this journey has started and who has been showing me the strength and courage to continue pursuing this path. Furthermore, to the many days, holidays and vacations that, most importantly, were devoted and sacrificed, to let me focus on this project.

“The future belongs to those who believe in the beauty of their dreams.” (ELEANOR ROOSEVELT, [19–])

ABSTRACT

Multi-level Resonant Converter topologies have been addressed to increase the power density and efficiency of step-down intermediate conversion stages, for Low-voltage (LV) systems, due to the higher current demand, in addition to its inherent benefit of soft-switching capability and fixed static-gain ratio, while operating above, or at, Resonance. This work proposes an extension for the Multi-level Resonant Flying Capacitor Converter (ML-RFLCC), by demonstrating the potential soft-switching and voltage regulation capabilities of a 1:3 RFLCC while operating under, and at, the Resonance. Due to the increased number of state variables, it presents a comprehensive state diagram to demonstrate the operating principle, and dependencies, of the different set of LC resonant tanks. In order to achieve such operation, this work proposes a operating condition coefficient Λ to derive a design methodology. To validate the proposed operation condition, a 400V 500W GaN-based 1:3 RFLCC is presented, illustrating the theoretical correlation and non-idealities while operating under-resonance.
Keywords: DC-DC Conversion, Multi-level Converter. Flying-Capacitor. Multi-Resonant. State-plane Trajectory. WBG Devices.

RESUMO

Conversores ressonantes multiníveis têm sido utilizados para alcançar altos níveis de densidade de potência e eficiência em conversores abaixadores de baixa tensão (LV), devido à demanda por altas correntes de saída e aos benefícios das propriedades de comutação suave. Esses conversores normalmente operam sincronizados ou acima da frequência de ressonância devido às suas características. Este trabalho propõe uma extensão ao conversor ressonante multinível do tipo capacitor flutuante (ML-RFLCC), demonstrando a capacidade de um conversor 1:3 de atingir comutação suave e regulação da tensão de saída enquanto opera em sincronização, ou abaixo, da frequência de ressonância. Por conta do número de variáveis de estado, é proposto um diagrama de estados para demonstrar o funcionamento do conversor proposto, e suas dependências, dos diferentes tanques ressonantes. Para atingir esses objetivos, este trabalho propõe um coeficiente de operação Λ. Um protótipo, empregando chaves do tipo GaN, é desenvolvido para validar os resultados teóricos e as não idealidades enquanto operando abaixo da frequência de ressonância.

Palavras-chave: Conversão CC-CC. Conversores Multiníveis. Capacitor Flutuante. Ressonância Multipla. Trajetória do plano de estado. semicondutores WBG.

LIST OF FIGURES

Figure 1 – Representation of Base form of different DC-DC Switched-Capacitor Topologies. 27
Figure 2 – Representation of different approaches for the realization of resonant switched-capacitor converter (ReSCC). 29
Figure 3 – Basic Structure for a 3L flying capacitor boost DC-DC converter. 30
Figure 4 – 3L resonant flying capacitor equivalent circuit for every topological stage. . 34
Figure 5 – Generic Structure for a n-level resonant flying capacitor boost DC-DC converter. 35
Figure 6 – Proposed Converter Circuit Topology. 35
Figure 7 – Generic Series Resonance LC Equivalent Circuit with a Differential-mode Voltage Excitation Signal. 37
Figure 8 – Normalized State-Plane Trajectory for a Generic LC series resonant circuit. 40
Figure 9 – Generic Series Resonance LCCp Equivalent Circuit with a Differential-mode Voltage Excitation Signal. 41
Figure 10 – Normalized State-Plane Trajectory for a Generic LCCp series resonant circuit. 43
Figure 11 – Generic Series Resonance LCCs Equivalent Circuit with a Differential-mode Voltage Excitation Signal. 44
Figure 12 – Normalized State-Plane Trajectory for a Generic LCCs series resonant circuit. 46
Figure 13 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region I within Interval I. 51
Figure 14 – Equivalent Circuit for Operating Region I within Interval II. 51
Figure 15 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region I within Interval IV. 53
Figure 16 – Equivalent Circuit for Operating Region I within Interval V. 53
Figure 17 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region I within Interval VII. 55
Figure 18 – Equivalent Circuit for Operating Region I within Interval VIII. 55
Figure 19 – Normalized State-Plane Trajectory for Operating Region I. 57
Figure 20 – Normalized Time-Domain State Variables for Operating Region I. 57
Figure 21 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region II within Interval I. 59
Figure 22 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region II within Interval III. 61
Figure 23 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region II within Interval IV. 63
Figure 24 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region II within Interval VI. 65

Figure 25 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region II within Interval VII. 66
Figure 26 – Normalized State-Plane Trajectory for Operating Region II. 68
Figure 27 – Normalized Time-Domain State Variables for Operating Region II. 68
Figure 28 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region III within Interval I. 70
Figure 29 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region III within Interval II. 72
Figure 30 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region III within Interval IV. 74
Figure 31 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region III within Interval VI. 76
Figure 32 – Normalized State-Plane Trajectory for Operating Region III. 77
Figure 33 – Normalized Time-Domain State Variables for Operating Region III. 77
Figure 34 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region IV within Interval I. 79
Figure 35 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region IV within Interval III. 81
Figure 36 – Equivalent Circuit and Normalized State-Plane Trajectory for Operating Region IV within Interval VI. 83
Figure 37 – Normalized State-Plane Trajectory for Operating Region IV. 84
Figure 38 – Normalized Time-Domain State Variables for Operating Region IV. 85
Figure 39 – Area representation of Switch S_6 Current waveform within the topological stages under Region I condition. 88
Figure 40 – Output Static Gain and Phase-Timing Characteristics as a function of Λ within Region I. 89
Figure 41 – Area representation of Switch S_6 Current waveform within the topological stages under Region II condition. 91
Figure 42 – Output Static Gain and Phase-Timing Characteristics as a function of Λ within Region II. 93
Figure 43 – Interval III and Interval IV Peak current stresses progression based on State-plane Trajectory. 93
Figure 44 – Peak current stresses progression based on resonant semi-cycles under Region II condition. 94
Figure 45 – Area representation of Switch S_6 Current waveform within the topological stages under Region III condition. 95
Figure 46 – Output Static Gain and Phase-Timing Characteristics as a function of Λ within Region III. 97

Figure 47 – Interval I and II Peak Current Stress Impact as a function of Λ within Region III. 97
Figure 48 – Area representation of Switch S_6 Current waveform within the topological stages under Region IV condition. 99
Figure 49 – Output Static Gain Characteristics as a function of Λ within Region IV. . . . 100
Figure 50 – Cycle-by-Cycle Maximum Normalized Peak Current Large-Signal Characteristic under Region I to IV condition. 102
Figure 51 – Global Maximum Normalized Peak Current Large-Signal Characteristic under Region I to IV condition. 102
Figure 52 – 4L-RFLCC Static Output and Flying capacitors' Voltage Characteristic under Region I to IV condition. 103
Figure 53 – 4L-RFLCC Switches $S_1 - S_6$ Maximum Current Stress Characteristic under Region I to IV condition. 103
Figure 54 – 4L-RFLCC Switches $S_1 - S_6$ Maximum Voltage Stress Characteristic under Region I to IV condition. 104
Figure 55 – Absolute Peak Current and Voltage Stresses for Active Switch S_1 under Target Specification Range. 106
Figure 56 – Absolute Peak Current and Voltage Stresses for Active Switch S_2 under Target Specification Range. 107
Figure 57 – Absolute Peak Current and Voltage Stresses for Active Switch S_3 under Target Specification Range. 107
Figure 58 – Absolute Peak Current and Voltage Stresses for Active Switch S_4 under Target Specification Range. 108
Figure 59 – Absolute Peak Current and Voltage Stresses for Active Switch S_5 under Target Specification Range. 108
Figure 60 – Absolute Peak Current and Voltage Stresses for Active Switch S_6 under Target Specification Range. 109
Figure 61 – Resonant Inductor Design and Built for the purpose of validating the proposed 4L-RFLCC. 112
Figure 62 – DC-link Capacitor Architecture for the Proposed 4L-RFLCC Prototype. . . 114
Figure 63 – SiC/GaN R_{ON} and Q_{OSS} distribution per device for different junction temperature conditions. 119
Figure 64 – SiC/GaN DFOM performance assessment as a function of junction temperature. 120
Figure 65 – *Gan Systems*'s *GS-0650-180-2-L*'s Reverse conduction Performance with junction temperature as a parameter for different turn-OFF gate voltage. . . 121
Figure 66 – *Gan Systems*'s *GS-0650-180-2-L*'s Reverse conduction Performance comparison towards 650V SiC Diodes from different suppliers with forward current I_{DS} as a parameter for different Junction Temperatures T_j. 122

Figure 67 – 650V SiC Diodes V_F and Q_C distribution per device for different junction temperature conditions under 10A forward current condition. 123
Figure 68 – System-level description of the FCML converter employing Cascaded Bootstrap Gate Drive. 124
Figure 69 – System-level description of the FCML converter employing Cascaded Bootstrap Gate Drive and Charge-Pump. 125
Figure 70 – System-level Implementation of AHV85110 Bipolar Drive Supply for GaN Systems' GS-065-018-2-L. 127
Figure 71 – Different Representations of a GaN device. 128
Figure 72 – System-Level Description Model including Parasitic Elements in a single Flying Capacitor Commutation Cell (FLCCC). 129
Figure 73 – Different Vertical Commutation Loop layout approaches. 130
Figure 74 – Final PCB Design Top and Bottom Layer View of a Flying Capacitor Commutation Cell 131
Figure 75 – Prototype Board Altium 3D view. 131
Figure 76 – Experimental Testing Setup for 4L-RFLCC validation. 132
Figure 77 – Prototype Board for 4L-RFLCC validation. 133
Figure 78 – Experimental Test Condition Points utilized during the 4L-RFLCC prototype validation. 134
Figure 79 – Experimental Results under Test Condition Set 1 and 2. 135
Figure 80 – 1st to 3rd Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 10kHz$ based on Clock-wise PWM Sequence. 136
Figure 81 – 4th to 6th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 10kHz$ based on Clock-wise PWM Sequence. 137
Figure 82 – 7th to 9th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 10kHz$ based on Clock-wise PWM Sequence. 137
Figure 83 – 1st to 3rd Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 10kHz$ based on Counter Clock-wise PWM Sequence. 138
Figure 84 – 4th to 6th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 10kHz$ based on Counter Clock-wise PWM Sequence. 138
Figure 85 – 7th to 9th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 10kHz$ based on Counter Clock-wise PWM Sequence. 139
Figure 86 – Experimental results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 50kHz$ based on Clock-wise PWM Sequence Type. 139
Figure 87 – 4th to 6th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 50kHz$ based on Clock-wise PWM Sequence. 140
Figure 88 – 7th to 9th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 50kHz$ based on Clock-wise PWM Sequence. 140

Figure 89 – Experimental results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Clock-wise PWM Sequence Type. 141
Figure 90 – Experimental results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Counter Clock-wise PWM Sequence Type. 141
Figure 91 – 1st to 2nd Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Clock-wise PWM Sequence. 142
Figure 92 – 3rd to 5th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Clock-wise PWM Sequence. 142
Figure 93 – 6th to 8th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Clock-wise PWM Sequence. 143
Figure 94 – 1st to 3rd Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Counter Clock-wise PWM Sequence. 143
Figure 95 – 4th to 5th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Counter Clock-wise PWM Sequence. 144
Figure 96 – 6th to 8th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Counter Clock-wise PWM Sequence. 144
Figure 97 – Experimental results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 300kHz$ based on Clock-wise PWM Sequence Type. 145
Figure 98 – 1st to 3rd Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 300kHz$ based on Counter Clock-wise PWM Sequence. 145
Figure 99 – 4th to 5th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 300kHz$ based on Counter Clock-wise PWM Sequence. 146
Figure 100 – 6th to 7th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 300kHz$ based on Counter Clock-wise PWM Sequence. 146
Figure 101 – Experimental Results Comparison for two different test conditions under the same Λ condition. 147
Figure 102 – Experimental results under Test Condition 9 highlighting the Resonant State Variables. 148
Figure 103 – 1st to 2nd Topological Stage Resonant Variables Experimental results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 500kHz$ based on Counter Clock-wise PWM Sequence. 148
Figure 104 – 4LRFLCC Equivalent Circuit upon Transition State 11 including Reverse-biased Diode D_5's intrisic output capacitance C_o 149
Figure 105 – 3rd to 4th Topological Stage Resonant Variables Experimental results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 500kHz$ based on Counter Clock-wise PWM Sequence. 149
Figure 106 – 5th to 6th Topological Stage Resonant Variables Experimental results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 500kHz$ based on Counter Clock-wise PWM Sequence. 150

Figure 107 – Experimental and Theoretical results comparison for the proposed converter within Operating Regions I to IV. 151
Figure 108 – Experimental results under Test Condition ⑩ highlighting the Resonant State Variables. 151
Figure 109 – Experimental results under Test Condition ⑪ highlighting the Resonant State Variables. 152
Figure 110 – Active Devices $S_1 - S_3$ High-frequency and Floating Voltage Measurement setup. 153
Figure 111 – Passive Devices $D_4 - D_6$ High-frequency and Floating Voltage Measurement setup. 154
Figure 112 – Switch S_1 and D_6 Voltage Stresses Experimental Results within Operating Region I and Test Condition ①. 155
Figure 113 – Switch S_3 and D_4 Voltage Stresses Experimental Results within Operating Region I and Test Condition ①. 156
Figure 114 – Switch S_2 and D_5 Voltage Stresses Experimental Results within Operating Region I and Test Condition ①. 157
Figure 115 – Switch S_1 and D_6 Dynamic Voltage Behaviour upon the Transition Event ⑪ under Test Condition ①. 158
Figure 116 – Switch S_3 and D_4 Dynamic Voltage Behaviour upon the Transition Event ⑪ under Test Condition ①. 159
Figure 117 – Switch D_6 Dynamic voltage behaviour upon Transient Event ⑪ under Test Condition ①. 159
Figure 118 – Switch S_3 and D_4 Dynamic Voltage Behaviour upon the Transition Event ㉑ under Test Condition ①. 160
Figure 119 – Switch S_2 and D_5 Dynamic Voltage Behaviour upon the Transition Event ㉑ under Test Condition ①. 161
Figure 120 – Switch D_4 Dynamic voltage behaviour upon Transient Event ㉑ under Test Condition ①. 161
Figure 121 – Switch S_2 and D_5 Dynamic Voltage Behaviour upon the Transition Event ㉛ under Test Condition ①. 162
Figure 122 – Switch S_1 and D_6 Dynamic Voltage Behaviour upon the Transition Event ㉛ under Test Condition ①. 163
Figure 123 – Switch D_5 Dynamic voltage behaviour upon Transient Event ㉛ under Test Condition ①. 164
Figure 124 – Switch S_1 and D_6 Voltage Stresses Experimental Results within Operating Region II and Test Condition ④. 165
Figure 125 – Switch S_3 and D_4 Voltage Stresses Experimental Results within Operating Region II and Test Condition ④. 166

Figure 126 – Switch S_2 and D_5 Voltage Stresses Experimental Results within Operating Region II and Test Condition ④. 167
Figure 127 – Switch S_3 and D_4 Dynamic Voltage Stresses Experimental Results within Operating Region II and Test Condition ④ upon a Transition Event (11 ↑). . 168
Figure 128 – Switch S_3 and D_4 Dynamic Voltage Stresses Experimental Results within Operating Region II and Test Condition ④ upon the First Idle State. 169
Figure 129 – Switch S_2 and D_5 Dynamic Voltage Stresses Experimental Results within Operating Region II and Test Condition ④ upon the Second Idle State. . . . 170
Figure 130 – Switch S_1 and D_6 Dynamic Voltage Stresses Experimental Results within Operating Region II and Test Condition ④ upon the Third Idle State. 171
Figure 131 – Switch S_1 and D_6 Voltage Stresses Experimental Results within Operating Region III and Test Condition ⑥. 172
Figure 132 – Switch S_3 and D_4 Voltage Stresses Experimental Results within Operating Region III and Test Condition ⑥. 173
Figure 133 – Switch S_2 and D_5 Voltage Stresses Experimental Results within Operating Region I and Test Condition ⑥. 174
Figure 134 – Switch S_1 and S_3 Idle State's Dynamic Voltage Stresses Experimental Results within Operating Region III and Test Condition ⑥. 175
Figure 135 – Active Switches Idle State's Dynamic Voltage Sharing Experimental Results within Operating Region III and Test Condition ⑥ during Dead-Time. . . . 176
Figure 136 – Passive Switches Idle State's Dynamic Voltage Sharing Experimental Results within Operating Region III and Test Condition ⑥ during Dead-Time. . . . 177
Figure 137 – Switch Pair S_1 and D_6 Voltage Stresses Experimental Results within Operating Region IV and Test Condition (12). 178
Figure 138 – Switch Pair S_3 and D_4 Voltage Stresses Experimental Results within Operating Region IV and Test Condition (12). 179
Figure 139 – Switch Pair S_2 and D_5 Voltage Stresses Experimental Results within Operating Region I and Test Condition (12). 180
Figure 140 – Switches Pair $S_3 - D_4$ Dead-time interval's Dynamic Voltage Sharing Experimental Results within Operating Region IV and Test Condition (12). 181
Figure 141 – Switches Pair $S_1 - D_6$ Quasi-ZVS behavior Experimental Results within Operating Region IV and Test Condition (12). 182
Figure 142 – 4LRFLCC Non-ideal Equivalent Circuit upon Transition State (11 ↑). 182
Figure 143 – 4LRFLCC Non-ideal Equivalent Circuit upon Transition State (31 ↑). 183
Figure 144 – Switches Pair $S_2 - D_5$ Quasi-ZVS behavior Experimental Results within Operating Region IV and Test Condition (12). 183
Figure 145 – 500W GaN-based 4L-RFLCC Efficiency Map as a function of Λ. 184
Figure 146 – 500W GaN-based 4L-RFLCC Efficiency Map as a function of I_{OUT}. 185

LIST OF TABLES

Table 1 – Summary of the different topological stages and their evolution. 34
Table 2 – List of Active Switches Transition Events. 49
Table 3 – Summary of the different topological stages and their characteristics for the 4LRFLC topology under Region I condition. 56
Table 4 – Summary of the different topological stages and their characteristics for the 4LRFLC topology under Region II condition. 67
Table 5 – Summary of the different topological stages and their characteristics for the 4LRFLC topology under Region III condition. 76
Table 6 – Summary of the different topological stages and their characteristics for the 4LRFLC topology under Region IV condition. 84
Table 7 – Table of Initial and Final Conditions for State Variables within Region I for Phase-Timing Definition. 87
Table 8 – Comparison between 3L-RFLCC and 4L-RFLCC under Region I of Operating condition. 90
Table 9 – Summary of the distribution of maximum peak voltage and current stresses in the Switches S_1 - S_6 under Region I condition. 90
Table 10 – Table of Initial and Final Conditions for State Variables within Region II for Phase-Timing Definition. 91
Table 11 – Summary of the distribution of maximum peak voltage and current stresses in the Switches S_1 - S_6 under Region II condition. 94
Table 12 – Table of Initial and Final Conditions for State Variables within Region III for Phase-Timing Definition. 95
Table 13 – Summary of the distribution of maximum peak voltage and current stresses in the Switches S_1 - S_6 under Region III condition. 98
Table 14 – Table of Initial and Final Conditions for State Variables within Region IV for Phase-Timing Definition. 98
Table 15 – Summary of the distribution of maximum peak voltage and current stresses in the Switches S_1 - S_6 under Region IV condition. 101
Table 16 – Summary of the Output Voltage Characteristic associated with Region I to Region IV condition. 101
Table 17 – Target 4LRFLCC Prototype Design Specifications. 105
Table 18 – Summary of the distribution of maximum peak voltage and current stresses in the Switches S_1 - S_6 under Region IV condition. 109
Table 19 – 46 AWG Wire Properties utilized for the resonant inductor construction. . . . 111
Table 20 – List of Inductor Magnetic core-based iteration based on the prototype target specification. 111
Table 21 – Resonant Capacitor's main properties for the 4L-RFLCC prototype build. . . 113

Table 22 – DC-link Capacitor's main properties for the 4L-RFLCC prototype build. . . . 114
Table 23 – Bootstrap Architecture and Component Selection for FCML converter found in the literature. 126
Table 24 – Digital Isolator and Gate Driver Architecture and Component Selection for FCML converter found in the literature. 126
Table 25 – Gate Driver Performance Attribute Comparison List Amongst different solutions. 127
Table 26 – List of Instruments for prototype testing. 133
Table 27 – List of Test Condition Sets utilized for the Operating Region and Output Voltage Regulation Validation assessment. 136
Table 28 – Operating Region II relative voltage comparison in between Counter Clock-wise and Clock-wise PWM Sequence type. 142
Table 29 – Test Condition set ⑥ Static Resonant Variables Comparison in between Theoretical and Experimental Results. 143
Table 30 – Test Condition set ⑦ and ⑧ Static Resonant Variables Comparison in between Theoretical and Experimental Results under the same Λ condition 146
Table 31 – Test Condition set ⑨ Static Resonant Variables Comparison in between Theoretical and Experimental Results. 150
Table 32 – Test Condition set ⑩ and ⑪ Static Resonant Variables Comparison in between Theoretical and Experimental Results within Operating Region IV. . 152

LIST OF ABBREVIATIONS AND ACRONYMS

AWG	American Wire Gauge
CCM	Continuous Conduction Mode
CMRR	Common-mode Rejection Ratio
DC	Direct-Current
DCM	Discontinuous Conduction Mode
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FCML	Flying-Capacitor Multi-level
FLCCC	Flying-Capacitor Commutation Cell
FOM	Figure of Merit
FSL	Fast-Switching Limit
GaN	Gallium Nitride
GD	Gate Driver
HSW	Hard-Switching
IC	Integrated-Chip
IGBT	Insulated-gate Bipolar Transistor
KVL	Kirchhoff's Voltage Law
LV	Low Voltage
MLCC	Multilayer Ceramic Capacitor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MV	Mega Voltage
PWM	Pulse-width Modulation
ReSC	Resonant Switched-Capacitor
RFLCC	Resonant Flying-Capacitor Converter
SC	Switched-Capacitor
Si	Silicon
SiC	Silicon Carbide
SSL	Slow-Switching Limit
SSW	Soft-Switching
WBG	Wide-band Gap

ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching
2L	Two-level
3L	Three-level
3L-RFLCC	Three-level Resonant Flying-Capacitor Converter
4L	Four-level
4L-RFLCC	Four-level Resonant Flying-Capacitor Converter

LIST OF SYMBOLS

N	Number of levels associated with a multi-level converter topology
A_e	Effective Core Area
$a_{\boldsymbol{x}}$	Ellipse Major-axis total length
B_s	Magnetic B field
$b_{\boldsymbol{x}}$	Ellipse Minor-axis total length
C_{ds}	Drain-to-Source Capacitor/Capacitance
C_{fly}	Flying Capacitor/Capacitance
C_{gd}	Gate-to-Drain Capacitor/Capacitance
C_{gs}	Gate-to-Source Capacitor/Capacitance
C_{IO}	Input-Output Equivalent Capacitance
C_{iss}	FET's Equivalent intrisic input capacitance
C_{oss}	FET's Equivalent intrisic output capacitance
$C_{oss,Q}$	Charge-related Equivalent output capacitance
C_{OUT}	Output Capacitor/Capacitance
C_{out}	Switches' intrisic Output Equivalent Capacitance
$C_{o.Diode}$	Diode's Equivalent Output Capacitance
$C_{o.FET}$	FET's Equivalent Output Capacitance
C_r	Resonant Flying Capacitor/Capacitance
$C_{r.eq}$	Equivalent Resonant Flying Capacitor/Capacitance
$C_{\boldsymbol{x}}$	Circle Center coordinate value
D	Duty Cycle
δ	Skin-depth
E_{oss}	C_{oss}'s stored energy as a function of v
L_d	Drain Inductor/Inductance
$L_{d_{PCB}}$	Drain PCB Parasitic Inductor/Inductance
L_g	Gate Inductor/Inductance
$L_{G_{PCB}}$	Gate-Loop PCB Parasitic Inductor/Inductance
L_{ks}	Kelvin-Source Inductor/Inductance
L_{PCB}	PCB Parasitic Inductor/Inductance
$L_{prototype}$	Measured Resonant inductor/inductance value

L_r	Resonant Inductor/Inductance
L_s	Power-Source Inductor/Inductance
$L_{s_{PCB}}$	Power-Source PCB Parasitic Inductor/Inductance
f_{SW}	Switching Frequency in Hz
f_0	Z_r-related Resonant Frequency in Hz
I_{C0}	Capacitor's Initial Current Condition in Amps
$i_{C_{fly}}(t)$	Instantaneous Flying-capacitor's current value
$i_{C_r}(t)$	Instantaneous Resonant Flying-capacitor's current value
$\overline{i_{C_r}(t)}$	Normalized Instantaneous Resonant Flying-capacitor's voltage value in reference to $\frac{Z_r}{V_{IN}}$.
$\overline{\overline{i_{C_r}(t)}}$	Normalized Instantaneous Resonant Flying-capacitor's voltage value in reference to $\frac{Z_{r_2}}{V_{IN}}$.
$\overline{\overline{\overline{i_{C_r}(t)}}}$	Normalized Instantaneous Resonant Flying-capacitor's voltage value in reference to $\frac{Z_{r_1}}{V_{IN}}$.
$MAX\left(\overline{I_{C_{r_n}}}\right)$	Maximum Resonant Capacitor **n**'s peak current value
$i_{L_r}(t)$	Instantaneous Resonant Inductor's current value
$\overline{i_{L_r}(t)}$	Normalized Instantaneous Resonant Inductor's voltage value in reference to $\frac{Z_r}{V_{IN}}$.
$\overline{\overline{i_{L_r}(t)}}$	Normalized Instantaneous Resonant Inductor's voltage value in reference to $\frac{Z_{r_2}}{V_{IN}}$.
$\overline{\overline{\overline{i_{L_r}(t)}}}$	Normalized Instantaneous Resonant Inductor's voltage value in reference to $\frac{Z_{r_1}}{V_{IN}}$.
I_{IN}	Average Input current value
$i_{OUT}(t)$	Instantaneous Output load current value
I_{OUT}	Average Output load current value
I_p	Peak Current thru the Magnetic component
I_1	Hard-switched Switching Current value
μ_r	Material relative magnetic permeability
ω_0	Z_r-related Resonant Velocity in $\frac{rad}{s}$
ω_1	Z_{r_1}-related Resonant Velocity in $\frac{rad}{s}$

ω_2	Z_{r_2}-related Resonant Velocity in $\frac{rad}{s}$
P_{DRV}	Total Gate-related Power consumption
P_{dt}	Dead-time-related conduction loss
P_G	Gate C_{iss} loss
P_{oss}	Output-capacitance C_{oss} loss
P_{rr}	Reverse-recovery loss
P_{vi}	Voltage-Current Overlap-related loss
Q_C	Diode's Capacitive Charge
$Q_{GD.tot}$	Total Gate Charge
Q_{oss}	C_{oss}'s stored charge as a function of v
R_{OUT}	Output Load Impedance/Resistance in Ω
R_{ON}	Device's ON-resistance
$r_{\boldsymbol{x}}$	Circle radius value
ρ	Material conductivity coefficient
$S_{\boldsymbol{x}}$	Switch
T_j	Junction Temperature
ΔT_{XYZ}	Interval's Time duration from **Y** to **X** within Operating Condition **Z**
τ_{rr}	Reverse-recovery-related coefficient
V_{C0}	Capacitor's Initial Voltage Condition in Volts
$v_{C_{fly}}(t)$	Instantaneous Flying-capacitor's voltage value
$v_{C_r}(t)$	Instantaneous Resonant Flying-capacitor's voltage value
$\overline{v_{C_r}(t)}$	Normalized Instantaneous Resonant Flying-capacitor's voltage value in reference to V_{IN}.
$MAX\left(\overline{V_{C_{rn}}}\right)$	Maximum Resonant Capacitor **n**'s peak voltage value
V_{DRV}	Gate Driver Voltage
V_{DM}	DC Differential Voltage in reference to V_1 and V_2 in Volts
V_{DS}	Drain-to-Source Voltage
V_F	Diode's Forward Voltage Drop
$V_{GS.OFF}$	Turn-OFF Gate-to-Source Voltage
$v_{L_r}(t)$	Instantaneous Resonant Inductor's voltage value
v_{IN}	Input Voltage in Volts

v_{OUT}	Output Voltage in Volts
V_{SD}	Reverse conduction Source-to-Drain Voltage Drop
V_1	DC Plus-Differential Voltage in Volts
V_2	DC Minus-Differential Voltage in Volts
Z_r	Characteristic Impedance

CONTENTS

1 INTRODUCTION . . . 26
1.1 CONTEXTUALIZATION AND LITERATURE REVIEW . . . 26
1.2 MOTIVATION . . . 33
1.2.1 Operation Principle . . . 33
1.2.2 Thesis Outline . . . 35
2 LC-NETWORK GENERAL DESCRIPTION . . . 37
2.1 CASE 1 - LC SERIES RESONANCE . . . 37
2.2 CASE 2 - LCCP SERIES RESONANCE . . . 40
2.3 CASE 3 - LCCS SERIES RESONANCE . . . 44
3 4L-RFLC BOOST CONVERTER DESCRIPTION . . . 48
3.1 MODULATION STRATEGY . . . 48
3.2 REGION I . . . 49
3.2.1 Interval I ($t_0 < t < t_1$) . . . 49
3.2.2 Interval II ($t_1 < t < t_2$) . . . 51
3.2.3 Interval III ($t_2 < t < t_3$) . . . 52
3.2.4 Interval IV ($t_3 < t < t_4$) . . . 52
3.2.5 Interval V ($t_4 < t < t_5$) . . . 53
3.2.6 Interval VI ($t_5 < t < t_6$) . . . 54
3.2.7 Interval VII ($t_6 < t < t_7$) . . . 54
3.2.8 Interval VIII ($t_7 < t < t_8$) . . . 55
3.2.9 Interval IX ($t_8 < t < t_9$) . . . 56
3.2.10 Summary of Operation . . . 56
3.3 REGION II . . . 58
3.3.1 Interval I ($t_0 < t < t_1$) . . . 58
3.3.2 Interval II ($t_1 < t < t_2$) . . . 60
3.3.3 Interval III ($t_2 < t < t_3$) . . . 60
3.3.4 Interval IV ($t_3 < t < t_4$) . . . 62
3.3.5 Interval V ($t_4 < t < t_5$) . . . 63
3.3.6 Interval VI ($t_5 < t < t_6$) . . . 64
3.3.7 Interval VII ($t_6 < t < t_7$) . . . 65
3.3.8 Interval VIII ($t_7 < t < t_8$) . . . 67
3.3.9 Summary of Operation . . . 67
3.4 REGION III . . . 69
3.4.1 Interval I ($t_0 < t < t_1$) . . . 69
3.4.2 Interval II ($t_1 < t < t_2$) . . . 70

3.4.3 **Interval III** ($t_2 < t < t_3$) **71**
3.4.4 **Interval IV** ($t_3 < t < t_4$) **72**
3.4.5 **Interval V** ($t_4 < t < t_5$) **73**
3.4.6 **Interval VI** ($t_5 < t < t_6$) **73**
3.4.7 **Interval VII** ($t_6 < t < t_7$) **75**
3.4.8 **Summary of Operation** **76**
3.5 REGION IV **78**
3.5.1 **Interval I** ($t_0 < t < t_1$) **78**
3.5.2 **Interval II** ($t_1 < t < t_2$) **79**
3.5.3 **Interval III** ($t_2 < t < t_3$) **79**
3.5.4 **Interval IV** ($t_3 < t < t_4$) **82**
3.5.5 **Interval V** ($t_4 < t < t_5$) **82**
3.5.6 **Interval VI** ($t_5 < t < t_6$) **83**
3.5.7 **Summary of Operation** **83**
4 **STATIC GAIN & LARGE-SIGNAL ANALYSIS** **86**
4.0.1 **Region I** **86**
4.0.2 **Region II** **90**
4.0.3 **Region III** **93**
4.0.4 **Region IV** **97**
4.0.5 **Large-Signal Analysis Summary** **100**
5 **PROTOTYPE DESIGN & COMPONENT SELECTION** **105**
5.0.1 **Project Specification & Design Methodology** **105**
5.0.2 **Component Stresses** **106**
5.0.3 **Resonant inductor L_r** **108**
5.0.4 **Resonant flying capacitors C_{r1} and C_{r2} & DC-link Capacitors** **111**
5.0.5 **Active Switches $S_1 - S_6$** **114**
5.0.6 **Gate Driver & Auxiliary Circuitries** **122**
5.0.7 **PCB Design** **127**
6 **EXPERIMENTAL RESULTS AND VALIDATION** **132**
6.0.1 **Operating Region & Output Voltage Regulation** **132**
6.0.2 **Switches $S_1 - S_6$'s Voltage Stresses** **151**
6.0.3 **Efficiency Map** **184**
7 **CONCLUSIONS** **186**
BIBLIOGRAPHY **189**

1 INTRODUCTION

1.1 CONTEXTUALIZATION AND LITERATURE REVIEW

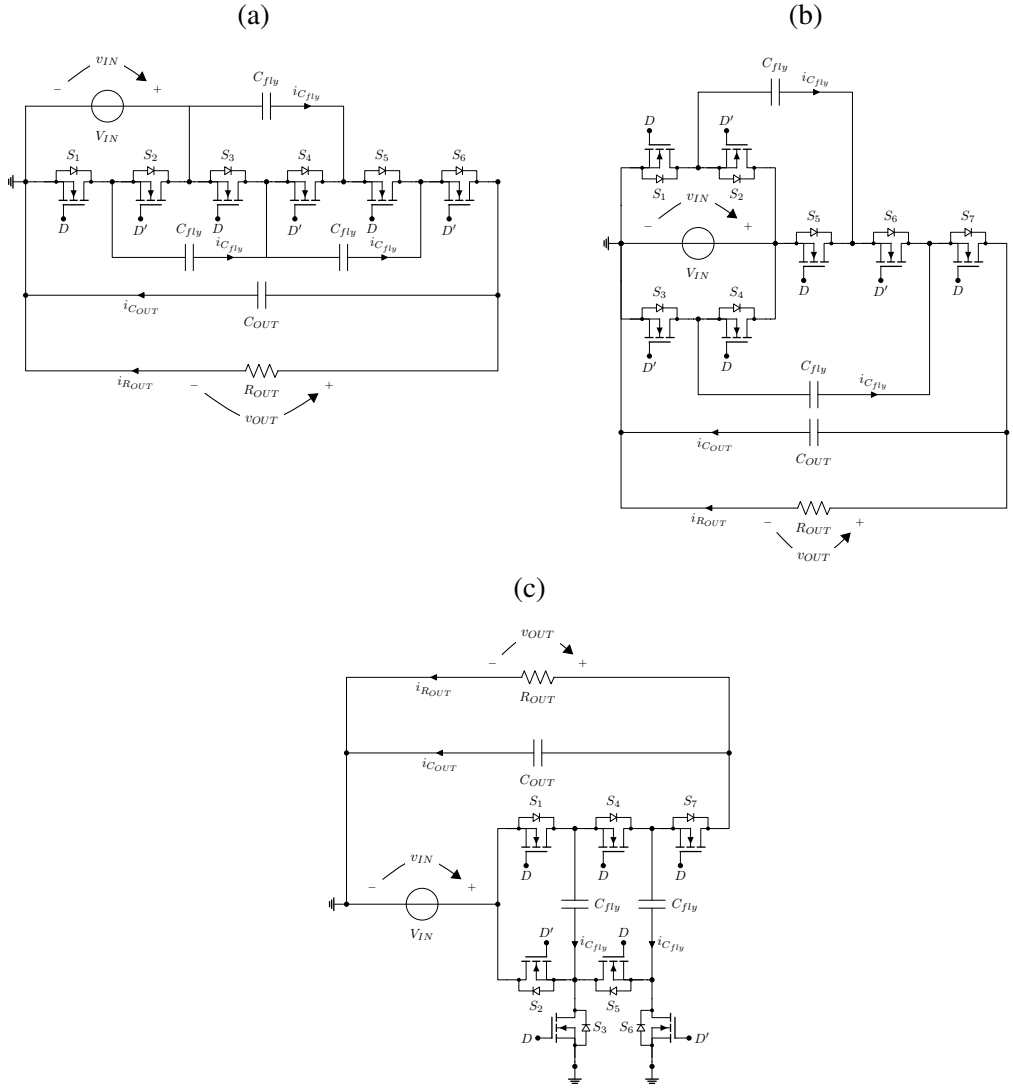
DC-DC Step-up and Step-down power conversion have been extensively utilized over the years in a broad range of applications from DC distribution networks [Zhang et al. 2016], where voltages are required to step-down from MV to LV (400V or 380V) levels, to renewable energy system, to lower voltage applications such as datacenters and telecommunication [Ye, Lei e Pilawa-Podgurski 2018] and low-voltage digital circuitry [Pilawa-Podgurski, Giuliano e Perreault 2008] [Pilawa-Podgurski e Perreault 2012], where the conversion ratio and output current requirements are usually high. As a consequence, high efficiency and high power density converters become important in order to achieve a high level of sustainability.

In order to fulfill such requirements, either multi-stage conversion have been widely employed, in order to overcome the poor performance of conventional buck-like or boost-like converters operating with a large conversion ratio, or isolated DC-DC converters, due to their ability of increasing the conversion ratio based on a magnetically coupling component to support the large conversion ratio [Zhang et al. 2016] [Vasic et al. 2019]. Even though multi-stage conversion architectures can potentially achieve good levels of power density and compactness [Vasic et al. 2019], the additional stages generally require bulky energy storage elements either to provide the intermediate voltage stabilization or to support the conversion such as a conventional 2L buck-like or boost-like converter's Volt-Second balance in an inductor.

Due to these distinct conditions, multilevel converters have been addressed in order to optimize the system's performance due to its ability to deliver a higher conversion ratio, lower Volt-Second balance in inductors, in case of magnetic-type converter, as well as the feasibility to utilize lower voltage switches [Brooks et al. 2022] which leads to better figure-of-merits (FoM) compared to high voltage switches. Amongst the different structures that are defined as multilevel converters, Switched-capacitor converters, as shown in Figure 1, have been widely utilized due to their key benefits such as the magnetic-less characteristic and possibility to fulfill a particular fixed voltage gain requirement in comparison to their natural counter-parts such as conventional buck or boost converters. Such characteristics generally lead to higher power density and small component count. On the other hand, due to the magnetic-less characteristic, large current spikes are experienced due to the charging/discharging process of the intermediate capacitors [Shoyama, Naka e Ninomiya 2004] and, consequently, lower efficiency is achievable. Therefore, such topology becomes limited to lower output current and/or lower input voltage applications. The Switched-capacitor converter types, shown in Figure 1, can be expanded to N levels, which leads to a higher output voltage gain. However, their applicability has practical limits in order to introduce a N voltage gain due to the input current flowing through N switching devices. As a consequence, introducing further losses and reducing the efficiency.

Different switched-capacitor topologies have been introduced such as the Ladder-type, Dickson, Fibonacci, Series-Parallel and Doubler. Each of these topologies have its benefits and

Figure 1 – Representation of the Base form of different DC-DC Switched-Capacitor, such as: (a) Ladder SC Converter. (b) Dickson SC Converter. (c) Fibonacci SC Converter.



drawbacks. The ladder-type, as shown in Figure 1a, is based on a set of capacitors establishing the DC potentials referred to the ground reference and a set of capacitors establishing the equalization amongst the DC-referenced capacitors [Seeman 2009]. The basic pulse-width modulation strategy is by driving the odd-numbered switches complementary to the even-numbered switches. The ladder-type is also suitable for non-integer voltage gains based on the position of the input voltage connection with reference to the ground. As a consequence, depending on the number of levels, the low-side components are the most stressed whereas the high-side devices are locally stressed based on the charging and discharging process. This behaviour leads to an unbalance in the current stresses making it not well suitable for high conversion ratio and high current applications.

In order to improve the unbalance in the current stresses, shown in the Ladder-type SC converter, the Dickson SC converter has been introduced, as shown in Figure 1b, by introducing phase-shifted ladder commutation cells. Therefore, by driving the two low-side bridge-legs

complementary as well as the high-side switches in a similar fashion as in the Ladder-type, the current stresses in the low-side switches are distributed accordingly whereas the current stresses in the high-side switches remain the same as shown in the Ladder-type SC converter. As a consequence, the Dickson SC converter becomes more suitable for slightly higher conversion ratio and higher current and applications. On the other hand, by introducing the phase-shifted ladder, the voltage stresses in the flying capacitors are no longer equal due to the phase-shifted ladder connection point; thus, leading to an unbalance in the voltage stresses in the switches during the OFF-state.

Alternatively, the Fibonacci SC converter has been introduced, as shown in Figure 1c, by applying cascaded three switches and 1 flying capacitor commutation cell. Differently from the other SC converters, the conversion ratio is given by the Fibonacci sequence. Therefore, a higher conversion ratio is achieved on a smaller component count compared to the Ladder and Dickson SC converters. As a consequence, higher efficiencies are achieved. On the other hand, similarly to the Ladder SC converter and the Dickson SC converter, there exist a progressive unbalance in the current stresses for the switches, based on the commutation cell position, and a unbalance in the voltage stresses in the active switches and passive components, respectively.

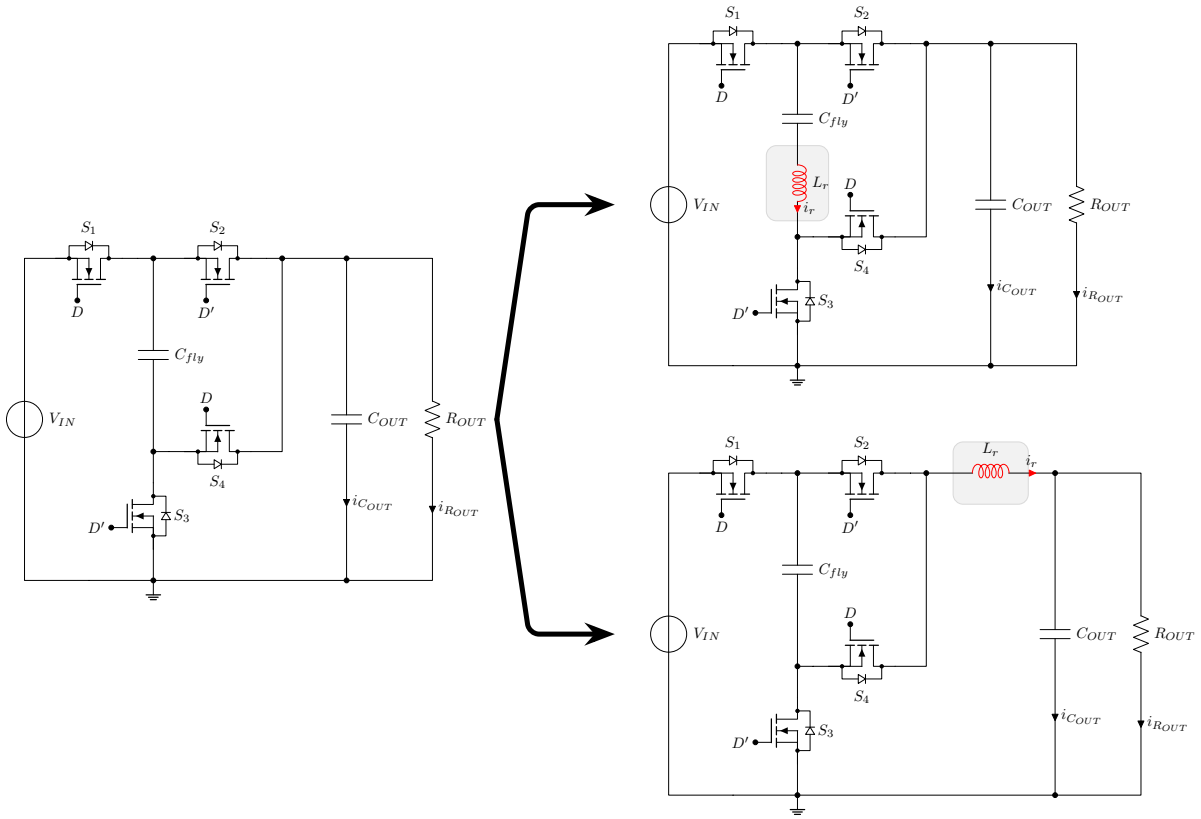
Driven by the main characteristics for each SC converter, [Seeman 2009] [Seeman e Sanders 2008] derives the Slow-Switching Limit (SSL) and Fast-Switching Limit (FSL) impedance analysis in order to compare the different topologies based upon the capacitive energy losses and the resistive elements energy losses, respectively.

Due to the excessive forced charging and discharging process, there exist an inherent drawback on the losses introduced by the switched capacitors as well as increase the device stresses [Lei e Pilawa-Podgurski 2015]. Thus, the efficiency becomes limited regardless of the internal resistance minimization [Shoyama, Naka e Ninomiya 2004] [Shoyama, Deriha e Ninomiya 2005]. Additionally, due to its hard-switched pulse-width modulation operation, it introduces further limitations in terms of high-frequency applications by increasing the switching losses [Li et al. 2017] and causing undesirable electromagnetic interference problems, which are solved by either increasing the switching frequency or employing larger switched capacitors [Lei e Pilawa-Podgurski 2015].

In order to reduce the current stresses and the forced charging/discharging process energy losses, an additional inductive element is introduced with the capacity of limiting the charging and discharging current of the intermediate capacitors, Such structure is named Hybrid Switched-capacitor converter. Thus, potentially increasing the converter's efficiency. Additionally, it also introduces the possibility of regulating the voltage gain, releasing the pressure of the input voltage requirement in order to fulfill a particular output voltage. However, the introduction of the inductive element naturally decreases the power density, becoming less suitable for high power density applications. Resonant switched-capacitor converters, as shown in Figure 2, have been a research interest due to its benefits such as high power-density and soft-switching capability while delivering a constant voltage gain and limiting the main drawback of conventional switched-

capacitor converter.

Figure 2 – Representation of different approaches for the realization of resonant switched-capacitor converter (ReSCC).



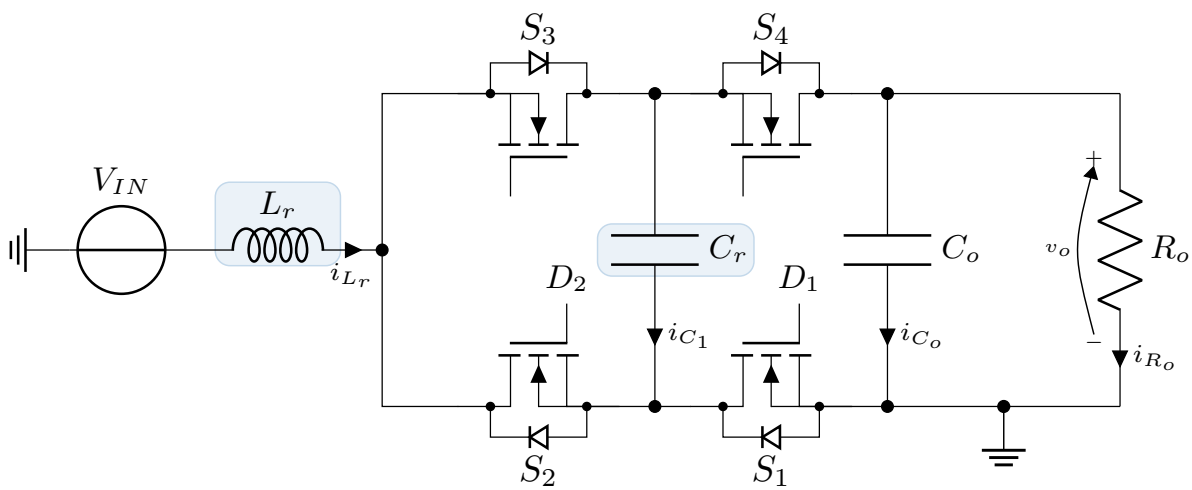
The resonant type employs small inductors and capacitors, in opposition to the bulky intermediate capacitors employed in conventional switched-capacitor converters, due to the voltage mismatching in between the intermediate capacitors being present across the inductors instead of the internal resistance of the active switches [Ye, Lei e Pilawa-Podgurski 2020]. Thus, enabling the utilization of smaller capacitors and bigger voltage ripples without sacrificing the system's efficiency. The small inductor and capacitor create a resonant behaviour based on the Active switches' status. As a consequence, the charging/discharging process is based on the resonance frequency and soft-switching can be achieved by exploring the switching frequency control as well as the phase-shift [Setiadi e Fujita 2016] [Sano e Fujita 2011] mechanism based on the modulation strategy employed by the converter.

Due to the limited voltage gain characteristic, additional conversion stages [Ye, Lei e Pilawa-Podgurski 2020] [Ye, Lei e Pilawa-Podgurski 2018] can be introduced in order to increase the voltage gain. The cascaded stages employ basic 2:1 switched-capacitor converter in series in order to achieve the desired output voltage gain. The main benefit is the simple resonant activity, due to the individual stages operation. On the other hand, this strategy leads to incremental voltage stresses in the upstream cascade converters and the utilization of intermediate bus capacitors in order to decouple the resonance in between the adjacent cascaded converters.

Different cascaded topologies [Lei e Pilawa-Podgurski 2015] explore the characteristics of switched-capacitor converter followed by conventional buck converters [Pilawa-Podgurski, Giuliano e Perreault 2008] with high switching frequency and high bandwidth due to its output current characteristic which then eliminates the need of bulky bus capacitors. Therefore, these architectures can be considered as merged-cascaded stages and improves the power density of the power conversion stage. Many different authors have explored the basic switched-capacitor architectures in order to reduce the components' stresses as well as the component count.

Alternatively, the flying capacitor multilevel converter, as shown in Figure 3, has also become attractive for similar applications, due to its component stresses' characteristics as well as its ability to regulate the output voltage. Likewise the switched-capacitor topologies, the flying capacitor topology can also be operated in resonant mode. Thus, bringing the similar benefits as discussed previously.

Figure 3 – Basic Structure for a 3L flying capacitor boost DC-DC converter.



Cascaded topologies have also been addressed in resonant mode [Ye, Lei e Pilawa-Podgurski 2018], and also where the essence is to minimize the resonant tank design complexity, as demonstrated by [Liu, Ge e Pilawa-Podgurski 2022], in which the resultant energy transfer is based on an interaction in between the two adjacent stages. Due to that, the filter, in between the stages, can be simplified, in comparison to [Ye, Lei e Pilawa-Podgurski 2018] where the intermediate filter is required to sustain an intermediate voltage level for the adjacent conversion stage. Alternatively, cascaded topologies have been explored with virtual intermediate voltage buses [Chen et al. 2022] [Zhu et al. 2024], where the first stage is essentially a switched capacitor, employing the conventional hard-charging mechanism as observed in non-resonant switched-capacitor converters, whereas [Ge, Ye e Pilawa-Podgurski 2023] addresses a similar mechanism except that the virtual intermediate bus is converted into a switching virtual bus, in which the advantages become the small-sized bus, the ability to increase the step-down conversion ratio, and the opportunity of exploring the virtual bus as part of the resonant energy-transfer mechanism in the adjacent conversion stage. As a consequence, the cascaded total resonant tank is greatly

reduced. On the other hand, due to the primary-stage's charge-pump behavior, there exist a high-current stresses in order to enable the switching bus mechanism.

The ability of the above-mentioned converters to greatly increase the power density is also driven by the passive components volume given the objective of defining the characteristic impedance to balance, and optimize, the energy utilization of the resonant tank components, such as the resonant inductor and resonant capacitor [Ye, Sanders e Pilawa-Podgurski 2019] [Ellis et al. 2024]. [Ye, Sanders e Pilawa-Podgurski 2019] addresses this issue by defining the energy utilization and comparing the characteristic impedance of different switched capacitors, operating in resonant mode, amongst which the FCML is further analyzed. By utilizing the energy processed by the capacitor and the inductor, the energy utilization refers to the amount of energy transfer per peak energy. In other words, it addresses the total voltage ripple, and current ripple, within the resonant capacitor and resonant inductor, respectively. From a different perspective, [Zhu, Ye e Pilawa-Podgurski 2024] addresses the switched-capacitor performance based on finite input and output capacitances. It expands the SSL and FSL by considering the impact of the charge/discharge of the output and input capacitors as a forced charging/discharging process in which it has been found that the capacitance ratio with respect to the flying capacitor impacts the performance, leading to a higher bus capacitance total volume requirements. The same analysis has not been performed for resonant-type converters. However, it could be expected the interference of the input and output capacitor into the conversion ratio, as well as in the ability of soft-switching, due to the higher sensibility of the operating mechanism as a result of a shift in the resonant frequency.

On the contrary, [Abramson et al. 2022] [Brooks et al. 2022] define a conduction mode factor, which describes the converter's operating condition with respect to the fundamental switching frequency and the resultant resonance frequency given the number of FLCCC stages, in order to derive an optimization function based on the conduction mode. The analysis focus on operations at and above resonance, where the converter operates either synchronously with the switching frequency; thus, achieving ZCS at every Switches State Transition; or intentionally increasing the conduction mode factor in order to reduce the current stresses, while retaining the resonant behavior within each FLCCC. The later leads to non-ZCS, introducing switching losses at the turn-OFF and turn-ON transition of the complementary switches. Based on the conduction mode factor, the charge associated with each flying capacitor is derived, exhibiting an optimum operating condition, where the conduction losses and switching losses are balanced. Although ZVS cannot be achieved for every Switch, a ZVS cross-conduction time is introduced [Ge et al. 2021] [Ge, Ye e Pilawa-Podgurski 2023] in order to achieve ZVS, where every Low-side Switches are simultaneously ON, imposing a high negative voltage across the inductor. As a result, the inductor's current falls linearly during this phase and introduces a ZCS for the complementary High-side Switches, greatly improving the converter's performance. Similarly, the Low-side Switches can also achieve by sufficiently increasing the inductor's current above zero. Yet, the non-ZVS Switches achieve ZCS, which is beneficial for high-current applications [Ge, Ye e

Pilawa-Podgurski 2023], despite of the C_{out}-associated losses.

Operating under resonance leads to ZCS for every Switch. However, it inhibits the ZVS transition and the associated C_{out} losses, possibly imposing limitation to the system's operating frequency. Yet, depending on the number of FLCCC, the switching voltage becomes small, leading to an acceptable C_{out} loss figures. Low-voltage applications, as demonstrated in the various papers above-mentioned, the C_{out} losses may not be very critical, instead, the high-current requirements becomes important, where Si MOSFETs remain competitive. For high-voltage applications, C_{out} losses are non-negligible and WBG devices introduces a degree of freedom in order to keep pushing the boundaries of power density by increasing the operating frequency and minimizing the resonant tank volume.

The majority of the past, and recent, work have explored the flying capacitor resonant converter as a non-regulated step-up or step-down converter with a given characteristic of constant voltage gain under the right operating conditions, such as the high characteristic impedance. Such characteristic leads to a constant voltage gain under a very wide load range, with the cost of having a larger resonant tank, becoming suitable for many different applications. Similarly, the same topology has been explored as a voltage gain multiplier/divider as a result of specific PWM strategies.

Due to the sinusoidal shape, the frequency-dependent state variables' description, which enables the optimization objects described previously, becomes more complex. Recent works have explored different methods of analytically solving for the unknown variables. [Ellis et al. 2024] [Ye, Sanders e Pilawa-Podgurski 2019] exploits the energy processed, in which [Ellis et al. 2024] [Brooks et al. 2022] emphasizes the conduction timings per phase as a consequence of the multi-resonance characteristic. The description aids the phase timings in order to accurately change the Switches State in order to fulfill the output requirements. The only drawback is the RFLCC operating condition, which is focused on either at resonance or above resonance, leading to a simplified frequency-dependent unknown variables, where the sinusoidal shape exhibits a symmetrical behavior in terms of initial and final condition within each phase. Similarly, [Ellis e Amirtharajah 2022] addresses the phase timings, for a Dickson-type switched-capacitor converter, in order to maintain a zero voltage-seconds across the inductor, based on the Kirchhoff's Voltage Law (KVL) for each topological stage where an average and ripple voltage level are considered as unknown variables. Based on the charge transfer, the unknown variables can be analytically solved.

Alternatively, due to the sinusoidal shape, a geometrical representation exhibits an advantage over purely analytical solutions due to the possibility of representing the sinusoidal shape by geometrical forms, such as circles and ellipses, and exploring the geometry rules. [Oruganti e Lee 1985] pioneered the State Plane Analysis, which became very popular specially for LLC converter application [Feng, Lee e Mattavelli 2013] [Vuchev e Grigorova 2021] [Rezayati et al. 2022] due to the possibility of increasing the output voltage regulation's bandwidth despite of the increased mathematical computational power demand. The same approach is taken in

non-isolated resonant converters [Shuai et al. 2010] [Setiadi e Fujita 2016] for a single LC resonant network. The resultant representation exhibits a circular trajectory, leading to a very comprehensive analysis with explicit radius and center to aid with the problem solving. [Setiadi e Fujita 2016] demonstrates the phase timing determination, which results in a similar result as described in [Ellis et al. 2024]. However, the approach, shown in [Setiadi e Fujita 2016], is limited due to the single LC resonant network and simple description, lacking the coverage to multi-resonant converters.

The multi-resonant characteristic introduces further complexity in the geometrical representation. As demonstrated in [Ge, Ye e Pilawa-Podgurski 2023], multiple interconnection amongst different passive elements possesses challenges by introducing different geometrical forms. As a consequence, [Ge, Ye e Pilawa-Podgurski 2023] suggests the individual representation, under each equivalent resonant tank framework, and the topological stages link as per the equilibrium states. As a consequence, it avoids the utilization of elliptical geometries as part of the problem solving.

1.2 MOTIVATION

In a similar fashion, [Shuai et al. 2010] proposed a unidirectional 3L resonant flying capacitor boost converter, where the same commutation cell can be used, as shown in Figure 3, in which a bidirectional version is exhibited. Thus, introducing no further components but perceiving the inductor L_r and capacitor C_r in a different manner. In the resonant-mode, L_r and C_r affect the static gain, depending on the operating switching frequency f_{sw} and output load conditions, simplified as a resistive element R_{OUT}. Thus, the 3L-RFLCC topology can also be explored to regulate the output voltage as a function of the switching frequency f_{sw}.

1.2.1 Operation Principle

For the sake of describing the operation of the 3L resonant flying capacitor boost converter, the Output Capacitor C_{OUT} is assumed to be big enough. Thus, the Output Voltage V_{OUT} is considered constant within the different topological stages. The switches S_1 and S_2 are actively switching complementary to each other, and constant 50% duty cycle, whereas the switches S_3 and S_4 are passively switching.

Aimed at exploring fully the resonant capability, the converter, shown in the Figure 3, operates at a Switching Frequency f_{sw} always below the Resonant Frequency f_o.

The Figure 4 represents the equivalent circuit and the Table 1 represents the main attributes within the different topological stages, in a sequential order. The third column, called as L_r and C_r State, represents the evolution of the charge/discharge of the resonant elements. By that, $\nearrow$ represents that the element is mainly charged, and $\searrow$ represents that the element is mainly discharged.

Figure 4 – 3L resonant flying capacitor equivalent circuit for: (a) 1st Topological Stage. (b) 2nd and 5th Topological Stage. (c) 4th Topological Stage.

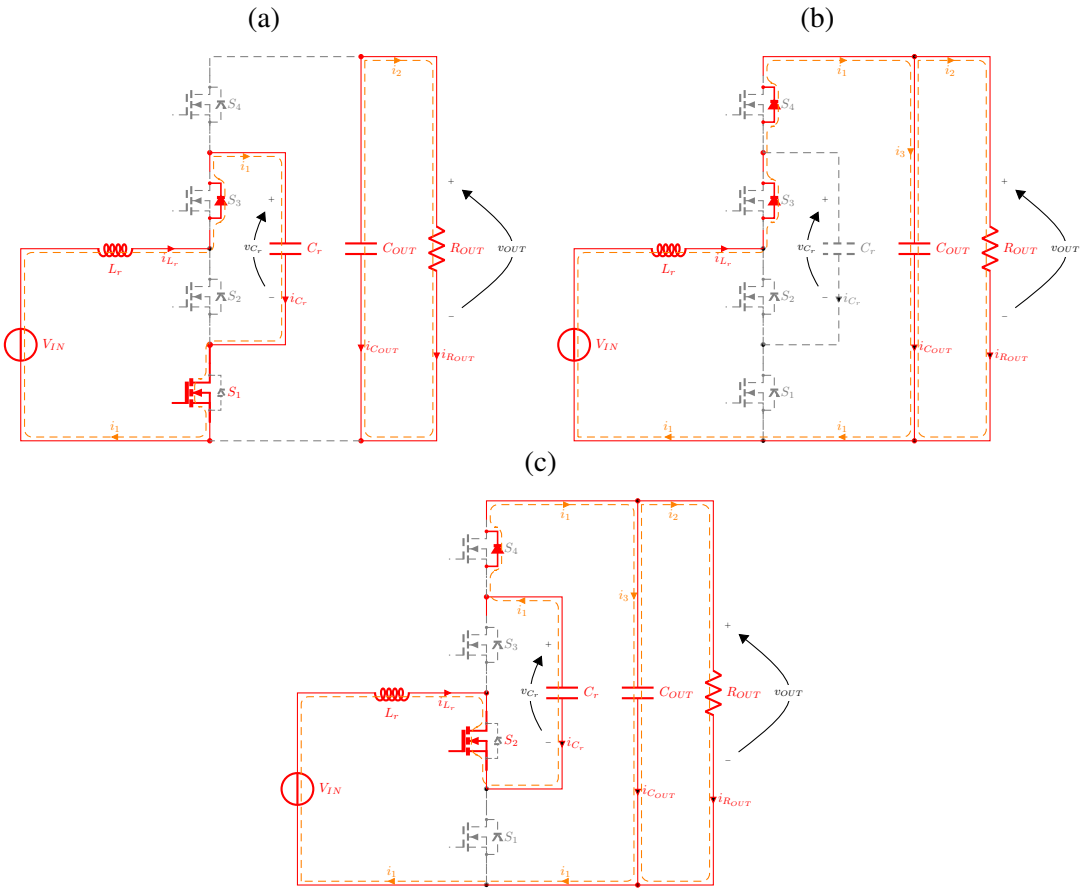


Table 1 – Summary of the different topological stages and their evolution.

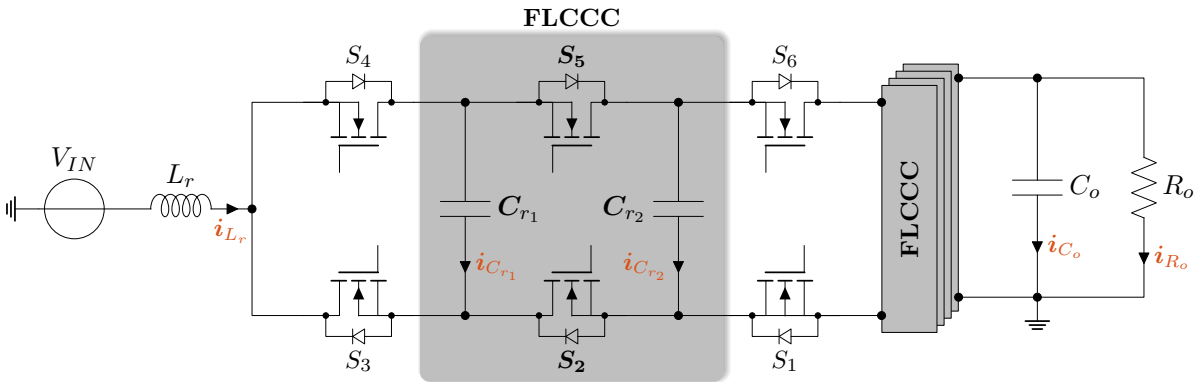
Topological Stage	**Switches State**		**L_r and C_r State**		**Operating Mode**	**State Plane**
	S_1	S_2	L_r	C_{r1}		z_{n1}
1st	ON	OFF	$\nearrow$	$\nearrow$	Resonant ω_0	$1-e^{-j\cdot\omega_o\cdot t}$
2nd	ON	OFF	$\searrow$	$\rightarrow$	Linear	$G+j\cdot\left[\overline{I_1}-(G-1)\cdot\omega_o\cdot(t-t_1)\right]$
3rd	ON	OFF	$\rightarrow$	$\rightarrow$	Idle	G
4th	OFF	ON	$\nearrow$	$\searrow$	Resonant ω_0	$G-1-e^{-j\cdot\omega_o\cdot t}$
5th	OFF	ON	$\searrow$	$\rightarrow$	Linear	$j\cdot\left[\overline{I_1}-(G-1)\cdot\omega_o\cdot(t-t_4)\right]$
6th	OFF	ON	$\rightarrow$	$\rightarrow$	*Idle*	0

The fifth column, called as Analytical Form, represents the description of each topological state, in a normalized form, in which the resonant inductor current i_{L_r} and the resonant capacitor voltage v_{C_r} are normalized.

1.2.2 Thesis Outline

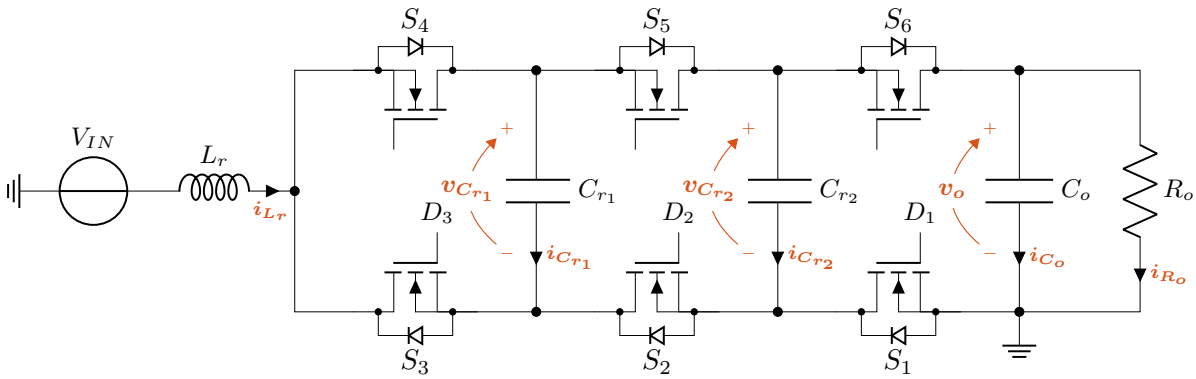
With the purpose of exploiting the potential of flying capacitor commutation cells, whilst the output voltage range becomes wider, and maintaining the component level count to a reasonable level, this work proposes an extension of the 3L resonant flying capacitor topology by introducing multilevels of resonant flying capacitor's commutation cell. The Figure 5 represents a generic n-levels resonant flying capacitor topology.

Figure 5 – Generic Structure for a n-level resonant flying capacitor boost DC-DC converter.



Despite of the possible generalization for n-levels, this thesis will primarily focus on the realization, description, and analyzes of a 4L-RFLC unidirectional DC-DC boost converter. Figure 6 shows the proposed 4L-Resonant Flying Capacitor DC-DC converter, which consists of six switches S_1 - S_6, one resonant inductor L_r, and two resonant capacitors C_{r_1} and C_{r_2} as well as one Output Capacitor C_o. The converter operates similarly as the 3L-RFLCC, referred in the 1.2.1. Depending on the switching state, the resonant elements will charge and discharge with a sinusoidal shape.

Figure 6 – Proposed Converter Circuit Topology.



Therefore, in order to address this problem, the first chapter will focus on a general description of different LC resonant tank, and their analytical and geometrical representation, which will aid in the unknown state variable resolution described in the second chapter. The Second Chapter will focus on the theoretical assessment of the proposed 4L-RFLCC, solving the state variables and characterizing the proposed 4L-RFLCC based on its frequency-dependent

characteristic, under different operating conditions. Within the same chapter, the component stresses will be addressed and described in order to compare possible different design choices and specification targets. Finally, the Third and Fourth Chapter will address the prototype design and validation, respectively. The final chapter will consist of the conclusions, observations and possible next steps as follow-up activities.

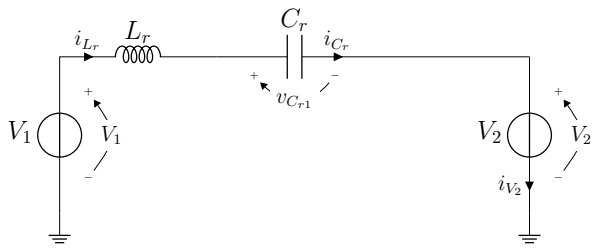
2 LC-NETWORK GENERAL DESCRIPTION

As observed previously, the primary mechanism of energy transfer, in a resonant converter, is generalized by a resonant activity in between at least one inductor and one capacitor, upon a single-ended or differential-mode excitation. This chapter addresses a general description of three different LC-networks, in which the proposed 4L-RFLCC exhibits within its operating behavior. The Series Resonance description has been described in details in [Barbi 2019] while this section expands the description with the generalized form considering the series and parallel connections of C_r, and a decomposition a charging and discharging scenario for the capacitor with an unknown initial voltage V_{C0} and initial current I_{C0} conditions where red and blue signs correspond to the resultant charging and discharging scenario for each individual capacitor.

2.1 CASE 1 - LC SERIES RESONANCE

The 1st case is comprised of a series resonance, based on a resonant inductor L_r and a resonant capacitor C_r connected in series upon a non-zero excitation step voltage, as shown in Figure 7.

Figure 7 – Generic Series Resonance LC Equivalent Circuit with a Differential-mode Voltage Excitation Signal.



Based on KVL, Equation (2.1) exhibits the sum of every voltage across the equivalent circuit loop, shown in Figure 7.

$$-V_1 + v_{L_r}(t) \pm v_{C_r}(t) + V_2 = 0 \tag{2.1}$$

Based on the definition of capacitor and inductor, (2.2) and (2.3) are derived.

$$i_{C_r}(t) = C_r \cdot \frac{dv_{C_r}(t)}{dt} = \pm i_{L_r}(t) \tag{2.2}$$

$$v_{L_r}(t) = L_r \cdot \frac{di_{L_r}(t)}{dt} \tag{2.3}$$

In order to facilitate the manipulations, Equation (2.4) is defined.

$$V_{DM} = V_1 - V_2 \tag{2.4}$$

By applying (2.2), (2.3) and (2.4) into (2.1), Equation (2.5) is derived.

$$L_r C_r \cdot \frac{d^2 v_{C_r}(t)}{dt^2} + v_{C_r}(t) = \pm\left(V_1 - V_2\right) = \pm V_{DM} \tag{2.5}$$

and perfoming a Laplace Transformation, Equation (2.6) is derived.

$$L_r C_r \cdot \left(s^2 V_{C_r}(s) - s v_{C_r}(0) - v_{C_r}\prime(0)\right) + V_{C_r}(s) = \pm\frac{1}{s} \cdot V_{DM} \tag{2.6}$$

The resonant capacitor C_r's initial conditions are described as shown in Equation (2.7) and (2.8).

$$v_{C_r}(0) = V_{C0} \tag{2.7}$$

$$v_{C_r}\prime(0) = \pm\frac{i_{C_r}(0)}{C_r} = \pm\frac{I_{C0}}{C_r} \tag{2.8}$$

By applying (2.7) and (2.8) into (2.6), the Equation (2.9) exhibits the final LaPlace representation.

$$V_{C_r}(s) = \pm\frac{1}{s} \cdot V_{DM} - (\pm V_{DM} - V_{C0}) \cdot \frac{s}{s^2 + {\omega_0}^2} \pm Z_r I_{C0} \cdot \frac{\omega_0}{s^2 + {\omega_0}^2} \tag{2.9}$$

where Z_r and ω_0 are defined as shown in Equation (2.10) and (2.11), respectively.

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{2.10}$$

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \tag{2.11}$$

By applying the inverse Laplace transformation in (2.9), the resonant capacitor C_r's voltage is described as shown in Equation (2.12).

$$v_{C_r}(t) = \pm V_{DM} - (\pm V_{DM} - V_{C0}) \cdot \cos(\omega_0 t) \pm Z_r I_{C0} \cdot \sin(\omega_0 t) \tag{2.12}$$

By applying (2.12) into (2.2), the resonant capacitor C_r's current, and consequently, the resonant inductor L_r's current, is described, as shown in Equation (2.13).

$$i_{L_r}(t) = \pm i_{C_r}(t) = \left(\frac{\pm V_{DM} - V_{C0}}{Z_r}\right) \cdot \sin(\omega_0 t) + I_{C0} \cdot \cos(\omega_0 t) \tag{2.13}$$

Equations (2.12) and (2.13) are further manipulated in order to achieve adimensional state variables, as described in Equations (2.14) and (2.15), respectively.

$$v_{C_r}(t) \cdot \frac{1}{V_1} = \frac{1}{V_1} \cdot \left[\pm V_{DM} - (\pm V_{DM} - V_{C0}) \cdot \cos(\omega_0 t) \pm Z_r I_{C0} \cdot \sin(\omega_0 t)\right] \tag{2.14}$$

$$i_{L_r}(t) \cdot \frac{Z_r}{V_1} = \frac{Z_r}{V_1} \cdot \left(\pm i_{C_r}(t)\right) = \frac{Z_r}{V_1} \cdot \left[(\pm V_{DM} - V_{C0}) \cdot \sin(\omega_0 t) + I_{C0} \cdot \cos(\omega_0 t)\right] \tag{2.15}$$

Based on (2.14) and (2.15), the normalization factors are defined and the normalized state variables are introduced, as shown in Equations (2.16) and (2.17), respectively.

$$\overline{v_{C_r}(t)} = v_{C_r}(t) \cdot \frac{1}{V_1} \tag{2.16}$$

$$\overline{i_{L_r}(t)} = i_{L_r}(t) \cdot \frac{Z_r}{V_1} \tag{2.17}$$

Thus,

$$\overline{v_{C_r}(t)} = \pm \overline{V_{DM}} - \left(\pm \overline{V_{DM}} - \overline{V_{C0}}\right) \cdot \cos(\omega_0 t) \pm Z_r \cdot \overline{I_{C0}} \cdot \sin(\omega_0 t) \tag{2.18}$$

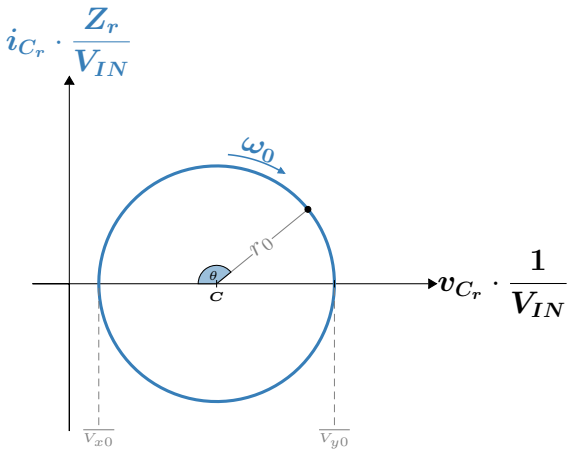
$$\overline{i_{L_r}(t)} = \pm \overline{i_{C_r}(t)} = \left(\pm \overline{V_{DM}} - \overline{V_{C0}}\right) \cdot \sin(\omega_0 t) + \overline{I_{C0}} \cdot \cos(\omega_0 t) \tag{2.19}$$

By manipulating (2.18) and (2.19), a general geometrical representation is derived, as shown in Equation (2.20).

$$\left(\overline{v_{C_r}(t)} \mp \overline{V_{DM}}\right)^2 + \left(\overline{i_{C_r}(t)}\right)^2 = \overline{I_{C0}}^2 + \left(\pm \overline{V_{DM}} - \overline{V_{C0}}\right)^2 \tag{2.20}$$

Equation (2.20) introduces a state-plane trajectory which corresponds to a circle with an explicit center C_0 and radius r_0, as shown in Equation (2.21) and (2.22), respectively, and geometrically exhibited in Figure 8.

Figure 8 – State-Plane Trajectory for a Generic LC series resonant circuit normalized to Z_r reference frame.



$$C_{0_{\langle Z_r \rangle}} = \left(\pm\overline{V_{DM}}, 0\right) \tag{2.21}$$

$$r_0{}^2 = \overline{I_{C0}}^2 + \left(\pm\overline{V_{DM}} - \overline{V_{C0}}\right)^2 \tag{2.22}$$

The trajectory initial condition depends on the charging/discharging scenario, where it starts at the point P_0, as shown in Equation (2.23), and progresses in the clockwise direction.

$$P_0 = \left(\pm\overline{V_{DM}} \mp r_0 \cdot \cos\left(\theta\right), \pm\overline{I_{C0}}\right) \tag{2.23}$$

2.2 CASE 2 - LCCP SERIES RESONANCE

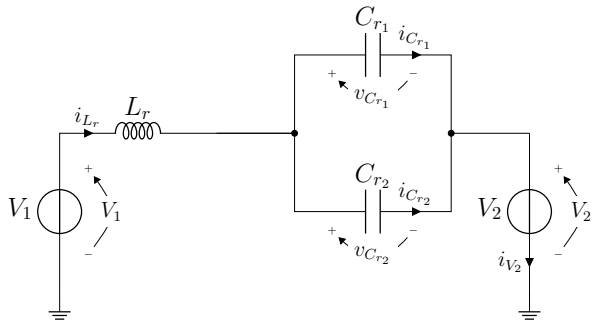
The 2nd case is comprised of a series resonance, based on a resonant inductor L_r, and a parallel connection of two resonant capacitors C_r, connected in series upon a non-zero excitation step voltage, as shown in Figure 9.

It can be observed as a particular case, from Case 1, where the resonant capacitor C_r becomes an equivalent resonant capacitor based on the parallel connection of two identical capacitors. The equivalent resonant capacitance is shown in Equation (2.24).

$$C_{r.eq} = 2 \cdot C_r \tag{2.24}$$

By applying (2.24) into (2.12), the equivalent resonant capacitors' voltage is derived, as shown in Equation (2.25).

Figure 9 – Generic Series Resonance LCCp Equivalent Circuit with a Differential-mode Voltage Excitation Signal.



$$v_{C_r}(t) = \pm V_{DM} - (\pm V_{DM} - V_{C0}) \cdot \cos\left(\frac{1}{\sqrt{2}} \cdot \omega_0 t\right) \pm \frac{\sqrt{2}}{2} \cdot Z_r I_{C0} \cdot \sin\left(\frac{1}{\sqrt{2}} \cdot \omega_0 t\right) \quad (2.25)$$

According to Equation (2.25), new resonant characteristics are introduced due to the parallel connection of capacitors. The resonant frequency ω_1 and characteristic impedance Z_{r_1} are defined, as per Equation (2.26) and (2.27), respectively.

$$\omega_1 = \frac{1}{\sqrt{2}} \cdot \omega_0 \quad (2.26)$$

$$Z_{r_1} = \frac{1}{\sqrt{2}} \cdot Z_r \quad (2.27)$$

Based on (2.26) and (2.27), (2.25) is re-defined as per Equation (2.28).

$$v_{C_r}(t) = \pm V_{DM} - (\pm V_{DM} - V_{C0}) \cdot \cos(\omega_1 t) \pm Z_{r_1} I_{C0} \cdot \sin(\omega_1 t) \quad (2.28)$$

Due to the parallel connection, (2.28) drives the current in the individual resonant capacitor, based on (2.29). The individual resonant capacitor's current is derived, as shown in Equation (2.30).

$$i_{C_r}(t) = C_r \cdot \frac{dv_{C_r}(t)}{dt} = \pm \frac{1}{2} \cdot i_{L_r}(t) \quad (2.29)$$

$$i_{C_r}(t) = \left(\frac{\pm V_{DM} - V_{C0}}{2Z_{r_1}}\right) \cdot \sin(\omega_1 t) + \frac{1}{2} \cdot I_{C0} \cdot \cos(\omega_1 t) \quad (2.30)$$

Similarly to the Case 1, (2.28) and (2.30) are manipulated to derive dimensionless state variables, as described in Equation (2.31) and (2.32), respectively.

$$v_{C_r}(t)\cdot\frac{1}{V_1}=\pm\frac{V_{DM}}{V_1}-\frac{\pm V_{DM}-V_{C0}}{V_1}\cdot\cos(\omega_1 t)\pm\frac{Z_{r_1}I_{C0}}{V_1}\cdot\sin(\omega_1 t) \tag{2.31}$$

$$i_{C_r}(t)\cdot\frac{2Z_{r_1}}{V_1}=\left(\frac{\pm V_{DM}-V_{C0}}{2Z_{r_1}}\right)\cdot\frac{2Z_{r_1}}{V_1}\cdot\sin(\omega_1 t)+\frac{1}{2}\cdot I_{C0}\cdot\frac{2Z_{r_1}}{V_1}\cdot\cos(\omega_1 t) \tag{2.32}$$

Based on (2.31) and (2.32), the normalization factors are defined and the normalized state variables are introduced, as shown in Equations (2.33) and (2.34), respectively.

$$\overline{v_{C_r}(t)}=v_{C_r}(t)\cdot\frac{1}{V_1} \tag{2.33}$$

$$\overline{\overline{i_{C_r}(t)}}=i_{C_r}(t)\cdot\frac{2Z_{r_1}}{V_1}=\sqrt{2}\cdot\overline{i_{C_r}(t)}=\frac{\omega_0}{\omega_1}\cdot\overline{i_{C_r}(t)} \tag{2.34}$$

Thus,

$$\overline{v_{C_r}(t)}=\pm\overline{V_{DM}}-\left(\pm\overline{V_{DM}}-\overline{V_{C0}}\right)\cdot\cos(\omega_1 t)\pm\frac{1}{2}\cdot\overline{\overline{I_{C0}}}\cdot\sin(\omega_1 t) \tag{2.35}$$

$$\overline{\overline{i_{C_r}(t)}}=\pm\frac{1}{2}\cdot\overline{\overline{i_{L_r}(t)}}=\left(\pm\overline{V_{DM}}-\overline{V_{C0}}\right)\cdot\sin(\omega_1 t)+\frac{1}{2}\cdot\overline{\overline{I_{C0}}}\cdot\cos(\omega_1 t) \tag{2.36}$$

By manipulating (2.35) and (2.36), a general geometrical representation is derived, as shown in Equation (2.37).

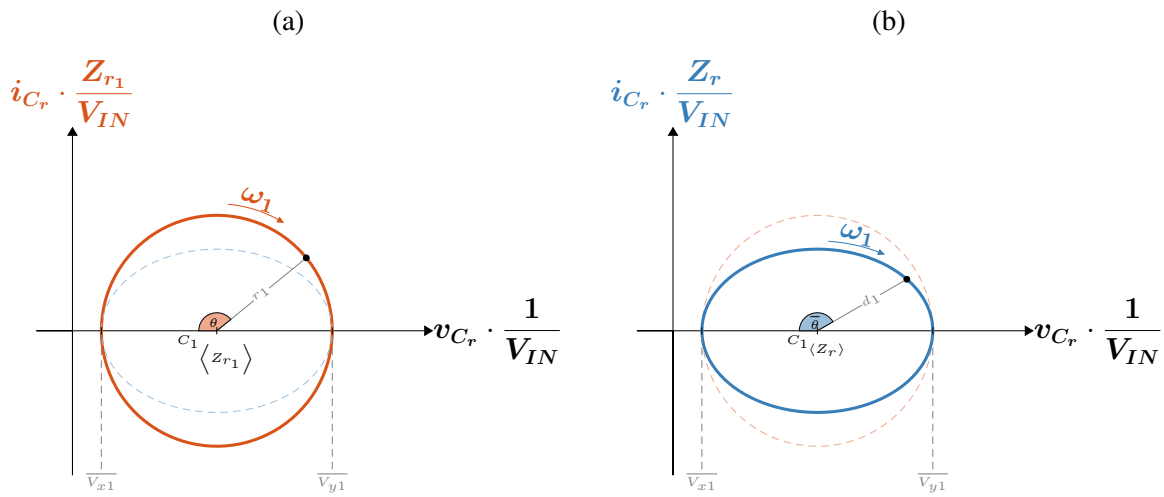
$$\left(\overline{v_{C_r}(t)}\mp\overline{V_{DM}}\right)^2+\left(\overline{\overline{i_{C_r}(t)}}\right)^2=\left(\frac{1}{2}\right)^2\cdot\overline{\overline{I_{C0}}}^2+\left(\pm\overline{V_{DM}}-\overline{V_{C0}}\right)^2 \tag{2.37}$$

Differently from Case 1, by altering the normalization factor, described in (2.34), to (2.17), the trajectory geometry is affected as derived in Equation (2.38).

$$\left(\overline{v_{C_r}(t)}\mp\overline{V_{DM}}\right)^2+\frac{\left(\overline{i_{C_r}(t)}\right)^2}{\left(\frac{\omega_1}{\omega_0}\right)^2}=\left(\frac{\omega_0}{\omega_1}\right)^2\cdot\left(\frac{1}{2}\right)^2\cdot\overline{I_{C0}}^2+\left(\pm\overline{V_{DM}}-\overline{V_{C0}}\right)^2 \tag{2.38}$$

Equations (2.37) and (2.38) are geometrical forms, representing the trajectory for the state variables, corresponding to a Circular and an Elliptical Trajectory, respectively. By modifying the normalization factor, the original circle is stretched/contracted in the i_{C_r} axis. The circle,

Figure 10 – State-Plane Trajectory for a Generic LCCp series resonant circuit normalized to:
(a) Z_{r_1} reference frame.
(b) Z_r reference frame.



represented in (2.37), exhibits an explicit center $C_{1_{\langle Z_{r_1}\rangle}}$ and radius r_1, as shown in Equation (2.39) and (2.40), respectively, and geometrically exhibited in Figure 10a.

$$C_{1_{\langle Z_{r_1}\rangle}} = \left(\pm\overline{V_{DM}}, 0\right) \tag{2.39}$$

$$r_1{}^2 = \left(\frac{1}{2}\right)^2 \cdot \overline{\overline{I_{C0}}}^2 + \left(\pm\overline{V_{DM}} - \overline{V_{C0}}\right)^2 \tag{2.40}$$

whereas, the Ellipse, represented in (2.38), exhibits an explicit center $C_{1_{\langle Z_r\rangle}}$ and a major axis oriented in the v_{C_r} direction, and a minor axis oriented in the i_{C_r} direction, with total lengths a_1 and b_1, respectively, as described in Equations (2.41), (2.42) and (2.43), and geometrically exhibited in Figure 10b.

$$C_{1_{\langle Z_{r_1}\rangle}} = \left(\pm\overline{V_{DM}}, 0\right) \tag{2.41}$$

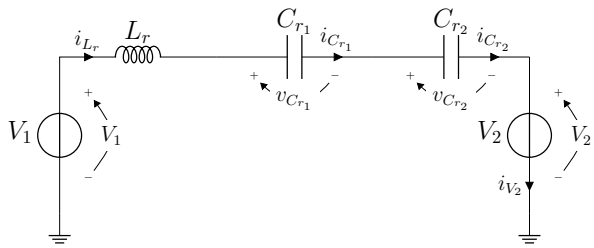
$$a_1{}^2 = \left(\frac{\omega_0}{\omega_1}\right)^2 \cdot \left(\frac{1}{2}\right)^2 \cdot \overline{I_{C0}}^2 + \left(\pm\overline{V_{DM}} - \overline{V_{C0}}\right)^2 \tag{2.42}$$

$$b_1{}^2 = \left(\frac{\omega_1}{\omega_0}\right)^2 \cdot \left[\left(\frac{\omega_0}{\omega_1}\right)^2 \cdot \left(\frac{1}{2}\right)^2 \cdot \overline{I_{C0}}^2 + \left(\pm\overline{V_{DM}} - \overline{V_{C0}}\right)^2\right] \tag{2.43}$$

2.3 CASE 3 - LCCS SERIES RESONANCE

The 3rd case is comprised of a series resonance, based on a resonant inductor L_r, and a series connection of two resonant capacitors C_r, connected in series upon a non-zero excitation step voltage, as shown in Figure 11.

Figure 11 – Generic Series Resonance LCCs Equivalent Circuit with a Differential-mode Voltage Excitation Signal.



It can also be observed as a particular case, from Case 1, where the resonant capacitor C_r becomes an equivalent resonant capacitor based on the series connection of two identical capacitors. The equivalent resonant capacitance is shown in Equation (2.44).

$$C_{r.eq} = \frac{1}{2} \cdot C_r \tag{2.44}$$

By applying (2.44) into (2.13), the equivalent resonant capacitors' voltage is derived, as shown in Equation (2.45).

$$i_{L_r}(t) = \pm i_{C_r}(t) = \left(\frac{V_{DM} - (\pm V_{C10}) - (\pm V_{C20})}{\sqrt{2} \cdot Z_r} \right) \cdot \sin\left(\sqrt{2} \cdot \omega_0 t\right) + I_{C0} \cdot \cos\left(\sqrt{2} \cdot \omega_0 t\right) \tag{2.45}$$

According to Equation (2.45), new resonant characteristics are introduced due to the series connection of capacitors. The resonant frequency ω_2 and characteristic impedance Z_{r_2} are defined, as per Equation (2.46) and (2.47), respectively.

$$\omega_2 = \sqrt{2} \cdot \omega_0 \tag{2.46}$$

$$Z_{r_2} = \sqrt{2} \cdot Z_r \tag{2.47}$$

Based on (2.46) and (2.47), (2.45) is re-defined as per Equation (2.48).

$$i_{L_r}(t) = \pm i_{C_r}(t) = \left(\frac{V_{DM} - (\pm V_{C10}) - (\pm V_{C20})}{Z_{r_2}} \right) \cdot \sin(\omega_2 t) + I_{C0} \cdot \cos(\omega_2 t) \tag{2.48}$$

Due to the series connection, (2.48) drives the current in the individual resonant capacitor, based on (2.49). The individual resonant capacitor's voltage is derived, as shown in Equation (2.50).

$$i_{L_r}(t) = \pm i_{C_{r_n}}(t) = \pm C_{r_n} \cdot \frac{dv_{C_{r_n}}(t)}{dt} \tag{2.49}$$

$$\begin{aligned} v_{C_{r_n}}(t) =& V_{C_{N0}} \pm \frac{1}{2} \cdot \left(V_{DM} - (\pm V_{C10}) - (\pm V_{C20})\right) \cdot \left(1 - \cos(\omega_2 t)\right) \pm \\ & \pm \frac{1}{2} \cdot Z_{r_2} \cdot I_{C0} \cdot \sin(\omega_2 t) \end{aligned} \tag{2.50}$$

Similarly to the Case 1, (2.48) and (2.50) are manipulated to derive dimensionless state variables, as described in Equation (2.53) and (2.52), respectively.

$$\begin{aligned} i_{L_r}(t) \cdot \frac{Z_{r_2}}{2V_1} = \pm i_{C_r}(t) \cdot \frac{Z_{r_2}}{2V_1} =& \left(\frac{V_{DM} - (\pm V_{C10}) - (\pm V_{C20})}{2}\right) \cdot \sin(\omega_2 t) + \\ & + \frac{Z_{r_2}}{2V_1} \cdot I_{C0} \cdot \cos(\omega_2 t) \end{aligned} \tag{2.51}$$

$$\begin{aligned} v_{C_{r_n}}(t) \cdot \frac{1}{V_1} =& \frac{V_{C_{N0}}}{V_1} \pm \frac{1}{2} \cdot \frac{V_{DM} - (\pm V_{C10}) - (\pm V_{C20})}{V_1} \cdot \left(1 - \cos(\omega_2 t)\right) \pm \\ & \pm \frac{1}{2} \cdot \frac{Z_{r_2} \cdot I_{C0}}{V_1} \cdot \sin(\omega_2 t) \end{aligned} \tag{2.52}$$

Based on (2.51) and (2.52), the normalization factors are defined and the normalized state variables are introduced, as shown in Equations (2.53) and (2.54), respectively.

$$\overline{\overline{\overline{i_{C_r}(t)}}} = i_{C_r}(t) \cdot \frac{Z_{r_2}}{2V_1} = \frac{1}{\sqrt{2}} \cdot \overline{i_{C_r}(t)} = \frac{\omega_0}{\omega_2} \cdot \overline{i_{C_r}(t)} \tag{2.53}$$

$$\overline{v_{C_{r_n}}(t)} = v_{C_{r_n}}(t) \cdot \frac{1}{V_1} \tag{2.54}$$

Thus,

$$\begin{aligned} \overline{\overline{\overline{i_{L_r}(t)}}} = \pm \overline{\overline{\overline{i_{C_r}(t)}}} =& \left(\frac{\overline{V_{DM}} - (\pm \overline{V_{C10}}) - (\pm \overline{V_{C20}})}{2}\right) \cdot \sin(\omega_2 t) + \\ & + \overline{\overline{\overline{I_{C0}}}} \cdot \cos(\omega_2 t) \end{aligned} \tag{2.55}$$

$$\begin{aligned} \overline{v_{C_{r_n}}(t)} =& \overline{V_{C_{N0}}} \pm \frac{1}{2} \cdot \left(\overline{V_{DM}} - (\pm \overline{V_{C10}}) - (\pm \overline{V_{C20}})\right) \cdot \left(1 - \cos(\omega_2 t)\right) \pm \\ & \pm \overline{\overline{\overline{I_{C0}}}} \cdot \sin(\omega_2 t) \end{aligned} \tag{2.56}$$

By manipulating (2.55) and (2.56), a general geometrical representation is derived, as shown in Equation (2.57).

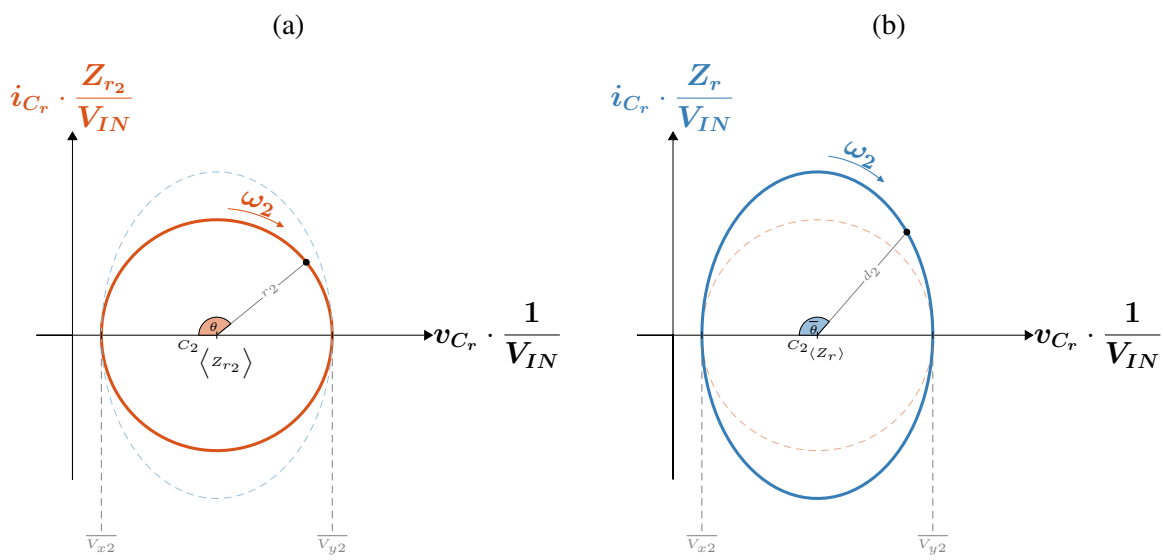
$$\begin{aligned}\left(\overline{v_{C_{rn}}(t)}-\overline{V_{CN0}}\mp\frac{1}{2}\cdot\left(\overline{V_{DM}}-\left(\pm\overline{V_{C10}}\right)-\left(\pm\overline{V_{C20}}\right)\right)\right)^2+\left(\overline{\overline{i_{C_r}(t)}}\right)^2 &= \\ \overline{\overline{I_{C0}}}^2+\left(\frac{1}{2}\right)^2\cdot\left(\overline{V_{DM}}-\left(\pm\overline{V_{C10}}\right)-\left(\pm\overline{V_{C20}}\right)\right)^2 &\end{aligned} \tag{2.57}$$

Similar to Case 2, by altering the normalization factor, described in (2.53), to (2.17), the trajectory geometry is affected as derived in Equation (2.58).

$$\begin{aligned}\left(\overline{v_{C_{rn}}(t)}-\overline{V_{CN0}}\mp\frac{1}{2}\cdot\left(\overline{V_{DM}}-\left(\pm\overline{V_{C10}}\right)-\left(\pm\overline{V_{C20}}\right)\right)\right)^2+\frac{\left(\overline{i_{C_r}(t)}\right)^2}{\left(\frac{\omega_2}{\omega_0}\right)^2} &= \\ \left(\frac{\omega_0}{\omega_2}\right)^2\cdot\overline{I_{C0}}^2+\left(\frac{1}{2}\right)^2\cdot\left(\overline{V_{DM}}-\left(\pm\overline{V_{C10}}\right)-\left(\pm\overline{V_{C20}}\right)\right)^2 &\end{aligned} \tag{2.58}$$

Equations (2.57) and (2.58) are geometrical forms, representing the trajectory for the state variables, corresponding to a Circular and an Elliptical Trajectory, respectively. By modifying the normalization factor, the original circle is stretched/contracted in the i_{C_r} axis. The circle, represented in (2.57), exhibits an explicit center $C_{2_{\langle Z_{r_2}\rangle}}$ and radius r_2, as shown in Equation (2.59) and (2.60), respectively, and geometrically exhibited in Figure 12a.

Figure 12 – State-Plane Trajectory for a Generic LCCs series resonant circuit normalized to:
(a) Z_{r_2} reference frame.
(b) Z_r reference frame.



$$C_{2_{\langle Z_{r_2}\rangle}}=\left(\overline{V_{CN0}}\pm\frac{1}{2}\cdot\left(\overline{V_{DM}}-\left(\pm\overline{V_{C10}}\right)-\left(\pm\overline{V_{C20}}\right)\right),0\right) \tag{2.59}$$

$$r_2{}^2 = \overline{\overline{\overline{I_{C0}}}}^2 + \left(\frac{1}{2}\right)^2 \cdot \left(\overline{V_{DM}} - \left(\pm\overline{V_{C10}}\right) - \left(\pm\overline{V_{C20}}\right)\right)^2 \tag{2.60}$$

whereas, the Ellipse, represented in (2.58), exhibits an explicit center $C_{2_{\langle Z_r \rangle}}$ and a major axis oriented in the $\boldsymbol{i}_{C_r}$ direction, and a minor axis oriented in the $\boldsymbol{v}_{C_r}$ direction, with total lengths a_2 and b_2, respectively, as described in Equations (2.61), (2.62) and (2.63), and geometrically exhibited in Figure 12b.

$$C_{2_{\langle Z_r \rangle}} = \left(\pm\overline{V_{DM}}, 0\right) \tag{2.61}$$

$$a_2{}^2 = \left(\frac{\omega_2}{\omega_0}\right)^2 \cdot \left[\left(\frac{\omega_0}{\omega_2}\right)^2 \cdot \overline{I_{C0}}^2 + \left(\frac{1}{2}\right)^2 \cdot \left(\overline{V_{DM}} - \left(\pm\overline{V_{C10}}\right) - \left(\pm\overline{V_{C20}}\right)\right)^2\right] \tag{2.62}$$

$$b_2{}^2 = \left(\frac{\omega_0}{\omega_2}\right)^2 \cdot \overline{I_{C0}}^2 + \left(\frac{1}{2}\right)^2 \cdot \left(\overline{V_{DM}} - \left(\pm\overline{V_{C10}}\right) - \left(\pm\overline{V_{C20}}\right)\right)^2 \tag{2.63}$$

3 4L-RFLC BOOST CONVERTER DESCRIPTION

The proposed 4L-RFLCC comprises six Switches, in which three Low-Side Switches $S_1 - S_3$ shall be actively driven whereas three High-Side Switches $S_4 - S_6$ are optionally driven. Additionally, in order to introduce the resonant link in between the Input and Output, the resonant inductor L_r and two resonant capacitors C_{r_1} and C_{r_2} are present.

In order to provide a comprehensive description of the proposed converter's operation principle the following assumptions are made:

1. Resonant Capacitors C_{r1} and C_{r2} are considered to be the same. Therefore, $C_{r1} = C_{r2} = C_r$.
2. Output Capacitor C_{OUT} is considered to be large enough. Therefore, v_{OUT} is a constant.
3. Switching Frequency f_{SW} is always lower, or equal to $\frac{2}{3}$, of the Resonant Frequency ω_o.
4. Switches S_1 - S_6 are considered ideal Two-Quadrant Switches with anti-parallel body diode. Therefore, C_{oss} is negligible.
5. Effect of dead-time is negligible for the analytical description of the proposed converter.

Additionally, the operating principles are divided into four distinct operating regions based on the operating condition of the proposed 4L-RFLCC. Each Region is discussed within this Chapter alongside its output characteristics and boundary conditions.

3.1 MODULATION STRATEGY

In order to secure a proper operation, the Switch Pair S_1S_6, S_2S_5 and S_3S_4, also referred as Switch Pair ①, ② and ③, respectively, shall not be driven simultaneously. The two possible driving strategies are either complementary, which by taking Switch Pair ① as an example, the Switch S_1 is driven by D_1 whereas Switch S_6 is driven by $\overline{D_1}$. Or, the Switch Pair is driven asynchronously but always fulfilling the exclusive driving strategy.

In order to fully utilize the Switch Pairs, and introduce a balance and synchronization amongst Switch Pairs, the duty-cycle ratio is approximately 66.6% $\left(D = \frac{2}{3}\right)$ whereas each Switch Pair is phase-shifted by 120°. As a result, there exist always two Switch Pairs activated within the operation of the proposed modulation scheme. The proposed 4L-RFLCC is also capable of being driven asynchronously based on the phase-timings, in order to reduce the idle state, in between Switching Transitions, and with lower duty-cycle ratio to achieve partial voltage conversion ratio. The two above-mentioned strategies will not be covered in this Thesis.

In order to avoid unintended reverse conduction, the High-side Switches $S_4 - S_6$ are passively driven. Thus, herewith they are considered as Diodes. Yet, the High-Side Switches can be considered as Active Switches, given their reverse conduction characteristics and the

phase-timing for Synchronous activation based on current. However, for the sake of description, and illustration, they are assumed to be Passive Switches.

The PWM Sequence, which is valid within every Operating Region, is considered to be clock-wise and counter clock-wise, depending on the Switch Pair activation sequencing, as defined in Table 2.

Table 2 – List of Active Switches Transition Events.

Transition Event	**Switches State**		
	S_1	S_2	S_3
11	ON↑	ON	OFF↓
21	ON	OFF ↓	ON ↑
31	OFF ↓	ON ↑	ON
12	OFF ↓	ON	ON ↑
22	ON ↑	OFF ↓	ON
32	ON	ON ↑	OFF ↓

According to Table 2, there exist three active Topological Stages whereas additional Passive Topological Stages may exist depending on the operating condition.

3.2 REGION I

By definition, the Operating Region I is under a heavy load condition and/or the operating switching frequency is low.

Due to the proposed topology connections, the output voltage V_{OUT} shall be higher or equal to the input voltage V_{IN}. At the start-up, the output bus capacitor charges up to approximately V_{IN} through the Passive Switches $S_4 - S_6$ whereas the resonant capacitors are completely discharged.

The operation of the converter starts at the Transition Event 11, in which the Interval I begins.

3.2.1 Interval I ($t_0 < t < t_1$)

When the Active Switch S_3 turns-OFF, while S_2 remains ON, and the Active Switch S_1 turns-ON, the converter operates with the equivalent circuit shown in Figure 13a. The Interval I consists of a $L_r\,(C_{r_1}||C_{r_2})$ resonant tank, analog to the description shown in the Section 2.2. As a result, the resonant tank is excited by V_{IN}, deriving a resonance activity under ω_1 trajectory velocity. The resonance creates a sinusoidal shaped state variables v_{C_r} and $i_{C_{r_n}}$, where $n \in \{1,2\}$, as described in Equations (2.28) and (2.30), respectively, in which the parameters are as described below.

$$V_{DM} = V_1 - V_2 = V_{IN} - 0 = V_{IN} \tag{3.1}$$

$$V_{C0} = 0 \tag{3.2}$$

$$I_{C0} = 0 \tag{3.3}$$

As a result, the resultant Z_{r_1}-normalized state variables are described in (3.4) and (3.5) while the state-plane trajectory, in the local resonant tank Z_{r_1} reference frame, is described as shown in (3.6) and Figure 13b, whereas the state-plane trajectory, in the system resonant tank Z_r reference frame, is described as shown in (3.7) and Figure 13c.

$$\overline{v_{C_r}(t)} = +1 - \cos(\omega_1 t) \tag{3.4}$$

$$\overline{\overline{i_{C_{rn}}(t)}} = +\frac{1}{2} \cdot \overline{\overline{i_{L_r}(t)}} = +\sin(\omega_1 t) \tag{3.5}$$

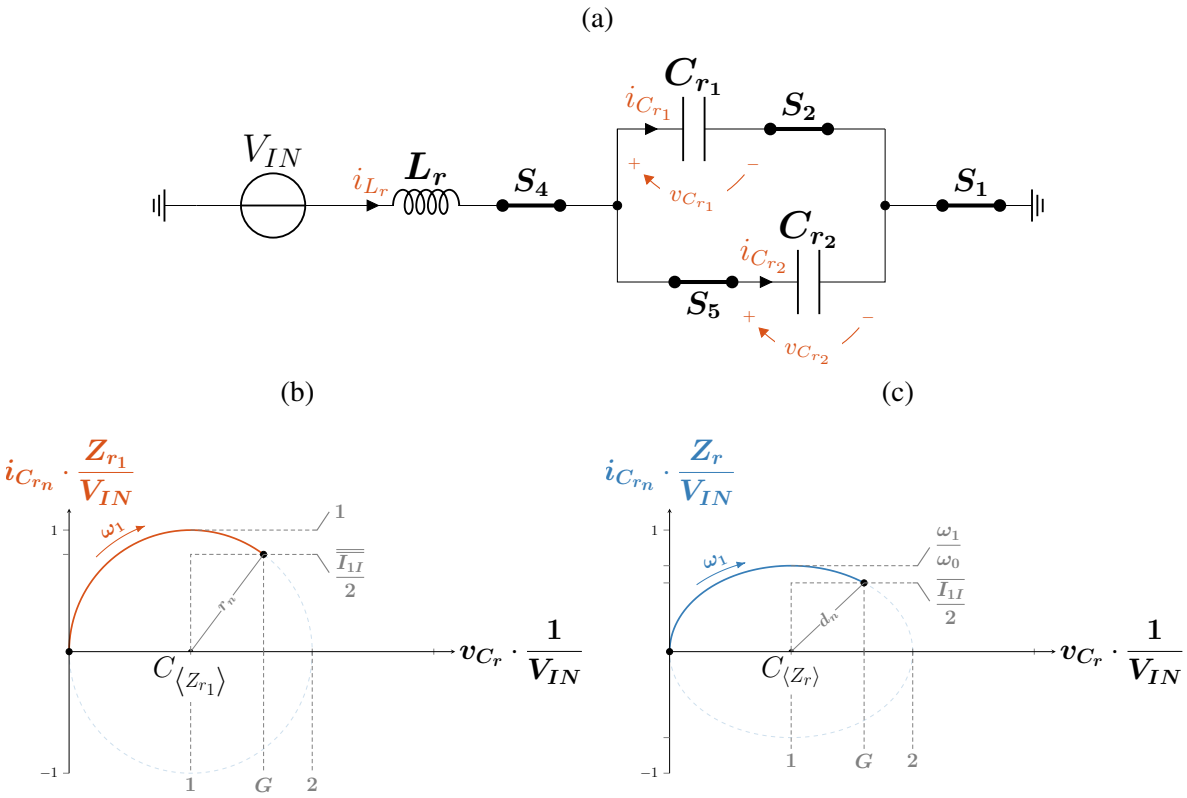
$$\left(\overline{v_{C_r}(t)} - 1\right)^2 + \left(\overline{\overline{i_{C_r}(t)}}\right)^2 = 1 \tag{3.6}$$

$$\left(\overline{v_{C_r}(t)} - 1\right)^2 + \frac{\left(\overline{i_{C_r}(t)}\right)^2}{\left(\frac{\omega_1}{\omega_0}\right)^2} = 1 \tag{3.7}$$

where $\frac{\omega_1}{\omega_0}$ is defined in Equation (2.26).

By interpreting the state-plane trajectory, in Figure 13b, the state variable $v_{C_{rn}}$ exhibits a maximum normalized peak voltage $MAX[V_{C_{rn}}]$ value of 2 and a maximum Z_{r_1}-normalized peak current $MAX[I_{C_{rn}}]$ value of 1. As a result, the boundary condition for the full sinusoidal waveform is identified, as well as the boundary condition for the transition to a passive topological stage given the actual output voltage V_{OUT} level. Once $\overline{v_{C_{rn}}}$ reaches V_{OUT}, the Diode D_6 forward biases; thus, changing the operating behavior, initiating the Interval II. Additionally, it indicates the resonant inductor current $\overline{\overline{i_{L_r}}}$ final condition at t_1 of $\overline{\overline{I_{1I}}}$.

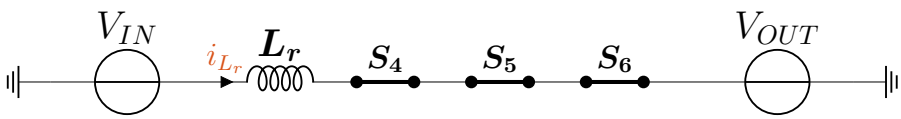
Figure 13 – Resultant Characteristics based on the Operating Region I within Interval I:
(a) Equivalent Circuit.
(b) Geometrical Representation normalized by Z_{r_1} reference frame.
(c) Geometrical Representation normalized by Z_r reference frame.



3.2.2 Interval II ($t_1 < t < t_2$)

By forward biasing Diode D_6, the resonant capacitors' voltage $\overline{v_{C_{r_n}}}$ clamps to the Output Voltage V_{OUT}, driving the resonant capacitors to an idle state. As a consequence, the converter operates with the equivalent circuit shown in Figure 14, when it initiates a linear stage, where the resonant inductor's current $\overline{i_{L_r}}$ linearly decreases. Equation (3.8) is derived according to the equivalent circuit.

Figure 14 – Equivalent Circuit for Operating Region I within Interval II.



$$\overline{i_{L_r}}(t) = (1-G) \cdot \omega_0 \cdot (t - t_1) + \overline{I_{1I}} \tag{3.8}$$

Due to the Passive Switches $S_4 - S_6$, the boundary condition for Interval II is by depleting the full stored energy from the resonant inductor L_r to the Output or by triggering the Transition State (21). As the goal is to operate the converter in DCM, the later is not addressed in the

4L-RFLCC analysis. Therefore, by assuming the current discontinuity, it shifts to an additional passive topological stage, initiating the Interval III.

3.2.3 Interval III ($t_2 < t < t_3$)

The Interval III is initiated by the current discontinuity, in which the Passive Switches $S_4 - S_6$ reverse biases, resulting in an idle state. The Interval III lasts until the Transition State **21** is triggered.

3.2.4 Interval IV ($t_3 < t < t_4$)

When the Active Switch S_2 turns-OFF, while S_1 remains ON, and the Active Switch S_3 turns-ON, the converter operates with the equivalent circuit shown in Figure 15a. The Interval IV consists of a $L_r C_{r_1}$ resonant tank, analog to the description shown in the Section 2.1. As a result, the resonant tank is excited by $V_{IN} - V_{OUT}$, deriving a resonance activity under ω_0 trajectory velocity. Due to the negative excitation, the resonant capacitor C_{r_1} transfers its energy to the output. The resonance creates a sinusoidal shaped state variables $\boldsymbol{v}_{C_{r_1}}$ and $\boldsymbol{i}_{C_{r_1}}$, as described in Equations (2.12) and (2.13), respectively, in which the parameters are as described below.

$$V_{DM} = V_1 - V_2 = V_{IN} - V_{OUT} \tag{3.9}$$

$$V_{C0} = V_{OUT} \tag{3.10}$$

$$I_{C0} = 0 \tag{3.11}$$

As a result, the resultant Z_r-normalized state variables are described in (3.12) and (3.13) while the state-plane trajectory, in the local resonant tank Z_r reference frame, is described as shown in (3.14) and Figure 15b.

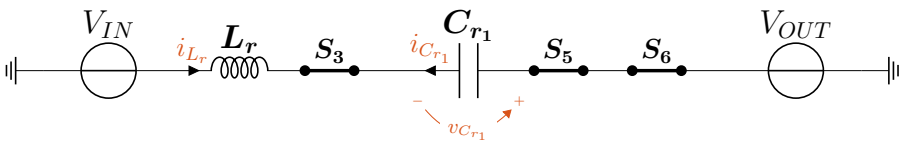
$$\overline{v_{C_r}(t)} = G - 1 + \cos(\omega_0 t) \tag{3.12}$$

$$\overline{i_{C_{r_1}}(t)} = -\overline{i_{L_r}(t)} = -\sin(\omega_0 t) \tag{3.13}$$

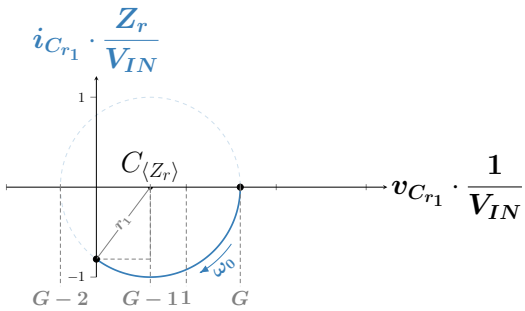
$$\left(\overline{v_{C_{r_1}}(t)} - (G-1)\right)^2 + \left(\overline{i_{C_{r_1}}(t)}\right)^2 = 1 \tag{3.14}$$

Figure 15 – Resultant Characteristics based on the Operating Region I within Interval IV:
(a) Equivalent Circuit.
(b) Geometrical Representation normalized by Z_r reference frame.

(a)



(b)

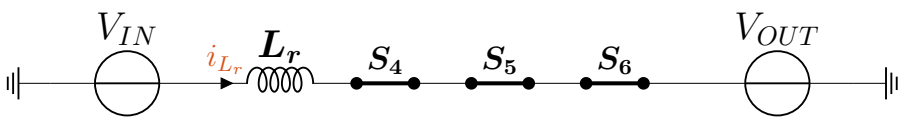


By interpreting the state-plane trajectory, in Figure 15b, the state variable $v_{C_{r_n}}$ exhibits a minimum normalized peak voltage $MIN[\overline{V_{C_{r_n}}}]$ value of G-2 and a maximum Z_{r_1}-normalized peak current $MAX[\overline{I_{C_{r_1}}}]$ value of 1. As a result, the boundary condition for the full sinusoidal waveform is identified, as well as the boundary condition for the transition to a passive topological stage given the actual output voltage V_{OUT} level. Once $\overline{v_{C_{r_1}}}$ reaches 0, the Diode D_4 forward biases; thus, changing the operating behavior, initiating the Interval V. Additionally, it indicates the resonant inductor current $\overline{i_{L_r}}$ final condition at t_4 of $\overline{I_{2I}}$.

3.2.5 Interval V ($t_4 < t < t_5$)

By forward biasing Diode D_4, the resonant capacitor's voltage $\overline{v_{C_{r_1}}}$ clamps to Ground 0, driving the resonant capacitor C_{r_1} to an idle state. As a consequence, the converter operates with the equivalent circuit shown in Figure 16, when it initiates a linear stage, where the resonant inductor's current $\overline{i_{L_r}}$ linearly decreases. Equation (3.15) is derived according to the equivalent circuit.

Figure 16 – Equivalent Circuit for Operating Region I within Interval V.



$$\overline{i_{L_r}}(t) = (1-G)\cdot\omega_0\cdot(t-t_4)+\overline{I_{2I}} \tag{3.15}$$

Due to the Passive Switches $S_4 - S_6$, the boundary condition for Interval V is by depleting the full stored energy from the resonant inductor L_r to the Output or by triggering the Transition State (31). As the goal is to operate the converter in DCM, the later is not addressed in the 4L-RFLCC analysis. Therefore, by assuming the current discontinuity, it shifts to an additional passive topological stage, initiating the Interval VI.

3.2.6 Interval VI ($t_5 < t < t_6$)

The Interval VI is initiated by the current discontinuity, in which the Passive Switches $S_4 - S_6$ reverse biases, resulting in an idle state. The Interval VI lasts until the Transition State (31) is triggered.

3.2.7 Interval VII ($t_6 < t < t_7$)

When the Active Switch S_1 turns-OFF, while S_3 remains ON, and the Active Switch S_2 turns-ON, the converter operates with the equivalent circuit shown in Figure 17a. The Interval VII consists of a $L_r C_{r_2}$ resonant tank, analog to the description shown in the Section 2.1. Due to an identical initial conditions, as within Interval IV, and equivalent circuit, the resonant capacitor C_{r_2} transfers its energy to the output. The resonance creates a sinusoidal shaped state variables $v_{C_{r_2}}$ and $i_{C_{r_2}}$, as described in Equations (2.12) and (2.13), respectively, in which the parameters are as described below.

$$V_{DM} = V_1 - V_2 = V_{IN} - V_{OUT} \tag{3.16}$$

$$V_{C0} = V_{OUT} \tag{3.17}$$

$$I_{C0} = 0 \tag{3.18}$$

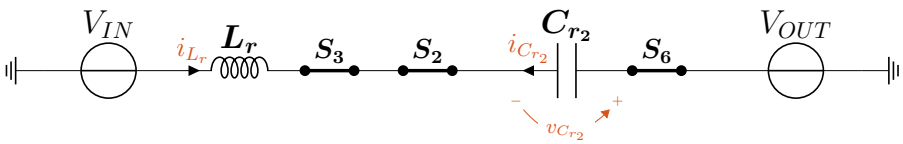
As a result, the resultant Z_r-normalized state variables are described in (3.19) and (3.20) while the state-plane trajectory, in the local resonant tank Z_r reference frame, is described as shown in (3.21) and Figure 17b.

$$\overline{v_{C_{r_2}}(t)} = G - 1 + \cos(\omega_0 t) \tag{3.19}$$

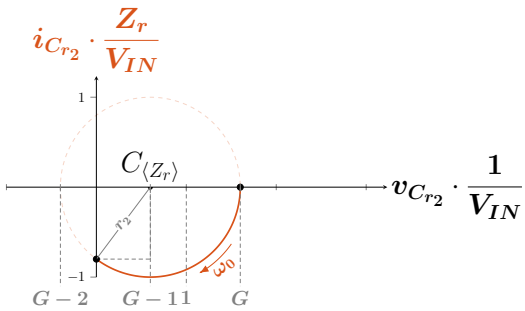
$$\overline{i_{C_{r_2}}(t)} = -\overline{i_{L_r}(t)} = -\sin(\omega_0 t) \tag{3.20}$$

Figure 17 – Resultant Characteristics based on the Operating Region I within Interval VII:
(a) Equivalent Circuit.
(b) Geometrical Representation normalized by Z_r reference frame.

(a)



(b)



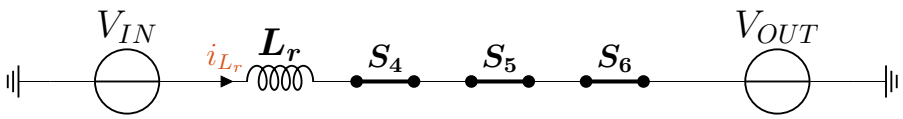
$$\left(\overline{v_{C_{r_2}}(t)} - (G-1)\right)^2 + \left(\overline{i_{C_{r_2}}(t)}\right)^2 = 1 \tag{3.21}$$

The state-plane trajectory interpretation is the same as for the Interval IV. Thus, once $\overline{v_{C_{r_2}}}$ reaches 0, the Diode D_5 forward biases; thus, changing the operating behavior, initiating the Interval VIII. Additionally, it indicates the resonant inductor current $\overline{i_{L_r}}$ final condition at t_7 of $\overline{I_{2I}}$.

3.2.8 Interval VIII ($t_7 < t < t_8$)

By forward biasing Diode D_5, the resonant capacitor's voltage $\overline{v_{C_{r_2}}}$ clamps to the Ground 0, driving the resonant capacitor C_{r_2} to an idle state. As a consequence, the converter operates with the equivalent circuit shown in Figure 18, when it initiates a linear stage, where the resonant inductor's current $\overline{i_{L_r}}$ linearly decreases. Equation (3.22) is derived according to the equivalent circuit.

Figure 18 – Equivalent Circuit for Operating Region I within Interval VIII.



$$\overline{i_{L_r}}(t) = (1-G) \cdot \omega_0 \cdot (t - t_7) + \overline{I_{2I}} \tag{3.22}$$

Due to the Passive Switches $S_4 - S_6$, the boundary condition for Interval VIII is by depleting the full stored energy from the resonant inductor L_r to the Output or by triggering the Transition State ⑪. As the goal is to operate the converter in DCM, the later is not addressed in the 4L-RFLCC analysis. Therefore, by assuming the current discontinuity, it shifts to an additional passive topological stage, initiating the Interval IX.

3.2.9 Interval IX ($t_8 < t < t_9$)

The Interval IX is initiated by the current discontinuity, in which the Passive Switches $S_4 - S_6$ reverse biases, resulting in an idle state. The Interval IX lasts until the Transition State ⑪ is triggered and a new cycle initiates.

3.2.10 Summary of Operation

Table 3 – Summary of the different topological stages and their characteristics for the 4LRFLC topology under Region I condition.

Topological Stage	**Switches State**			**L_r and C_r State**			**Operating Mode**
	S_1	S_2	S_3	L_r	C_{r1}	C_{r2}	
1st	ON	ON	OFF	$\nearrow$	$\nearrow$	$\nearrow$	*Resonant* (ω_1)
2nd	ON	ON	OFF	$\searrow$	$\rightarrow$	$\rightarrow$	*Linear*
3rd	ON	ON	OFF	$\rightarrow$	$\rightarrow$	$\rightarrow$	*Idle*
4th	ON	OFF	ON	$\nearrow$	$\searrow$	$\rightarrow$	*Resonant* (ω_0)
5th	ON	OFF	ON	$\searrow$	$\rightarrow$	$\rightarrow$	*Linear*
6th	ON	OFF	ON	$\rightarrow$	$\rightarrow$	$\rightarrow$	*Idle*
7th	OFF	ON	ON	$\nearrow$	$\rightarrow$	$\searrow$	*Resonant* (ω_0)
8th	OFF	ON	ON	$\searrow$	$\rightarrow$	$\rightarrow$	*Linear*
9th	OFF	ON	ON	$\rightarrow$	$\rightarrow$	$\rightarrow$	*Idle*

The Table 3 summarizes the different topological stages, and their main characteristics,which are illustrated in the Z_r State-Plane Trajectories in Figure 19 and in the time-domain state variables, shown in Figure 20. Due to the operating point of the proposed 4L-RFLCC, driven by the $\Lambda \leq 1$ condition, its behaviour differs given the particular characteristic of having every flying capacitors' voltage being clamped by the output voltage and fully discharged to zero. This condition leads to a particular behaviour in which the proposed 4L-RFLCC behaves linearly within multiple Intervals of the operating principle, similarly as shown for the 3L-RFLCC shown in Section 1.2.1. By that, this Region of Operation is the most similar to the 3L-RFLCC amongst all Regions of Operation.

Due to the further number of flying capacitors' commutation cell, there exist additional stages where the converter is capable of transferring energy from the input to the output linearly.

Figure 19 – Normalized State-Plane Trajectory under Operating Region I for:
(a) C_{r_1}
(b) C_{r_2}

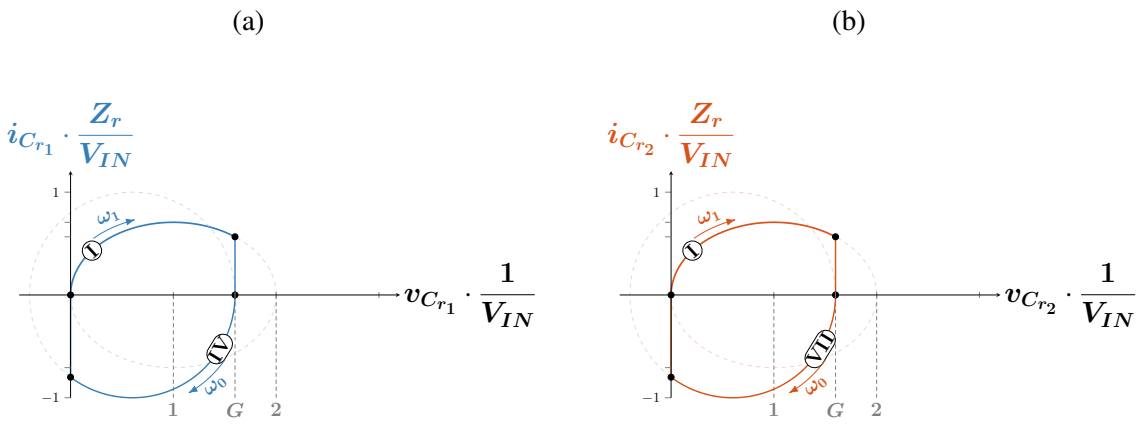
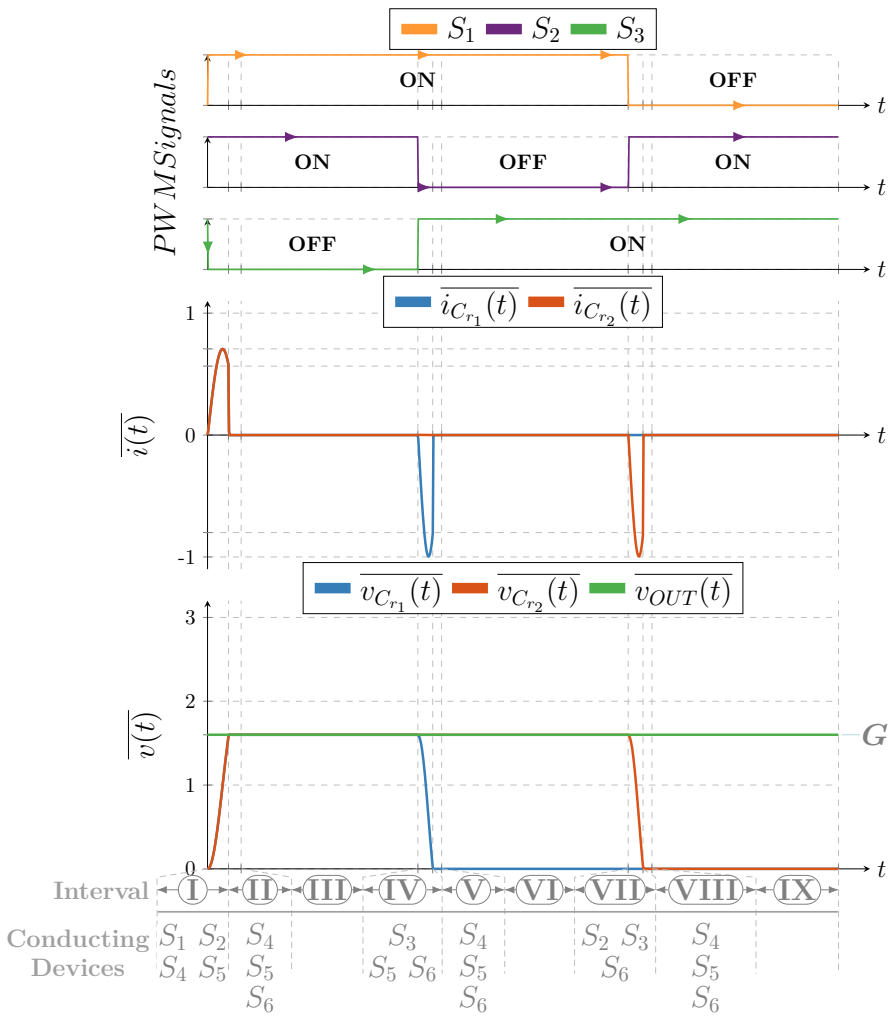


Figure 20 – Normalized Time-Domain State Variables for Operating Region I.



This characteristics, enables a higher utilization of the proposed converter in delivering the energy packages, which can be directly comparable to the 3L-RFLCC.

3.3 REGION II

By taking the Region I's boundary condition, as defined within Section 3.2.1, the Operating Region II modifies the converter's operating principles by eliminating the linear topological stages, shown in Sections 3.2.3, 3.2.5 and 3.2.8. Given an increment in V_{OUT}, based on the operating condition, the following Section describe the converter's behavior within the Operating Region II.

3.3.1 Interval I ($t_0 < t < t_1$)

When the Active Switch S_3 turns-OFF, while S_2 remains ON, and the Active Switch S_1 turns-ON, the converter operates with the equivalent circuit shown in Figure 21a. The Interval I consists of a $L_r\left(C_{r_1}||C_{r_2}\right)$ resonant tank, analog to the description shown in the Section 2.2 and 3.2.1, where the major difference is the non-zero resonant capacitors' initial voltage condition V_{C0}. The resonance creates a sinusoidal shaped state variables $\boldsymbol{v}_{C_r}$ and $\boldsymbol{i}_{C_{r_n}}$, where $n \in \{1,2\}$, as described in Equations (2.28) and (2.30), respectively, in which the parameters are as described below.

$$V_{DM} = V_1 - V_2 = V_{IN} - 0 = V_{IN} \tag{3.23}$$

$$V_{C0} = V_{1II} \tag{3.24}$$

$$I_{C0} = 0 \tag{3.25}$$

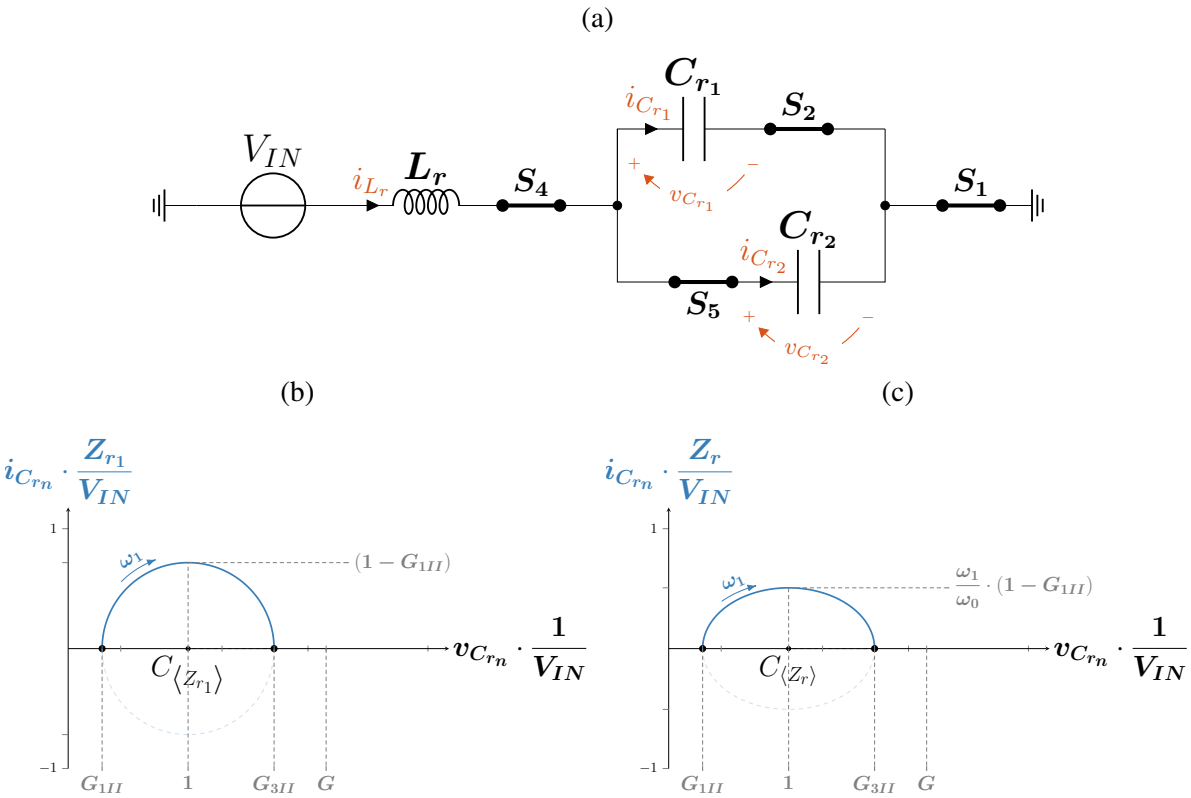
As a result, the resultant Z_{r_1}-normalized state variables are described in (3.26) and (3.27) while the state-plane trajectory, in the local resonant tank Z_{r_1} reference frame, is described as shown in (3.28) and Figure 21b, whereas the state-plane trajectory, in the system resonant tank Z_r reference frame, is described as shown in (3.29) and Figure 21c.

$$\overline{v_{C_r}(t)} = +1 - (1 - G_{1II})\cos(\omega_1 t) \tag{3.26}$$

$$\overline{\overline{i_{C_{r_n}}(t)}} = +\frac{1}{2}\cdot\overline{\overline{i_{L_r}(t)}} = +(1 - G_{1II})\sin(\omega_1 t) \tag{3.27}$$

$$\left(\overline{v_{C_r}(t)} - 1\right)^2 + \left(\overline{\overline{i_{C_r}(t)}}\right)^2 = 1 \tag{3.28}$$

Figure 21 – Resultant Characteristics based on the Operating Region II within Interval I:
(a) Equivalent Circuit.
(b) Geometrical Representation normalized by Z_{r_1} reference frame.
(c) Geometrical Representation normalized by Z_r reference frame.



$$\left(\overline{v_{C_r}(t)} - 1\right)^2 + \frac{\left(\overline{i_{C_r}(t)}\right)^2}{\left(\frac{\omega_1}{\omega_0}\right)^2} = (1 - G_{1II})^2 \tag{3.29}$$

By interpreting the state-plane trajectory, in Figure 21b, the Region II exhibits a lower radius trajectory, leading to a lower maximum Z_{r_1}-normalized peak current $MAX[\overline{\overline{I_{C_{rn}}}}]$ as well as a lower total resonant capacitors' voltage ripple. As a result, the maximum normalized peak voltage $MAX[\overline{V_{C_{rn}}}]$ value of G_{3II} no longer clamps to the Output Voltage V_{OUT}, during the Interval I, as exhibited within Region I. As a consequence, the boundary conditions for the full sinusoidal waveform is identified, being tied exclusively to the operating switching frequency which leads to shorter time intervals in between Transition States (11) and (21). As the goal is to operate the converter in DCM, the later is not addressed in the 4L-RFLCC analysis. Therefore, by assuming the current discontinuity, it shifts to an additional passive topological stage, initiating the Interval II.

3.3.2 Interval II ($t_1 < t < t_2$)

The Interval II is initiated by the current discontinuity, in which the Passive Switches $S_4 - S_5$ reverse biases, resulting in an idle state. The Interval II lasts until the Transition State (21) is triggered.

3.3.3 Interval III ($t_2 < t < t_3$)

When the Active Switch S_2 turns-OFF, while S_1 remains ON, and the Active Switch S_3 turns-ON, the converter operates with the equivalent circuit shown in Figure 22a. The Interval III consists of a $L_r\left(C_{r_1}C_{r_2}\right)$ resonant tank, analog to the description shown in the Section 2.3. As a result, the resonant tank is excited by V_{IN}, deriving a resonance activity under ω_2 trajectory velocity. Due to the Switches State, C_{r_1} transfers its energy to C_{r_2} additionally to the energy coming from the Input V_{IN}. The resonance creates a sinusoidal shaped state variables $v_{C_{r_1}}$, $v_{C_{r_2}}$ and i_{C_r}, as described in Equations (2.50) and (2.48), respectively, in which the parameters are as described below.

$$V_{DM} = V_1 - V_2 = V_{IN} - 0 = V_{IN} \tag{3.30}$$

$$V_{C0} = V_{3II} \tag{3.31}$$

$$I_{C0} = 0 \tag{3.32}$$

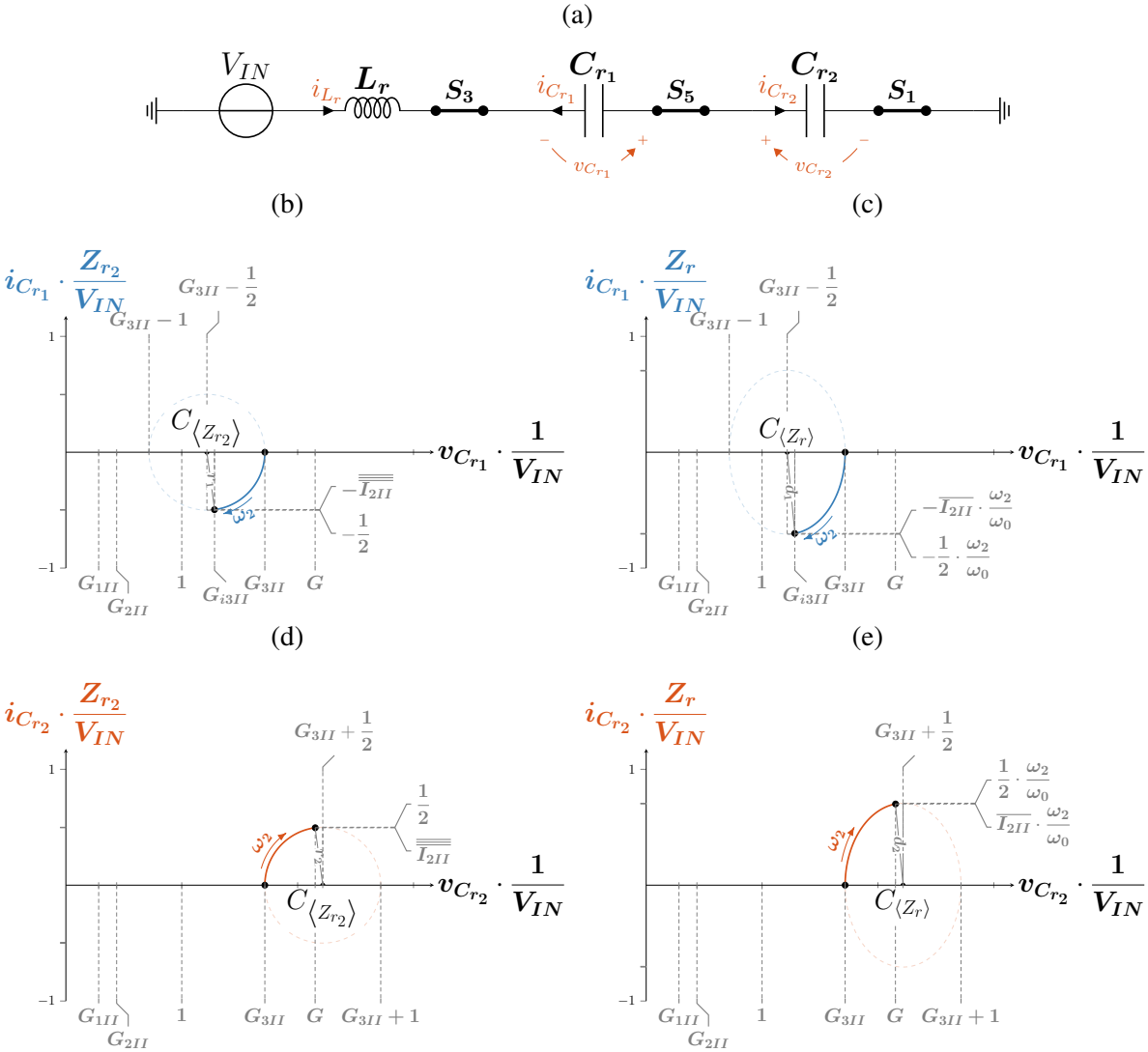
As a result, the resultant Z_{r_2}-normalized state variables are described in (3.33) and (3.34) while the state-plane trajectory, in the local resonant tank Z_{r_2} reference frame, is described as shown in (3.35) and Figure 22b, whereas the state-plane trajectory, in the system resonant tank Z_r reference frame, is described as shown in (3.36) and Figure 22c.

$$\overline{v_{C_{r_n}}(t)} = G_{3II} \pm \left(\frac{1}{2}\right) \cdot \left(1 - \cos\left(\omega_2 t\right)\right) \tag{3.33}$$

$$\overline{\overline{i_{C_{r_n}}(t)}} = \pm\overline{\overline{i_{L_r}(t)}} = \pm\left(\frac{1}{2}\right) \cdot \sin\left(\omega_2 t\right) \tag{3.34}$$

$$\left(\overline{v_{C_{r_n}}(t)} - \left(G_{3II} \pm \frac{1}{2}\right)\right)^2 + \left(\overline{\overline{i_{C_{r_n}}(t)}}\right)^2 = \left(\frac{1}{2}\right)^2 \tag{3.35}$$

Figure 22 – Resultant Characteristics based on the Operating Region II within Interval III:
(a) Equivalent Circuit.
(b) C_{r_1} Geometrical Representation normalized by Z_{r_2} reference frame.
(c) C_{r_1} Geometrical Representation normalized by Z_r reference frame.
(d) C_{r_2} Geometrical Representation normalized by Z_{r_2} reference frame.
(e) C_{r_2} Geometrical Representation normalized by Z_r reference frame.



$$\left(\overline{v_{C_{r_n}}(t)} - \left(G_{3II} \pm \frac{1}{2}\right)\right)^2 + \frac{\left(\overline{i_{C_{r_n}}(t)}\right)^2}{\left(\frac{\omega_2}{\omega_0}\right)^2} = \left(\frac{1}{2}\right)^2 \tag{3.36}$$

By interpreting the state-plane trajectory, in Figure 22b and 22d, due to the Input Voltage excitation V_{IN}, C_{r_2} is capable of charging by one normalized unit. Thus, it is maximum total voltage ripple $MAX[\overline{\Delta V_{C_{r_2}}} = 1]$. As a consequence, the boundary conditions for the full sinusoidal waveform is identified, being tied to V_{OUT} and the operating switching frequency. Within the Region III, V_{OUT} is expected to be within a normalized unit away from the G_{3II} value. Therefore, the maximum normalized peak voltage $MAX[\overline{V_{C_{r_2}}}]$ clamps to V_{OUT}, during the Interval III.

Once $\overline{v_{C_{r_2}}}$ reaches V_{OUT}, the Diode D_6 forward biases; thus, changing the operating behavior, initiating the Interval IV. Additionally, it indicates the resonant inductor current $\overline{\overline{\overline{i_{L_r}}}}$ final condition at t_3 of $\overline{\overline{I_{2II}}}$.

3.3.4 Interval IV ($t_3 < t < t_4$)

By forward biasing Diode D_6, $\overline{v_{C_{r_2}}}$ clamps to the V_{OUT}, driving C_{r_2} to an idle state whilst C_{r_1} remains discharging, deviating its charge transfer from C_{r_2} to the Output. As a result, the converter operates with the equivalent circuit shown in Figure 23a. The Interval IV consists of a $L_rC_{r_1}$ resonant tank, analog to the description shown in the Section 2.1. As a result, the resonant tank is excited by $V_{IN} - V_{OUT}$, deriving a resonance activity under ω_0 trajectory velocity.

The resonance creates a sinusoidal shaped state variables $\boldsymbol{v}_{C_{r_1}}$ and $\boldsymbol{i}_{C_{r_1}}$, as described in Equations (2.12) and (2.13), respectively, in which the parameters are as described below.

$$V_{DM} = V_1 - V_2 = V_{IN} - V_{OUT} \tag{3.37}$$

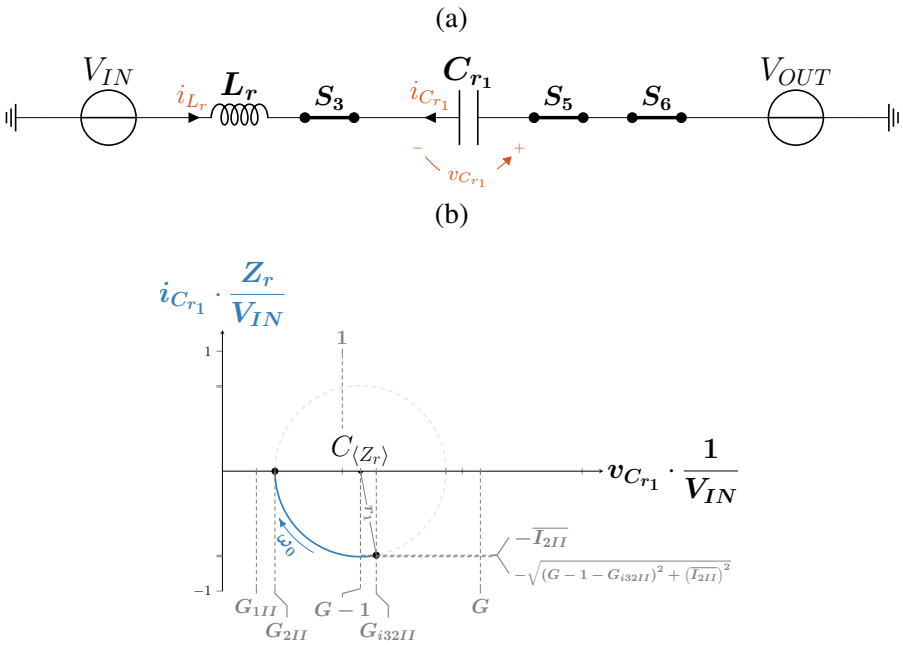
$$V_{C0} = V_{i32II} \tag{3.38}$$

$$I_{C0} = I_{2II} \tag{3.39}$$

As a result, the resultant Z_r-normalized state variables are described in (3.40) and (3.41) while the state-plane trajectory, in the local, and system, resonant tank Z_r reference frame, is described as shown in (3.42) and Figure 23b.

$$\overline{v_{C_{r_1}}(t)} = G - 1 - \left(G - 1 - G_{i32II}\right) \cdot \cos(\omega_0 t) - \overline{I_{2II}} \cdot \sin(\omega_0 t) \tag{3.40}$$

Figure 23 – Resultant Characteristics based on the Operating Region II within Interval IV:
(a) Equivalent Circuit.
(b) Geometrical Representation normalized by Z_r reference frame.



$$\overline{i_{C_{r_1}}(t)} = -\overline{i_{L_r}(t)} = -\left(G-1-G_{i32II}\right)\cdot\sin(\omega_0 t) + \overline{I_{2II}}\cdot\cos(\omega_0 t) \tag{3.41}$$

$$\left(\overline{v_{C_{r_1}}(t)} - (G-1)\right)^2 + \left(\overline{i_{C_{r_1}}(t)}\right)^2 = \left(G-1-G_{i32II}\right)^2 + \left(\overline{I_{2II}}\right)^2 \tag{3.42}$$

By interpreting the state-plane trajectory, in Figure 23b, the Interval IV exhibits a smaller total charge transfer to the Output due to the predecessor $L_r\left(C_{r_1}C_{r_2}\right)$ resonant tank activity where the total amount of charge is reduced compared to the total charge transferred during Interval I. As a consequence, the boundary conditions for the full resonant cycle, comprised by Interval III and IV, is identified by being dependent on the switching frequency, leading to the Transition State 31 prior to the realization of the full resonant cycle. As the goal is to operate the converter in DCM, the later is not addressed in the 4L-RFLCC analysis. Therefore, by assuming the current discontinuity, it shifts to an additional passive topological stage, initiating the Interval V.

3.3.5 Interval V ($t_4 < t < t_5$)

The Interval V is initiated by the current discontinuity, in which the Passive Switches $S_5 - S_6$ reverse biases, resulting in an idle state. The Interval V lasts until the Transition State 31 is triggered.

3.3.6 Interval VI ($t_5 < t < t_6$)

When the Active Switch S_1 turns-OFF, while S_3 remains ON, and the Active Switch S_2 turns-ON, the converter operates with the equivalent circuit shown in Figure 24a. The Interval VI consists of a $L_rC_{r_2}$ resonant tank, analog to the description shown in the Section 2.1. As a result, the resonant tank is excited by $V_{IN} - V_{OUT}$, deriving a resonance activity under ω_0 trajectory velocity. The resonance creates a sinusoidal shaped state variables $v_{C_{r_2}}$ and $i_{C_{r_2}}$, as described in Equations (2.12) and (2.13), respectively, in which the parameters are as described below.

$$V_{DM} = V_1 - V_2 = V_{IN} - V_{OUT} \tag{3.43}$$

$$V_{C0} = V_{OUT} \tag{3.44}$$

$$I_{C0} = 0 \tag{3.45}$$

As a result, the resultant Z_r-normalized state variables are described in (3.46) and (3.47) while the state-plane trajectory, in the local resonant tank Z_r reference frame, is described as shown in (3.48) and Figure 24b.

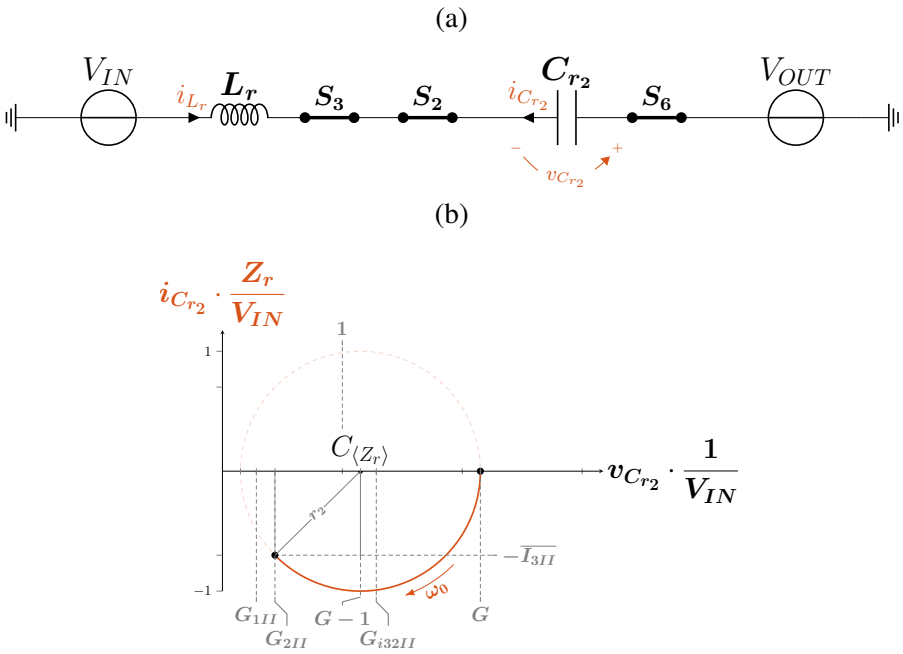
$$\overline{v_{C_{r_2}}(t)} = G - 1 + \cos(\omega_0 t) \tag{3.46}$$

$$\overline{i_{C_{r_2}}(t)} = -\overline{i_{L_r}(t)} = -\sin(\omega_0 t) \tag{3.47}$$

$$\left(\overline{v_{C_{r_2}}(t)} - (G-1)\right)^2 + \left(\overline{i_{C_{r_2}}(t)}\right)^2 = 1 \tag{3.48}$$

By interpreting the state-plane trajectory, in Figure 24b, the state variable $v_{C_{r_2}}$ exhibits a minimum normalized peak voltage $MIN[\overline{V_{C_{r_2}}}]$ value of G-2 and a maximum Z_{r_1}-normalized peak current $MAX[\overline{I_{C_{r_2}}}]$ value of 1. As a result, the boundary condition for the full sinusoidal waveform is identified, as well as the boundary condition for the transition to a passive topological stage given the V_{OUT} level and $v_{C_{r_1}}$ condition. Because of the total charge intake, during Interval I, is always lower than 1, as per Equation (3.29), the C_{r_2} trajectory encounter the C_{r_1} trajectory, which has been idling since Interval IV. Once $\overline{v_{C_{r_2}}}$ reaches G_{2II}, the Diode D_5 forward biases; thus, changing the operating behavior, initiating the Interval VII. Additionally, it indicates the resonant inductor current $\overline{i_{L_r}}$ final condition at t_6 of $\overline{I_{3II}}$.

Figure 24 – Resultant Characteristics based on the Operating Region II within Interval VI:
(a) Equivalent Circuit.
(b) Geometrical Representation normalized by Z_r reference frame.



3.3.7 Interval VII ($t_6 < t < t_7$)

By forward biasing Diode D_5, C_{r_1} starts to discharge, whilst C_{r_2} remains discharging, to the Output. As a result, the converter operates with the equivalent circuit shown in Figure 25a. The Interval VII consists of a $L_r\,(C_{r_1}||C_{r_2})$ resonant tank, analog to the description shown in the Section 2.2. As a result, the resonant tank is excited by $V_{IN} - V_{OUT}$, deriving a resonance activity under ω_1 trajectory velocity. The resonance creates a sinusoidal shaped state variables v_{C_r} and $i_{C_{r_n}}$, as described in Equations (2.28) and (2.30), respectively, in which the parameters are as described below.

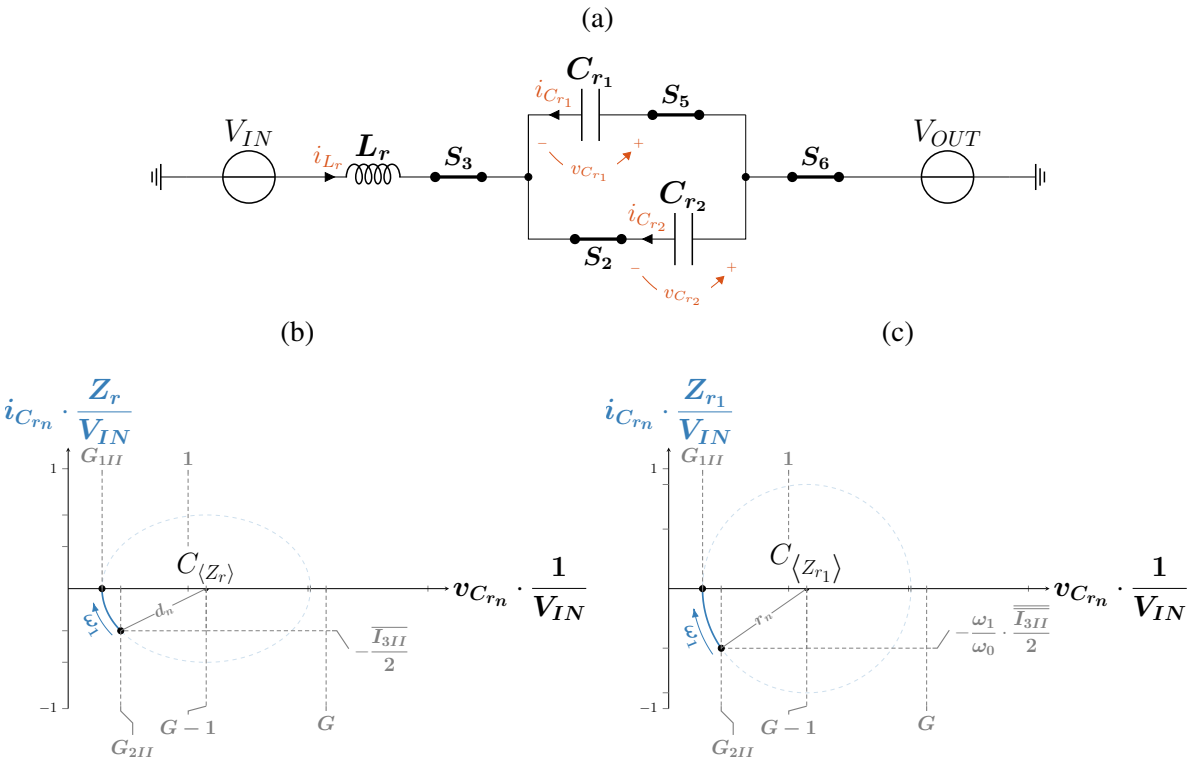
$$V_{DM} = V_1 - V_2 = V_{IN} - V_{OUT} \tag{3.49}$$

$$V_{C0} = V_{2II} \tag{3.50}$$

$$I_{C0} = \frac{I_{3II}}{2} \tag{3.51}$$

As a result, the resultant Z_{r_1}-normalized state variables are described in (3.52) and (3.53) while the state-plane trajectory, in the local resonant tank Z_{r_1} reference frame, is described as shown in (3.54) and Figure 25b, whereas the state-plane trajectory, in the system resonant tank Z_r reference frame, is described as shown in (3.55) and Figure 25c.

Figure 25 – Resultant Characteristics based on the Operating Region II within Interval VII:
(a) Equivalent Circuit.
(b) Geometrical Representation normalized by Z_{r_1} reference frame.
(c) Geometrical Representation normalized by Z_r reference frame.



$$\overline{v_{C_r}(t)} = G - 1 - \left(G - 1 - G_{2II}\right)\cos(\omega_1 t) - \left(\frac{1}{2}\right)^2 \overline{\overline{I_{3II}}} \cdot \sin(\omega_1 t) \tag{3.52}$$

$$\overline{\overline{i_{C_{rn}}(t)}} = -\frac{1}{2} \cdot \overline{\overline{i_{L_r}(t)}} = -\left(G - 1 - G_{2II}\right)\sin(\omega_1 t) + \left(\frac{1}{2}\right) \cdot \overline{\overline{I_{3II}}} \cdot \cos(\omega_1 t) \tag{3.53}$$

$$\left(\overline{v_{C_r}(t)} - (G-1)\right)^2 + \left(\overline{\overline{i_{C_r}(t)}}\right)^2 = \left(G - 1 - G_{2II}\right)^2 + \left(\frac{1}{2}\right)^2 \cdot \overline{\overline{I_{3II}}}^2 \tag{3.54}$$

$$\left(\overline{v_{C_r}(t)} - (G-1)\right)^2 + \frac{\left(\overline{i_{C_r}(t)}\right)^2}{\left(\frac{\omega_1}{\omega_0}\right)^2} = \left(G - 1 - G_{2II}\right)^2 + \left(\frac{1}{2}\right)^2 \cdot \left(\frac{\omega_0}{\omega_1}\right)^2 \cdot \overline{I_{3II}}^2 \tag{3.55}$$

The interpreting of the state-plane trajectory, in Figure 25c, is not as clear due to I_{C0}. However, in order to sustain a steady-state condition, C_{r_1} and C_{r_2} shall discharge its energy and return to the t_0 initial conditions. Therefore, by assuming the current discontinuity, it shifts to an additional passive topological stage, initiating the Interval VIII.

3.3.8 Interval VIII ($t_7 < t < t_8$)

The Interval VIII is initiated by the current discontinuity, in which the Passive Switches $S_5 - S_6$ reverse biases, resulting in an idle state. The Interval V lasts until the Transition State (11) is triggered and a new cycle initiates.

3.3.9 Summary of Operation

Table 4 – Summary of the different topological stages and their characteristics for the 4LRFLC topology under Region II condition.

Topological Stage	**Switches State**			**L_r and C_r State**			**Operating Mode**
	S_1	S_2	S_3	L_r	C_{r1}	C_{r2}	
1st	ON	ON	OFF	$\nearrow$	$\nearrow$	$\nearrow$	*Resonant* (ω_1)
2nd	ON	ON	OFF	$\rightarrow$	$\rightarrow$	$\rightarrow$	*Idle*
3rd	ON	OFF	ON	$\nearrow$	$\searrow$	$\nearrow$	*Resonant* (ω_2)
4th	ON	OFF	ON	$\nearrow$	$\searrow$	$\rightarrow$	*Resonant* (ω_0)
5th	ON	OFF	ON	$\rightarrow$	$\rightarrow$	$\rightarrow$	*Idle*
6th	OFF	ON	ON	$\nearrow$	$\rightarrow$	$\searrow$	*Resonant* (ω_0)
7th	OFF	ON	ON	$\nearrow$	$\searrow$	$\searrow$	*Resonant* (ω_1)
8th	OFF	ON	ON	$\rightarrow$	$\rightarrow$	$\rightarrow$	*Idle*

The Table 4 summarizes the different topological stages, and their main characteristics, which are illustrated in the Z_r State-Plane Trajectories in Figure 26 and in the time-domain state variables, shown in Figure 27. Shifting from Region I to Region II has shown to have a major effect on how the coupling from C_{r_1} and C_{r_2} to each other as well as to the Output. C_{r_1} introduced a sufficient voltage condition that prevents it from falling to zero, leading to a reduced current stress within every Interval.

Figure 26 – Normalized State-Plane Trajectory under Operating Region II for:
(a) C_{r_1}
(b) C_{r_2}

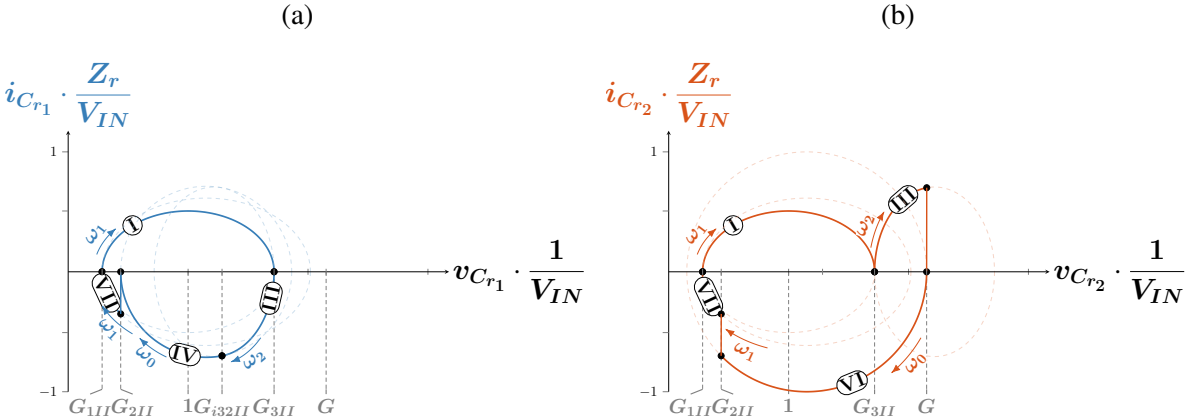
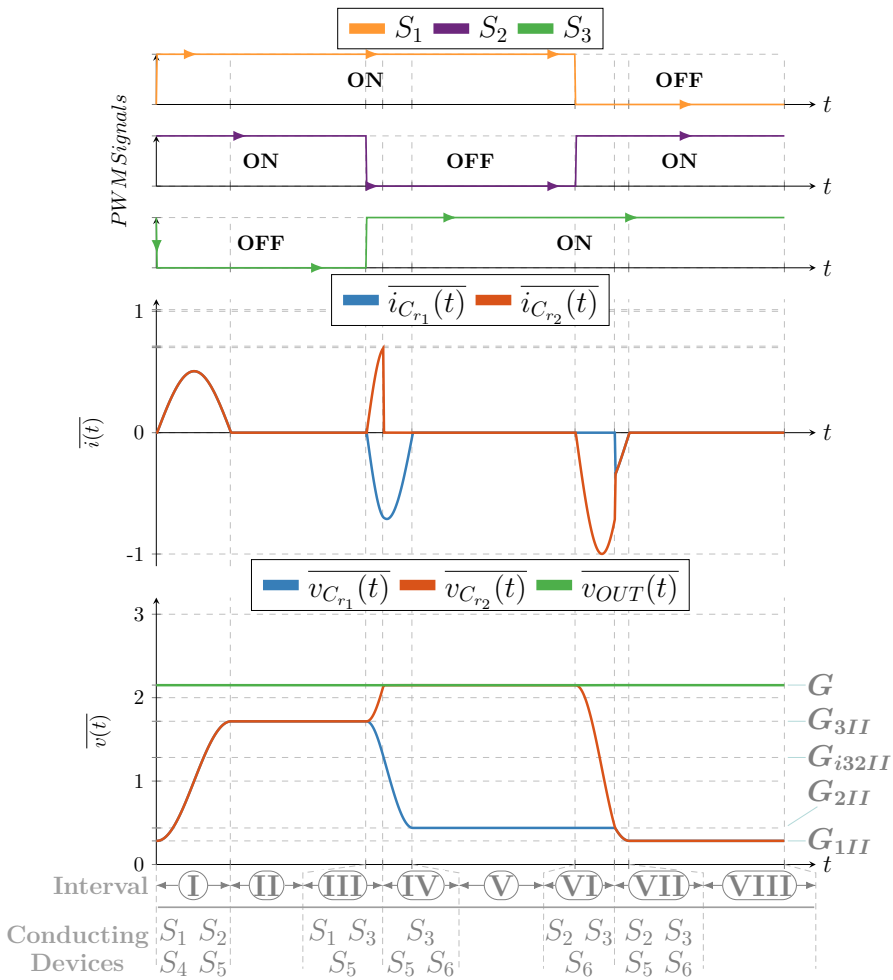


Figure 27 – Normalized Time-Domain State Variables for Operating Region II.



3.4 REGION III

By considering the Region II's key characteristics, the boundary condition is C_{r_2} clamping to V_{OUT}, as described within Section 3.3.3. The clamping mechanism is dependent on the total charge transferred during the Interval I. Therefore, as derived in Equation (3.29), the maximum charge transferred is reduced, leading to a proportional reduction in $MAX[V_{C_r}(t_1)]$. As a result, the Interval III exhibits a larger headroom for the resonant cycle upon the Transition State **21**. Symmetrically, as V_{OUT} increases, the Interval VI also exhibits a larger headroom for the resonant cycle, upon the Transition State **31**, due to a constant total charge transfer within Interval VI. Therefore, upon the boundary condition when the Interval III and VI exhibits a full resonant cycle, the 4L-RFLCC modifies its behavior and the Operating Region III begins. Given an increment in V_1 and V_{OUT}, based on the operating condition, the following Section describe the converter's behavior within the Operating Region III.

3.4.1 Interval I ($t_0 < t < t_1$)

When the Active Switch S_3 turns-OFF, while S_2 remains ON, and the Active Switch S_1 turns-ON, the converter operates with the equivalent circuit shown in Figure 28a. The Interval I consists of a $L_rC_{r_1}$ resonant tank, analog to the description shown in the Section 2.1, where the major difference is the C_{r_1} C_{r_2} resonant capacitors' initial voltage conditions V_{C0}, keeping the Diode D_5 reverse-biased. As a result, the resonant tank is excited by V_{IN}, deriving a resonance activity under ω_0 trajectory velocity. The resonance creates a sinusoidal shaped state variables $v_{C_{r_1}}$ and $i_{C_{r_1}}$, as described in Equations (2.12) and (2.13), respectively, in which the parameters are as described below.

$$V_{DM} = V_1 - V_2 = V_{IN} - 0 = V_{IN} \tag{3.56}$$

$$V_{C0} = V_{1III} \tag{3.57}$$

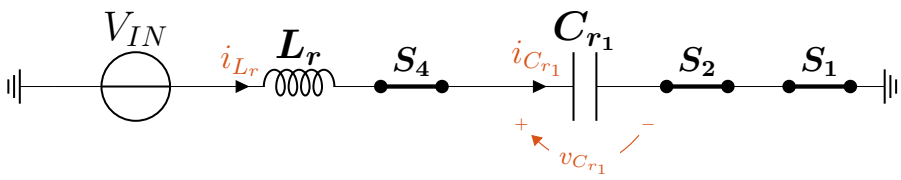
$$I_{C0} = 0 \tag{3.58}$$

As a result, the resultant Z_r-normalized state variables are described in (3.59) and (3.60) while the state-plane trajectory, in the local, and system, resonant tank Z_r reference frame, is described as shown in (3.61) and Figure 28b.

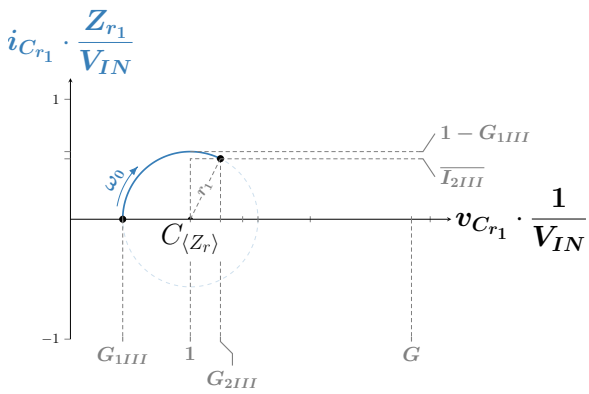
$$\overline{v_{C_{r_1}}(t)} = 1 - \left(1 - G_{1III}\right) \cdot \cos(\omega_0 t) \tag{3.59}$$

Figure 28 – Resultant Characteristics based on the Operating Region III within Interval I:
(a) Equivalent Circuit.
(b) Geometrical Representation normalized by Z_r reference frame.

(a)



(b)



$$\overline{i_{C_{r_1}}(t)} = +\overline{i_{L_r}(t)} = +\left(1 - G_{1III}\right) \cdot \sin(\omega_0 t) \tag{3.60}$$

$$\left(\overline{v_{C_{r_1}}(t)} - 1\right)^2 + \left(\overline{i_{C_{r_1}}(t)}\right)^2 = \left(1 - G_{1III}\right)^2 \tag{3.61}$$

By interpreting the state-plane trajectory, in Figure 28b, due to the Input Voltage excitation V_{IN}, C_{r_1} is capable of charging by one normalized unit. Thus, it is maximum total voltage ripple $MAX[\overline{\Delta V_{C_{r_1}}} = 1]$. As a consequence, the boundary conditions for the full sinusoidal waveform is identified, being tied to V_{2III} and the operating switching frequency. Within the Region III, G_{2III} is expected to be within a normalized unit away from the G_{3III} value. Therefore, the maximum normalized peak voltage $MAX[\overline{V_{C_{r_1}}}]$ clamps to V_{3III}, during the Interval I.

Once $\overline{v_{C_{r_1}}}$ reaches V_{3III}, the Diode D_5 forward biases; thus, changing the operating behavior, initiating the Interval II. Additionally, it indicates the resonant inductor current $\overline{\overline{i_{L_r}}}$ final condition at t_1 of $\overline{\overline{I_{2III}}}$.

3.4.2 Interval II ($t_1 < t < t_2$)

As per the passive topological stage transition to Interval II, the converter operates with the equivalent circuit shown in Figure 29a. The Interval II consists of a $L_r\,(C_{r_1}||C_{r_2})$ resonant tank, analog to the description shown in the Section 2.2 and 3.3.1, where the major difference is

the non-zero resonant capacitors' initial current condition I_{C0}. The resonance creates a sinusoidal shaped state variables v_{C_r} and $i_{C_{r_n}}$, where $n \in \{1,2\}$, as described in Equations (2.28) and (2.30), respectively, in which the parameters are as described below.

$$V_{DM} = V_1 - V_2 = V_{IN} - 0 = V_{IN} \tag{3.62}$$

$$V_{C0} = V_{1II} \tag{3.63}$$

$$I_{C0} = \frac{I_{2III}}{2} \tag{3.64}$$

As a result, the resultant Z_{r_1}-normalized state variables are described in (3.65) and (3.66) while the state-plane trajectory, in the local resonant tank Z_{r_1} reference frame, is described as shown in (3.67) and Figure 29b, whereas the state-plane trajectory, in the system resonant tank Z_r reference frame, is described as shown in (3.68) and Figure 29c.

$$\overline{v_{C_r}(t)} = +1 - (1 - G_{1III})\cos(\omega_1 t) \tag{3.65}$$

$$\overline{\overline{i_{C_{r_n}}(t)}} = +\frac{1}{2} \cdot \overline{\overline{i_{L_r}(t)}} = +(1 - G_{1III})\sin(\omega_1 t) \tag{3.66}$$

$$\left(\overline{v_{C_r}(t)} - 1\right)^2 + \left(\overline{\overline{i_{C_r}(t)}}\right)^2 = 1 \tag{3.67}$$

$$\left(\overline{v_{C_r}(t)} - 1\right)^2 + \frac{\left(\overline{i_{C_r}(t)}\right)^2}{\left(\frac{\omega_1}{\omega_0}\right)^2} = (1 - G_{1III})^2 \tag{3.68}$$

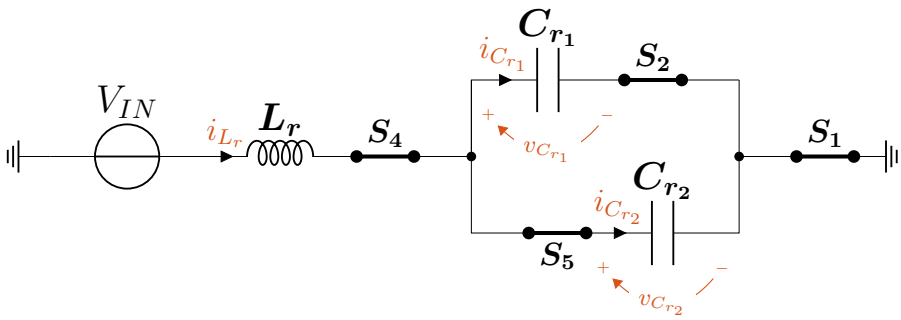
The interpreting of the state-plane trajectory, in Figure 29c, is not as clear due to I_{C0}. However, in order to sustain the DCM goal, C_{r_1} and C_{r_2} shall discharge its energy. By assuming the current discontinuity, it shifts to an additional passive topological stage, initiating the Interval III.

3.4.3 Interval III ($t_2 < t < t_3$)

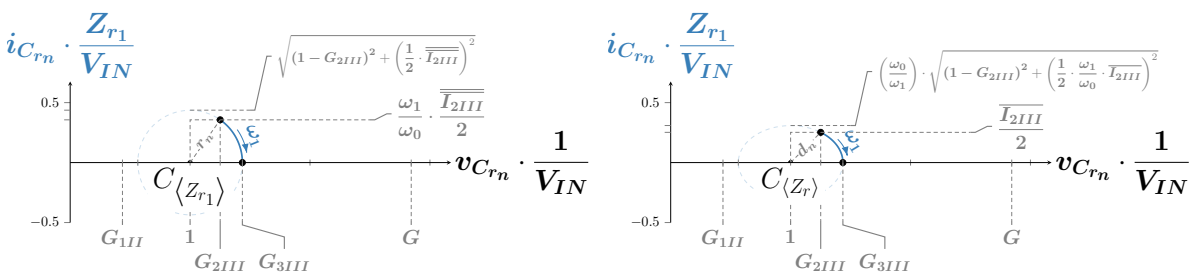
The Interval III is initiated by the current discontinuity, in which the Passive Switches $S_4 - S_5$ reverse bias, resulting in an idle state. The Interval III lasts until the Transition State **21** is triggered.

Figure 29 – Resultant Characteristics based on the Operating Region III within Interval II:
(a) Equivalent Circuit.
(b) Geometrical Representation normalized by Z_{r_1} reference frame.
(c) Geometrical Representation normalized by Z_r reference frame.

(a)



(b) (c)



3.4.4 Interval IV ($t_3 < t < t_4$)

When the Active Switch S_2 turns-OFF, while S_1 remains ON, and the Active Switch S_3 turns-ON, the converter operates with the equivalent circuit shown in Figure 30a. The Interval IV consists of a $L_r\,(C_{r_1}C_{r_2})$ resonant tank, analog to the description shown in the Section 2.3. As a result, the resonant tank is excited by V_{IN}, deriving a resonance activity under ω_2 trajectory velocity. Due to the Switches State, C_{r_1} transfers its energy to C_{r_2} additionally to the energy coming from the Input V_{IN}. The resonance creates a sinusoidal shaped state variables $v_{C_{r_1}}$, $v_{C_{r_2}}$ and i_{C_r}, as described in Equations (2.50) and (2.48), respectively, in which the parameters are as described below.

$$V_{DM} = V_1 - V_2 = V_{IN} - 0 = V_{IN} \tag{3.69}$$

$$V_{C0} = V_{3III} \tag{3.70}$$

$$I_{C0} = 0 \tag{3.71}$$

As a result, the resultant Z_{r_2}-normalized state variables are described in (3.72) and (3.73) while the state-plane trajectory, in the local resonant tank Z_{r_2} reference frame, is described as shown in (3.74) and Figure 30b, whereas the state-plane trajectory, in the system resonant tank Z_r reference frame, is described as shown in (3.75) and Figure 30c.

$$\overline{v_{C_{r_n}}(t)} = G_{3III} \pm \left(\frac{1}{2}\right) \cdot \left(1 - \cos\left(\omega_2 t\right)\right) \tag{3.72}$$

$$\overline{\overline{\overline{i_{C_{r_n}}(t)}}} = \pm \overline{\overline{\overline{i_{L_r}(t)}}} = \pm \left(\frac{1}{2}\right) \cdot \sin\left(\omega_2 t\right) \tag{3.73}$$

$$\left(\overline{v_{C_{r_n}}(t)} - \left(G_{3III} \pm \frac{1}{2}\right)\right)^2 + \left(\overline{\overline{\overline{i_{C_{r_n}}(t)}}}\right)^2 = \left(\frac{1}{2}\right)^2 \tag{3.74}$$

$$\left(\overline{v_{C_{r_n}}(t)} - \left(G_{3III} \pm \frac{1}{2}\right)\right)^2 + \frac{\left(\overline{i_{C_{r_n}}(t)}\right)^2}{\left(\frac{\omega_2}{\omega_0}\right)^2} = \left(\frac{1}{2}\right)^2 \tag{3.75}$$

By interpreting the state-plane trajectory, in Figure 30b and 30d, due to the Input Voltage excitation V_{IN}, C_{r_2} is capable of charging by one normalized unit while C_{r_1} discharge the same amount. Thus, it is maximum total voltage ripple $MAX[\overline{\Delta V_{C_{r_n}}} = \pm 1]$. As a consequence, the boundary conditions for the full sinusoidal waveform is identified, being tied to the operating switching frequency as V_{1III} and V_{OUT} have introduced enough headroom for the full resonance. Thus, the boundary relies on the Transition State **31**. As the goal is to operate the converter in DCM, the later is not addressed in the 4L-RFLCC analysis. Therefore, by assuming the current discontinuity, it shifts to an additional passive topological stage, initiating the Interval V.

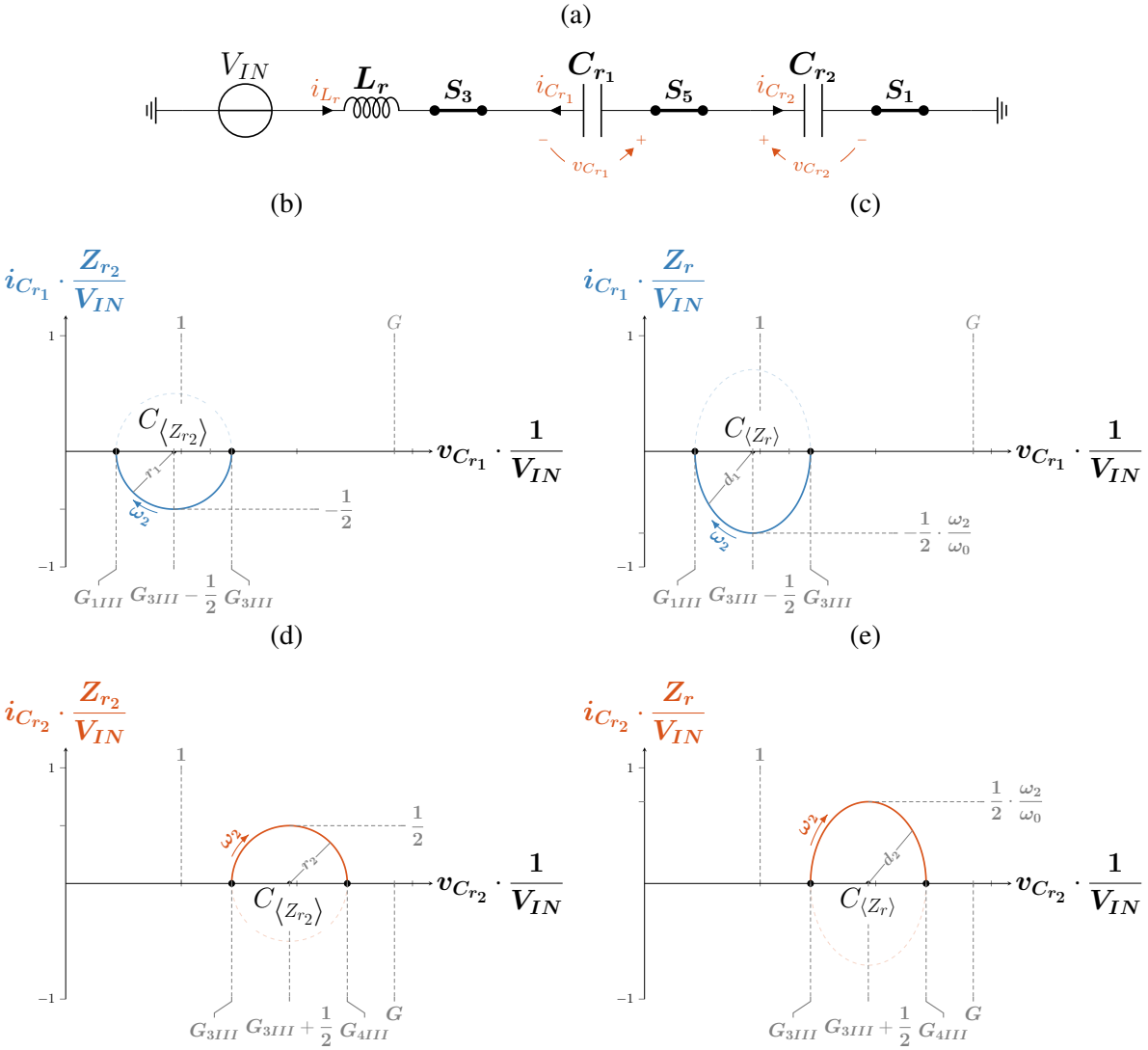
3.4.5 Interval V ($t_4 < t < t_5$)

The Interval V is initiated by the current discontinuity, in which the Passive Switch S_5 reverse biases, resulting in an idle state. The Interval III lasts until the Transition State **21** is triggered.

3.4.6 Interval VI ($t_5 < t < t_6$)

When the Active Switch S_1 turns-OFF, while S_3 remains ON, and the Active Switch S_2 turns-ON, the converter operates with the equivalent circuit shown in Figure 31a. The Interval VI consists of a $L_r C_{r_2}$ resonant tank, analog to the description shown in the Section 2.1. As a result, the resonant tank is excited by $V_{IN} - V_{OUT}$, deriving a resonance activity under ω_0 trajectory

Figure 30 – Resultant Characteristics based on the Operating Region III within Interval IV:
(a) Equivalent Circuit.
(b) C_{r_1} Geometrical Representation normalized by Z_{r_2} reference frame.
(c) C_{r_1} Geometrical Representation normalized by Z_r reference frame.
(d) C_{r_2} Geometrical Representation normalized by Z_{r_2} reference frame.
(e) C_{r_2} Geometrical Representation normalized by Z_r reference frame.



velocity. The resonance creates a sinusoidal shaped state variables $v_{C_{r_2}}$ and $i_{C_{r_2}}$, as described in Equations (2.12) and (2.13), respectively, in which the parameters are as described below.

$$V_{DM} = V_1 - V_2 = V_{IN} - V_{OUT} \tag{3.76}$$

$$V_{C0} = V_{4III} \tag{3.77}$$

$$I_{C0} = 0 \tag{3.78}$$

As a result, the resultant Z_r-normalized state variables are described in (3.79) and (3.80) while the state-plane trajectory, in the local resonant tank Z_r reference frame, is described as shown in (3.81) and Figure 31b.

$$\overline{v_{C_{r_2}}(t)} = G - 1 - (G - 1 - G_{4III}) \cdot \cos(\omega_0 t) \tag{3.79}$$

$$\overline{i_{C_{r_2}}(t)} = -\overline{i_{L_r}(t)} = -(G - 1 - G_{4III}) \cdot \sin(\omega_0 t) \tag{3.80}$$

$$\left(\overline{v_{C_{r_2}}(t)} - (G-1)\right)^2 + \left(\overline{i_{C_{r_2}}(t)}\right)^2 = G_{4III} - G + 1 \tag{3.81}$$

By interpreting the state-plane trajectory, in Figure 31b, the state variable $v_{C_{r_2}}$ exhibits a reduced total charge transferred thanks to the decoupling in between C_{r_2} and the Output, which corresponds to the variable G outgrowing G_{4III}. As a result, the boundary condition for the full sinusoidal waveform is identified, as well as the boundary condition for the transition to a passive topological stage given the $v_{C_{r_1}}$ condition. Due to the reduced total charge transferred, C_{r_2} trajectory does not encounter C_{r_1}. Therefore, the full resonance cycle is fulfilled during Interval VI. Once i_{L_r} reaches zero, the discontinuity initiates the Interval VII.

3.4.7 Interval VII ($t_6 < t < t_7$)

The Interval VII is initiated by the current discontinuity, in which the Passive Switch S_6 reverse biases, resulting in an idle state. The Interval VII lasts until the Transition State **11** is triggered and a new cycle initiates.

Figure 31 – Resultant Characteristics based on the Operating Region III within Interval VI:
(a) Equivalent Circuit.
(b) Geometrical Representation normalized by Z_r reference frame.

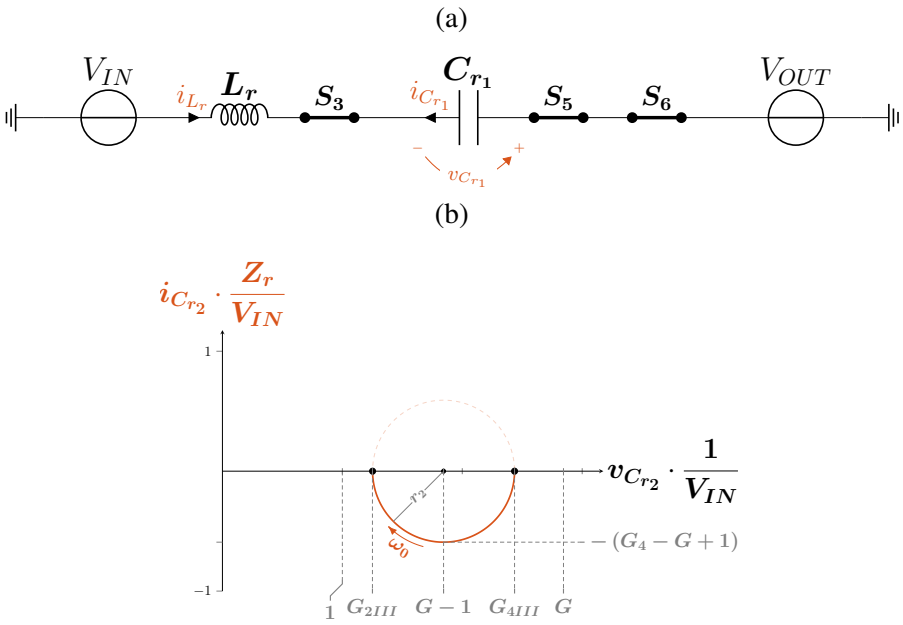


Table 5 – Summary of the different topological stages and their characteristics for the 4LRFLC topology under Region III condition.

Topological Stage	Switches State			L_r and C_r State			Operating Mode
	S_1	S_2	S_3	L_r	C_{r1}	C_{r2}	
1st	ON	ON	OFF	↗	↗	→	*Resonant* (ω_0)
2nd	ON	ON	OFF	↗	↗	↗	*Resonant* (ω_1)
3rd	ON	ON	OFF	→	→	→	*Idle*
4th	ON	OFF	ON	↗	↘	↗	*Resonant* (ω_2)
5th	ON	OFF	ON	→	→	→	*Idle*
6th	OFF	ON	ON	↗	→	↘	*Resonant* (ω_0)
7th	OFF	ON	ON	→	→	→	*Idle*

3.4.8 Summary of Operation

The Table 5 summarizes the different topological stages, and their main characteristics, which are illustrated in the Z_r State-Plane Trajectories in Figure 32 and in the time-domain state variables, shown in Figure 33. Shifting from Region II to Region III has shown to further extend the effect on how the coupling from C_{r_1} and C_{r_2} to each other as well as to the Output, emphasizing the possibility of fulfilling a full resonance, simplifying the operation as well as the analysis. C_{r_1} and C_{r_2} introduced a sufficient voltage condition that prevents it from falling to zero and prevents it from clamping to the Output, respectively, leading to a reduced current stress within every Interval.

Figure 32 – Normalized State-Plane Trajectory under Operating Region III for:
(a) C_{r_1}
(b) C_{r_2}

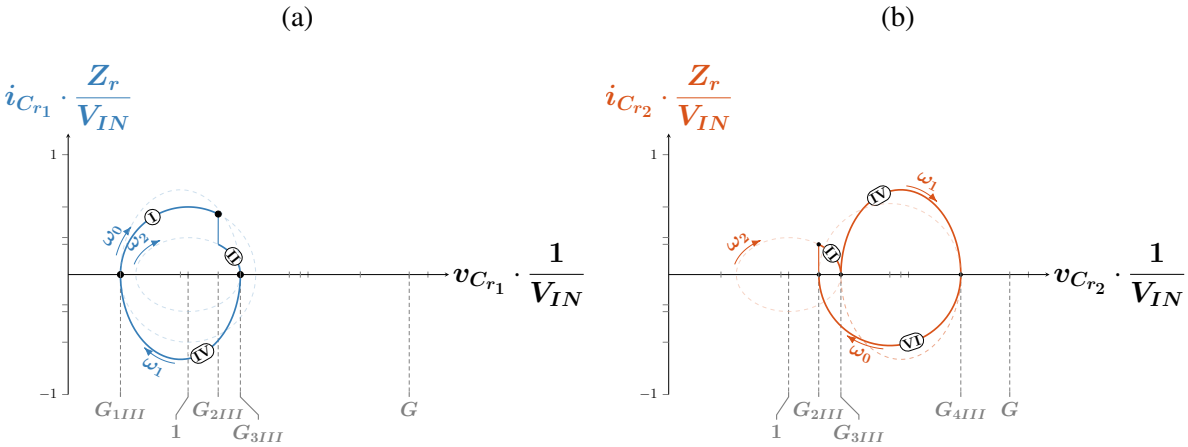
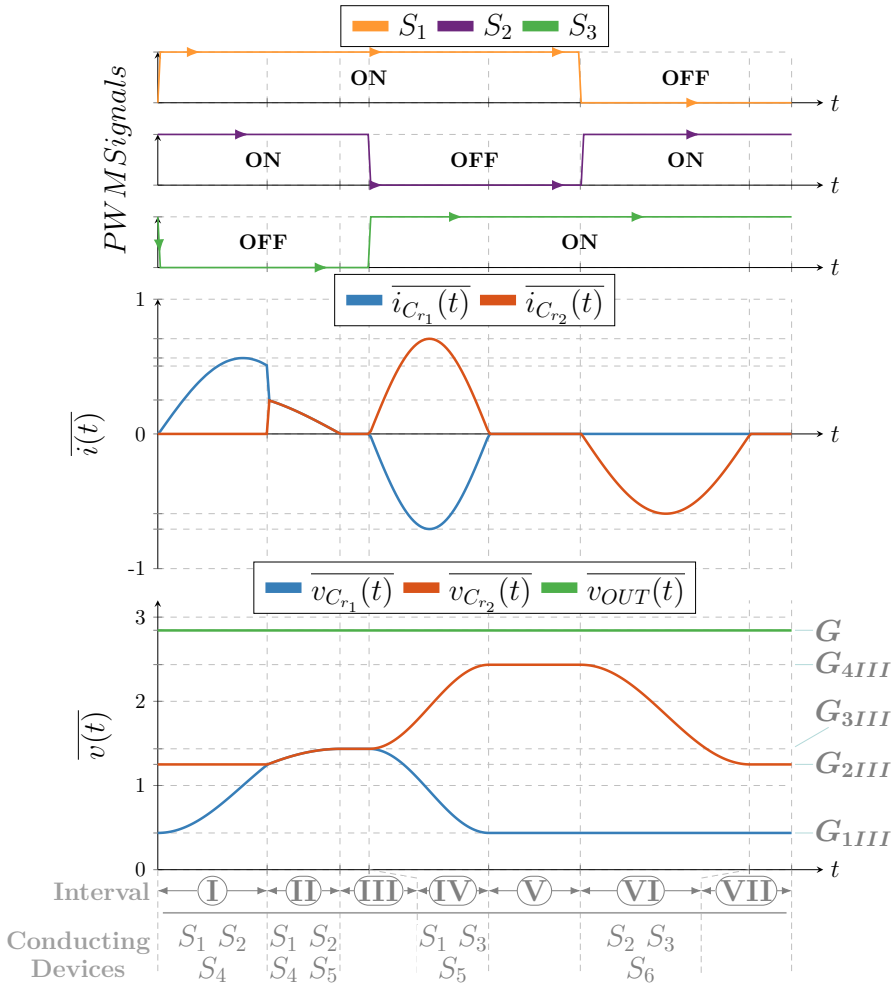


Figure 33 – Normalized Time-Domain State Variables for Operating Region III.



3.5 REGION IV

3.5.1 Interval I ($t_0 < t < t_1$)

When the Active Switch S_3 turns-OFF, while S_2 remains ON, and the Active Switch S_1 turns-ON, the converter operates with the equivalent circuit shown in Figure 34a. The Interval I consists of a $L_rC_{r_1}$ resonant tank, analog to the description shown in the Section 2.1, identical to the operating behavior from Region III. As a result, the resonant tank is excited by V_{IN}, deriving a resonance activity under ω_0 trajectory velocity. The resonance creates a sinusoidal shaped state variables $v_{C_{r_1}}$ and $i_{C_{r_1}}$, as described in Equations (2.12) and (2.13), respectively, in which the parameters are as described below.

$$V_{DM} = V_1 - V_2 = V_{IN} - 0 = V_{IN} \tag{3.82}$$

$$V_{C0} = V_{1IV} \tag{3.83}$$

$$I_{C0} = 0 \tag{3.84}$$

As a result, the resultant Z_r-normalized state variables are described in (3.85) and (3.86) while the state-plane trajectory, in the local, and system, resonant tank Z_r reference frame, is described as shown in (3.87) and Figure 34b.

$$\overline{v_{C_{r_1}}(t)} = 1 - \left(1 - G_{1IV}\right) \cdot \cos(\omega_0 t) \tag{3.85}$$

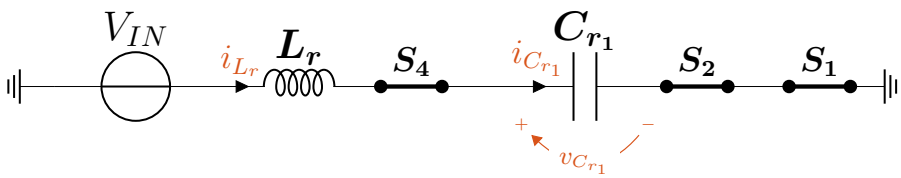
$$\overline{i_{C_{r_1}}(t)} = +\overline{i_{L_r}(t)} = +\left(1 - G_{1IV}\right) \cdot \sin(\omega_0 t) \tag{3.86}$$

$$\left(\overline{v_{C_{r_1}}(t)} - 1\right)^2 + \left(\overline{i_{C_{r_1}}(t)}\right)^2 = \left(1 - G_{1IV}\right)^2 \tag{3.87}$$

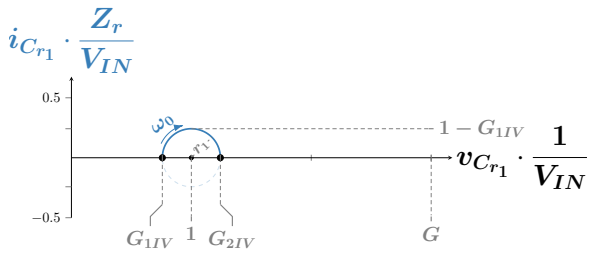
By interpreting the state-plane trajectory, in Figure 34b, due to the non-zero V_{C0}, shown in (3.83), C_{r_1} is capable of charging by less than one normalized unit. Thus, it is maximum total voltage ripple $MAX[\overline{\Delta V_{C_{r_1}}} \leq 1]$. Due to the topology connections, the boundary conditions for the full sinusoidal waveform are identified, being tied to V_{2IV}, given the Diode D_5's Status, and the operating switching frequency. As C_{r_2} is fully voltage-decoupled from C_{r_1}, the first is no longer a valid boundary condition. Therefore, the operating switching frequency f_{sw} is the only restriction. By considering the goal of maintaining DCM, $i_{L_r} \to 0$ by t_1; thus, altering the converter's operating principles and initiating a Passive Topological Stage.

Figure 34 – Resultant Characteristics based on the Operating Region IV within Interval I:
(a) Equivalent Circuit.
(b) Geometrical Representation normalized by Z_r reference frame.

(a)



(b)



3.5.2 Interval II ($t_1 < t < t_2$)

The Interval II is initiated by the current discontinuity, in which the Passive Switch S_4 reverse biases, resulting in an idle state. The Interval II lasts until the Transition State (21) is triggered. Additionally, Interval II is prompt to be null due to the synchronization of resonant frequency ω_0 and $\frac{2}{3} \cdot f_{sw}$ when the condition $\frac{2}{3} \cdot f_{sw} = \frac{\omega_0}{2\pi}$ is met.

3.5.3 Interval III ($t_2 < t < t_3$)

When the Active Switch S_2 turns-OFF, while S_1 remains ON, and the Active Switch S_3 turns-ON, the converter operates with the equivalent circuit shown in Figure 35a. The Interval III consists of a $L_r\,(C_{r_1}C_{r_2})$ resonant tank, analog to the description shown in the Section 2.3, and Section 3.4.4, with the exception of C_{r_1} and C_{r_2}'s initial voltage condition $V_{C0_{\langle C_{rn} \rangle}}$, shown in (3.89) and (3.90), respectively, differing from each other. As a result, the resonant tank is excited by V_{IN} and attenuated by $\mp V_{C0_{\langle C_{rn} \rangle}}$, deriving a resonance activity under ω_2 trajectory velocity. Due to the Switches State, C_{r_1} transfers its energy to C_{r_2} additionally to the energy coming from the Input V_{IN}. The resonance creates a sinusoidal shaped state variables $v_{C_{r_1}}$, $v_{C_{r_2}}$ and i_{C_r}, as described in Equations (2.50) and (2.48), respectively, in which the parameters are as described below.

$$V_{DM} = V_1 - V_2 = V_{IN} - 0 = V_{IN} \tag{3.88}$$

$$V_{C0_{\langle C_{r_1} \rangle}} = V_{2IV} \tag{3.89}$$

$$V_{C0_{\langle C_{r_2} \rangle}} = V_{3IV} \tag{3.90}$$

$$I_{C0} = 0 \tag{3.91}$$

As a result, the resultant Z_{r_2}-normalized state variables are described in (3.92), (3.93) and (3.94) while the state-plane trajectory, in the local resonant tank Z_{r_2} reference frame, is described as shown in (3.95), and (3.96), and Figure 35b and 35d, whereas the state-plane trajectory, in the system resonant tank Z_r reference frame, is described as shown in (3.97), and (3.98), and Figure 35c and 30e.

$$\overline{v_{C_{r_1}}(t)} = G_{2IV} - \left(\frac{1}{2}\right) \cdot \left(1 + G_{2IV} - G_{3IV}\right)\left(1 - \cos\left(\omega_2 t\right)\right) \tag{3.92}$$

$$\overline{v_{C_{r_2}}(t)} = G_{2IV} + \left(\frac{1}{2}\right) \cdot \left(1 + G_{2IV} - G_{3IV}\right) \cdot \left(1 - \cos\left(\omega_2 t\right)\right) \tag{3.93}$$

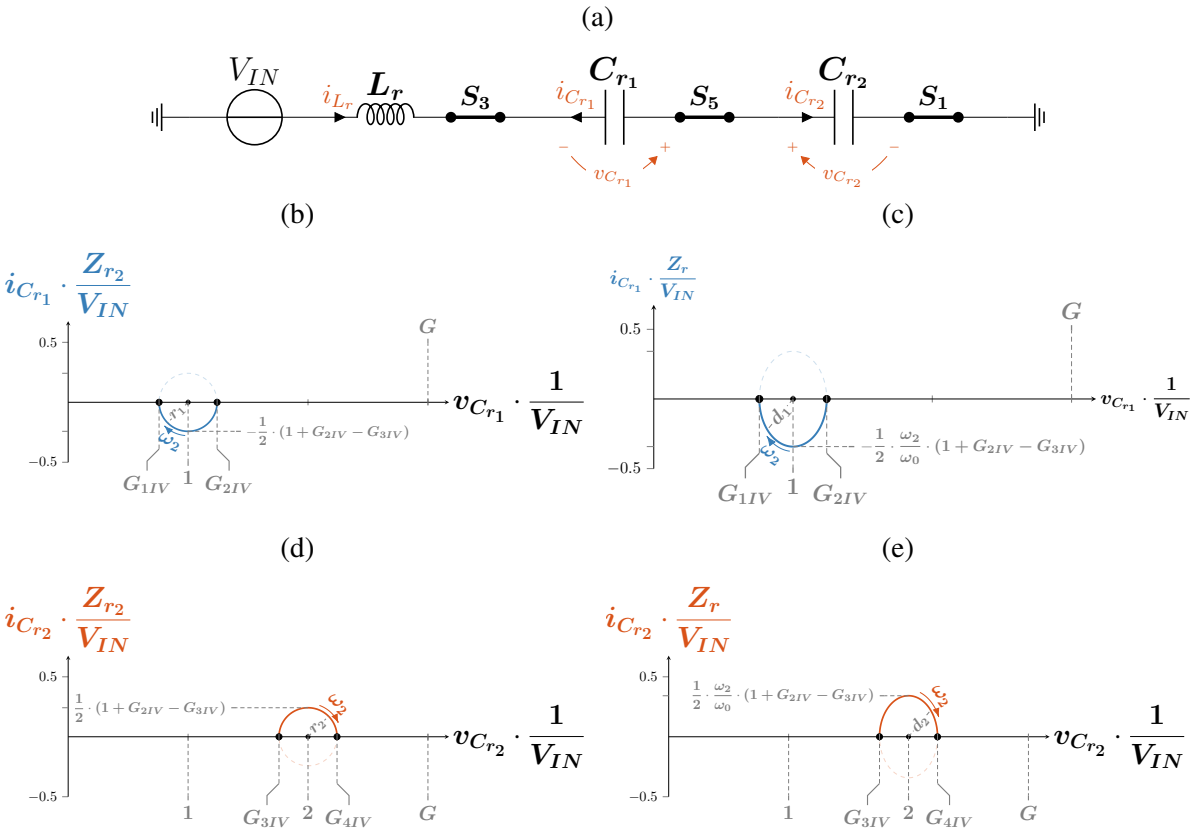
$$\overline{\overline{i_{C_{r_n}}(t)}} = \pm \overline{\overline{i_{L_r}(t)}} = \pm \left(\frac{1}{2}\right) \cdot \left(1 + G_{2IV} - G_{3IV}\right) \cdot \sin\left(\omega_2 t\right) \tag{3.94}$$

$$\begin{aligned} &\left(\overline{v_{C_{r_1}}(t)} - \left(G_{2IV} + \frac{1}{2} \cdot \left(1 + G_{2IV} - G_{3IV}\right)\right)\right)^2 + \left(\overline{\overline{i_{C_{r_1}}(t)}}\right)^2 = \\ &= \left(\frac{1}{2}\right)^2 \cdot \left(1 + G_{2IV} - G_{3IV}\right)^2 \end{aligned} \tag{3.95}$$

$$\begin{aligned} &\left(\overline{v_{C_{r_2}}(t)} - \left(G_{3IV} - \frac{1}{2} \cdot \left(1 + G_{2IV} - G_{3IV}\right)\right)\right)^2 + \left(\overline{\overline{i_{C_{r_2}}(t)}}\right)^2 = \\ &= \left(\frac{1}{2}\right)^2 \cdot \left(1 + G_{2IV} - G_{3IV}\right)^2 \end{aligned} \tag{3.96}$$

$$\begin{aligned} &\left(\overline{v_{C_{r_1}}(t)} - \left(G_{2IV} + \frac{1}{2} \cdot \left(1 + G_{2IV} - G_{3IV}\right)\right)\right)^2 + \frac{\left(\overline{i_{C_{r_1}}(t)}\right)^2}{\left(\frac{\omega_2}{\omega_0}\right)^2} = \\ &= \left(\frac{1}{2}\right)^2 \cdot \left(1 + G_{2IV} - G_{3IV}\right)^2 \end{aligned} \tag{3.97}$$

Figure 35 – Resultant Characteristics based on the Operating Region IV within Interval III:
(a) Equivalent Circuit.
(b) C_{r_1} Geometrical Representation normalized by Z_{r_2} reference frame.
(c) C_{r_1} Geometrical Representation normalized by Z_r reference frame.
(d) C_{r_2} Geometrical Representation normalized by Z_{r_2} reference frame.
(e) C_{r_2} Geometrical Representation normalized by Z_r reference frame.



$$\left(\overline{v_{C_{r_2}}(t)} - \left(G_{3IV} - \frac{1}{2} \cdot \left(1 + G_{2IV} - G_{3IV}\right)\right)\right)^2 + \frac{\left(\overline{i_{C_{r_2}}(t)}\right)^2}{\left(\frac{\omega_2}{\omega_0}\right)^2} = \tag{3.98}$$

$$= \left(\frac{1}{2}\right)^2 \cdot \left(1 + G_{2IV} - G_{3IV}\right)^2$$

By interpreting the state-plane trajectory, in Figure 35b and 35d, due to the Input Voltage excitation V_{IN} and $\mp V_{C0_{\langle C_{r_n} \rangle}}$, the total charge transfer from C_{r_1} to C_{r_2} remains one normalized unit. Thus, it is maximum total voltage ripple $MAX[\overline{\Delta V_{C_{r_n}}} = \pm 2]$ at the end of the states' trajectories. As a consequence, the boundary conditions for the full sinusoidal waveform is identified, being tied to the operating switching frequency as V_{1V} and V_{4IV} have introduced enough headroom for the full resonance. Thus, the boundary relies on the Transition State (31). As the goal is to operate the converter in DCM, the later is not addressed in the 4L-RFLCC analysis. Therefore, by assuming the current discontinuity, it shifts to an additional passive topological stage, initiating

the Interval IV.

3.5.4 Interval IV ($t_3 < t < t_4$)

The Interval IV is initiated by the current discontinuity, in which the Passive Switches S_5 reverse bias, resulting in an idle state. The Interval IV lasts until the Transition State (31) is triggered. Due to the higher resonant frequency ω_2, within Interval III, and the maximum operating switching frequency $f_{sw.MAX}$, the condition $\frac{\omega_2}{2\pi} \leq \frac{2}{3} \cdot f_{sw}$ is always met.

3.5.5 Interval V ($t_4 < t < t_5$)

When the Active Switch S_1 turns-OFF, while S_3 remains ON, and the Active Switch S_2 turns-ON, the converter operates with the equivalent circuit shown in Figure 36a. The Interval V consists of a $L_r C_{r_2}$ resonant tank, analog to the description shown in the Section 2.1 and identical to Interval VI within Region III. As a result, the resonant tank is excited by $V_{IN} - V_{OUT}$, deriving a resonance activity under ω_0 trajectory velocity. The resonance creates a sinusoidal shaped state variables $v_{C_{r_2}}$ and $i_{C_{r_2}}$, as described in Equations (2.12) and (2.13), respectively, in which the parameters are as described below.

$$V_{DM} = V_1 - V_2 = V_{IN} - V_{OUT} \tag{3.99}$$

$$V_{C0} = V_{4IV} \tag{3.100}$$

$$I_{C0} = 0 \tag{3.101}$$

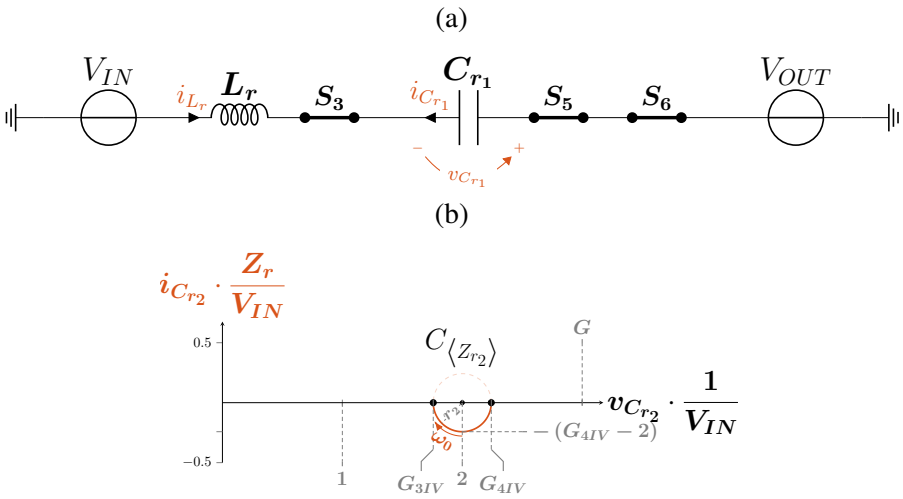
As a result, the resultant Z_r-normalized state variables are described in (3.102) and (3.103) while the state-plane trajectory, in the local resonant tank Z_r reference frame, is described as shown in (3.104) and Figure 36b.

$$\overline{v_{C_{r_2}}(t)} = G - 1 - (G - 1 - G_{4IV}) \cdot \cos(\omega_0 t) \tag{3.102}$$

$$\overline{i_{C_{r_2}}(t)} = -\overline{i_{L_r}(t)} = -(G - 1 - G_{4IV}) \cdot \sin(\omega_0 t) \tag{3.103}$$

$$\left(\overline{v_{C_{r_2}}(t)} - (G-1)\right)^2 + \left(\overline{i_{C_{r_2}}(t)}\right)^2 = G_{4IV} - G + 1 \tag{3.104}$$

Figure 36 – Resultant Characteristics based on the Operating Region IV within Interval V:
(a) Equivalent Circuit.
(b) Geometrical Representation normalized by Z_r reference frame.



By interpreting the state-plane trajectory, in Figure 36b, the state variable $v_{C_{r_2}}$ exhibits a reduced total charge transferred thanks to the decoupling in between C_{r_2} and the Output, which corresponds to the variable G outgrowing G_{4III} as G_{4III} has a descending characteristic. As a result, the boundary condition for the full sinusoidal waveform is identified and relies on the Transition State 11. As the goal is to operate the converter in DCM, the later is not addressed in the 4L-RFLCC analysis. Therefore, by assuming the current discontinuity, it shifts to an additional passive topological stage, initiating the Interval VI.

3.5.6 Interval VI ($t_5 < t < t_6$)

The Interval VI is initiated by the current discontinuity, in which the Passive Switch S_6 reverse biases, resulting in an idle state. The Interval VI lasts until the Transition State 11 is triggered and a new cycle initiates.

3.5.7 Summary of Operation

The Table 6 summarizes the different topological stages, and their main characteristics, which are illustrated in the Z_r State-Plane Trajectories in Figure 37 and in the time-domain state variables, shown in Figure 38. Shifting from Region III to Region IV has demonstrated to completely eliminate the voltage coupling amongst C_{r_n} and the Output. Thus, simplifying the assessment and operation of the converter. Additionally, due to the decoupling, every resonance is capable of coursing without interruption. As a consequence, the voltage conversion ratio becomes constant within Region IV and the 4L-RFLCC no longer is capable of stepping-up $V_{OUT} > 3$. Also, due to the full resonances, based on the State-plane Trajectories, C_{r_n}'s mean values have become clear, tending to the same mean value as expected in a non-resonant 4L-FLCC.

Table 6 – Summary of the different topological stages and their characteristics for the 4LRFLC topology under Region IV condition.

Topological Stage	**Switches State**			**L_r and C_r State**			**Operating Mode**
	S_1	S_2	S_3	L_r	C_{r1}	C_{r2}	
1st	ON	ON	OFF	$\nearrow$	$\nearrow$	$\rightarrow$	*Resonant* (ω_0)
2nd	ON	ON	OFF	$\rightarrow$	$\rightarrow$	$\rightarrow$	*Idle*
3rd	ON	OFF	ON	$\nearrow$	$\searrow$	$\nearrow$	*Resonant* (ω_2)
4th	ON	OFF	ON	$\rightarrow$	$\rightarrow$	$\rightarrow$	*Idle*
5th	OFF	ON	ON	$\nearrow$	$\rightarrow$	$\searrow$	*Resonant* (ω_0)
6th	OFF	ON	ON	$\rightarrow$	$\rightarrow$	$\rightarrow$	*Idle*

Figure 37 – Normalized State-Plane Trajectory under Operating Region IV for:
(a) C_{r_1}
(b) C_{r_2}

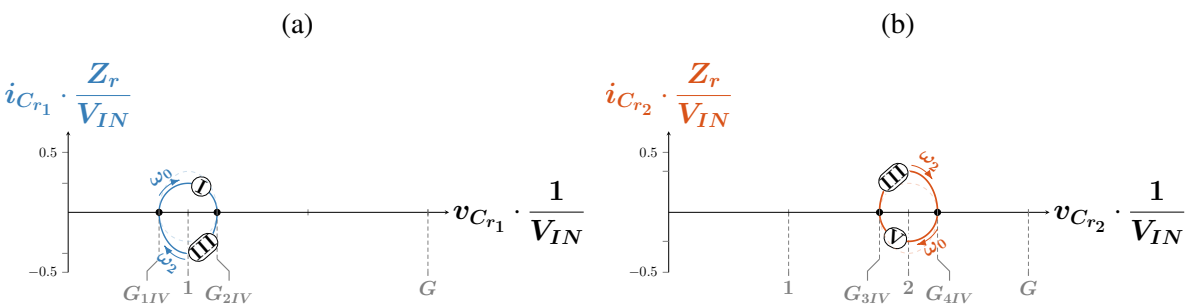
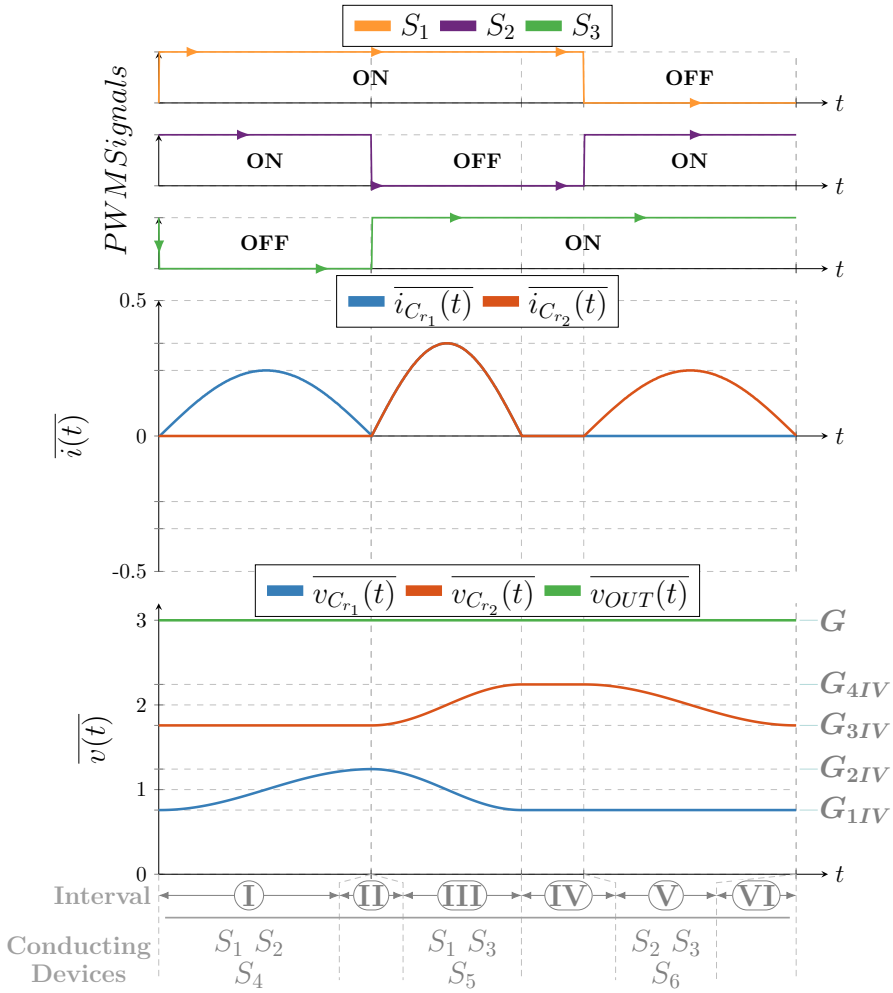


Figure 38 – Normalized Time-Domain State Variables for Operating Region IV.



4 STATIC GAIN & LARGE-SIGNAL ANALYSIS

The Static Gain and Large-Signal Analysis are determined based on the analytical and geometrical representations, presented in Section 3, where the initial and final conditions of the state variables are considered to aid in the process.

As per the energy conservation, Equation (4.1) is valid throughout the entire process by assuming 100% efficiency.

$$\begin{aligned} P_{OUT} &= P_{IN} \\ V_{OUT} \cdot I_{OUT} &= V_{IN} \cdot I_{IN} \end{aligned} \tag{4.1}$$

Additionally, V_{OUT} is defined as per Equation (4.2)

$$V_{OUT} = R_{OUT} \cdot I_{OUT} \tag{4.2}$$

By normalizing (4.2), Equation (4.3) is derived.

$$G = r_o \cdot \overline{I_{OUT}} \tag{4.3}$$

where r_o is defined as the normalized output load impedance, as shown in (4.4)

$$r_o = \frac{R_{OUT}}{Z_r} \tag{4.4}$$

Solving for the unknown parameter $\overline{I_{OUT}}$, it can be derived based on the Passive Switch S_6's current, as described in (4.5).

$$\overline{I_{OUT}} = f_{sw} \cdot \int_{t_i}^{t_f} \overline{I_{S_6}(t)}\, dt \tag{4.5}$$

Based on every interval time duration, the energy conservation theorem and/or the volt-second balance, for the resonant inductor, and the charge-balance for the resonant capacitors, are applied to find the relationship amongst the unknown variables. Thus, Equations (2.2) and (2.3) are the bases for the solution.

4.0.1 Region I

Based on the Geometrical Representations, and the definition of the initial and final conditions for $\overline{v_{c_{r_n}}}$ and $\overline{i_{c_{r_n}}}$, the phase-timings are defined as shown in Table 7.

The Passive Switch S_6's current is expressed in the equation (4.6), based on the expressions described in the Section 3.2, and shown in Figure 39.

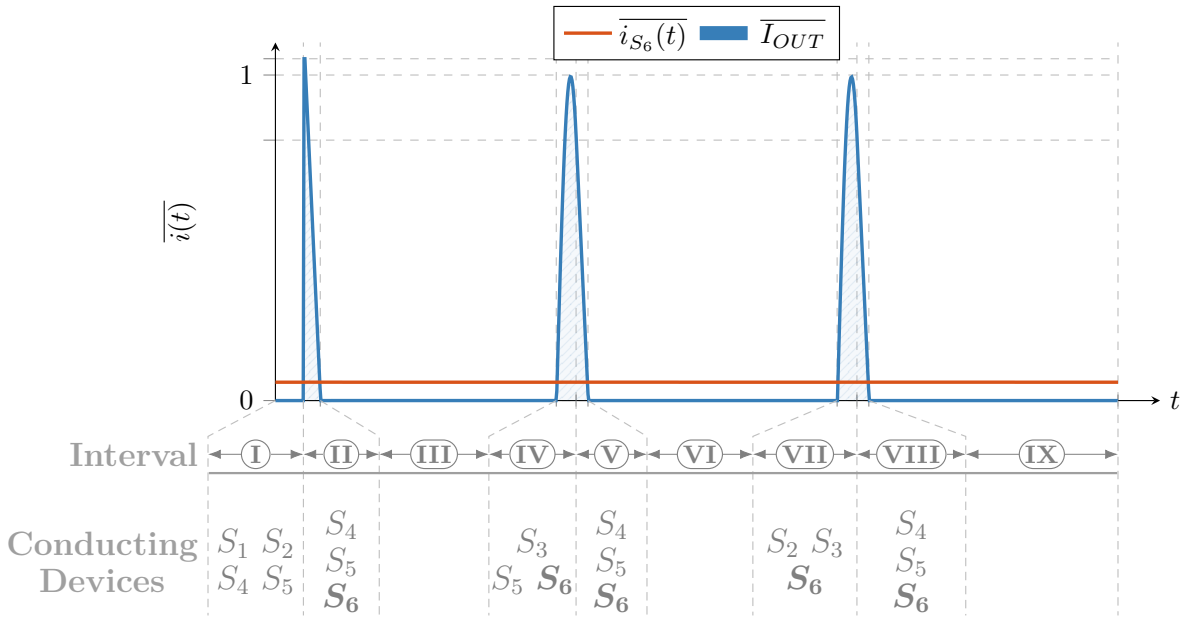
Table 7 – Table of Initial and Final Conditions for State Variables within Region I for Phase-Timing Definition.

Time Interval	**State Variables**					**Phase Timing**
	$\overline{i_{L_r}(t)}$	$\overline{v_{C_{r_1}}(t)}$	$\overline{i_{C_{r_1}}(t)}$	$\overline{v_{C_{r_2}}(t)}$	$\overline{i_{C_{r_2}}(t)}$	
t_0	0	0	0	0	0	
t_1	$\overline{I_{2I}}$	G	$\overline{I_{2I}}/2$	G	$\overline{I_{2I}}/2$	$\pi - acos(G-1)/\omega_1$
t_2	0	G	0	G	0	$\overline{I_{2I}}/G-1$
t_3	0	G	0	G	0	$\frac{1}{3}\cdot\frac{1}{f_{sw}} - \Delta T_{21I} - \Delta T_{10I}$
t_4	$\overline{I_{3I}}$	0	$-\overline{I_{3I}}$	G	0	$\pi - acos(G-1)/\omega_0$
t_5	0	0	0	G	0	$\overline{I_{3I}}/G-1$
t_6	0	0	0	G	0	$\frac{1}{3}\cdot\frac{1}{f_{sw}} - \Delta T_{54I} - \Delta T_{43I}$
t_7	$\overline{I_{5I}}$	0	0	0	$-\overline{I_{5I}}$	$\pi - acos(G-1)/\omega_0$
t_8	0	0	0	0	0	$\overline{I_{3I}}/G-1$
t_9	0	0	0	0	0	$\frac{1}{3}\cdot\frac{1}{f_{sw}} - \Delta T_{87I} - \Delta T_{76I}$

$$\overline{I_{S_6}(t)} = \begin{cases} 0, & t_0 < t < t_1 \\ (1-G)\cdot\omega_o\cdot(t-t_1)+\overline{I_{1I}}, & t_1 < t < t_2 \\ 0, & t_2 < t < t_3 \\ \sin(\omega_o\cdot t), & t_3 < t < t_4 \\ (1-G)\cdot\omega_o\cdot(t-t_4)+\overline{I_{2I}}, & t_4 < t < t_5 \\ 0, & t_5 < t < t_6 \\ \sin(\omega_o\cdot t), & t_6 < t < t_7 \\ (1-G)\cdot\omega_o\cdot(t-t_7)+\overline{I_{2I}}, & t_7 < t < t_8 \\ 0, & t_8 < t < t_9 \end{cases} \tag{4.6}$$

Based on (4.6), an expression for the normalized output current can be derived, as shown in (4.7).

Figure 39 – Area representation of Switch S_6 Current waveform within the topological stages under Region I condition.



$$\begin{aligned}\overline{I_{OUT}} = f_{sw} \cdot \int_{t_1}^{t_2} \overline{I_{S_6}(t)}\, dt + f_{sw} \cdot \int_{t_3}^{t_4} \overline{I_{S_6}(t)}\, dt + \\ + f_{sw} \cdot \int_{t_4}^{t_5} \overline{I_{S_6}(t)}\, dt + f_{sw} \cdot \int_{t_6}^{t_7} \overline{I_{S_6}(t)}\, dt + \\ + f_{sw} \cdot \int_{t_7}^{t_8} \overline{I_{S_6}(t)}\, dt\end{aligned} \tag{4.7}$$

By solving (4.7), Equation (4.8) is determined.

$$\overline{I_{OUT}} = 2 \cdot \frac{f_{sw}}{\omega_o} \cdot \frac{G}{G-1} \tag{4.8}$$

In order to simplify (4.8), the coefficient μ_o is defined as the ratio in between the switching frequency and the resonant frequency, as shown in (4.9).

$$\mu_o = \frac{2\pi \cdot f_{sw}}{\omega_0} \tag{4.9}$$

Thus,

$$\overline{I_{OUT}} = 2 \cdot \frac{\mu_o}{2\pi} \cdot \frac{G}{G-1} \tag{4.10}$$

By applying (4.3) and (4.4) into (4.10), the static voltage conversion ratio is derived, as a function of only the 4L-RFLCC operating conditions.

$$G = 2 \cdot \frac{r_o \cdot \mu_o}{2 \cdot \pi} + 1 \tag{4.11}$$

Based on (4.11) the coefficient Λ, as shown in (4.12), is defined as a reference for the resonant operating condition of the proposed converter.

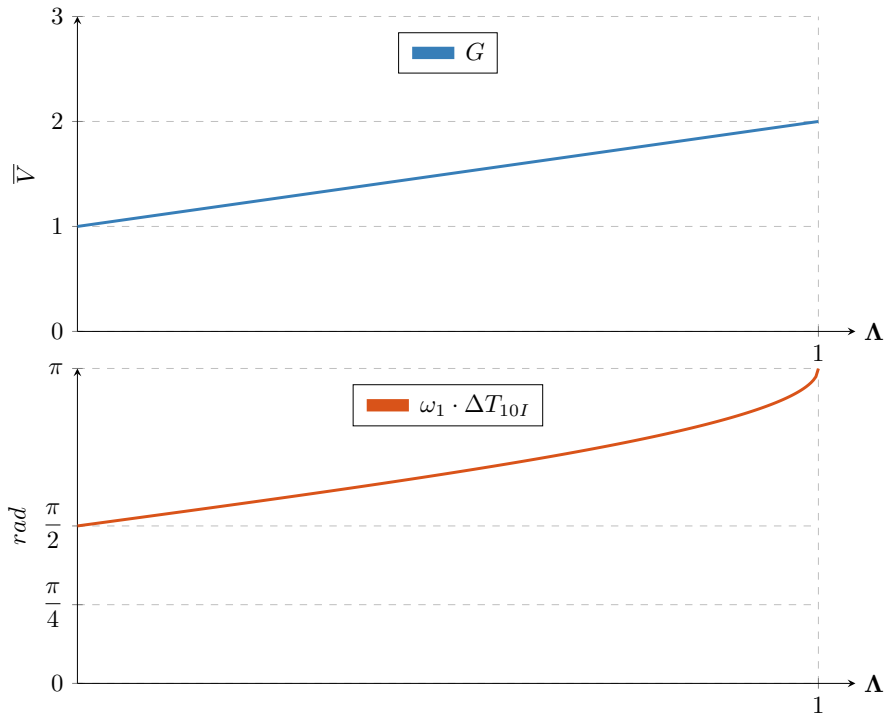
$$\Lambda = \frac{r_o \cdot \mu_o}{\pi} \tag{4.12}$$

Thus,

$$G = \Lambda + 1 \tag{4.13}$$

Based on (4.13) and Table 7, the phase-timings can be derived in order to prove the Region I's boundary conditions, as shown in Figure 40.

Figure 40 – Output Static Gain and Phase-Timing Characteristics as a function of Λ within Region I.



The Output characteristic, derived for the Region I, is particularly similar to the 3L-RFLCC Output characteristic, as shown in Equation (4.13). The increase of FLCCC is emphasized in the multiplier factor in the linear coefficient of Equation (4.13). The Table 8 represents the comparison between 3L-RFLCC and 4L-RFLCC's output characteristics.

Given the FLCCC characteristic, which imposes a differential voltage across the devices, depending on the Switching State, as per Table 2, the maximum peak voltage stresses exhibits

Table 8 – Comparison between 3L-RFLCC and 4L-RFLCC under Region I of Operating condition.

Topology	$G(\Lambda)$	$\overline{\mathbf{I_{L_{r_{MAX}}}}}$		$\overline{\mathbf{V_{S_{x_{MAX}}}}}$	**Nr of Intervals IO's Power Transfer**
		$\omega_x \cdot \Delta T \leq \frac{\pi}{2}$	$\omega_x \cdot \Delta T > \frac{\pi}{2}$		
3L-RFLCC	$\Lambda+1$	$\sqrt{1-(1-G)^2}$	1	G	3 $(out\ of\ 6)$
4L-RFLCC	$2\cdot\Lambda+1$	$\frac{\omega_o}{\omega_1}\cdot\sqrt{1-(1-G)^2}$	$\frac{\omega_o}{\omega_1}$	G	5 $(out\ of\ 9)$

a dependency with $v_{C_{r_n}}$ whereas the peak current stresses have a direct relationship with the State-plane Trajectory parameter and equivalent circuits, defined in Section 3.2. Thus, Table 9 introduces the maximum peak voltage and current stresses within Region I, where the indexes correspond to the topological stage.

Table 9 – Summary of the distribution of maximum peak voltage and current stresses in the Switches S_1 - S_6 under Region I condition.

	Switches S_1 - S_6					
	S_1	S_2	S_3	S_4	S_5	S_6
V_{MAX}	$G^{(7)(8)}$	$G^{(4)(5)}$	$G^{(1)(2)}$	$G^{(4)}$	$G^{(7)}$	$G^{(1)}$
I_{MAX}	$2\cdot\frac{\omega_1}{\omega_o}^{(1)}$	$1^{(7)}$	$1^{(4)(7)}$	$2\cdot\frac{\omega_1}{\omega_o}^{(1)}$	$1^{(4)}$	$1^{(4)(7)}$

4.0.2 Region II

Based on the Geometrical Representations, and the definition of the initial and final conditions for $\overline{v_{c_{r_n}}}$ and $\overline{i_{c_{r_n}}}$, the phase-timings are defined as shown in Table 10.

The Passive Switch S_6's current is expressed in the equation (4.14), based on the expressions described in the Section 3.3, and shown in Figure 41.

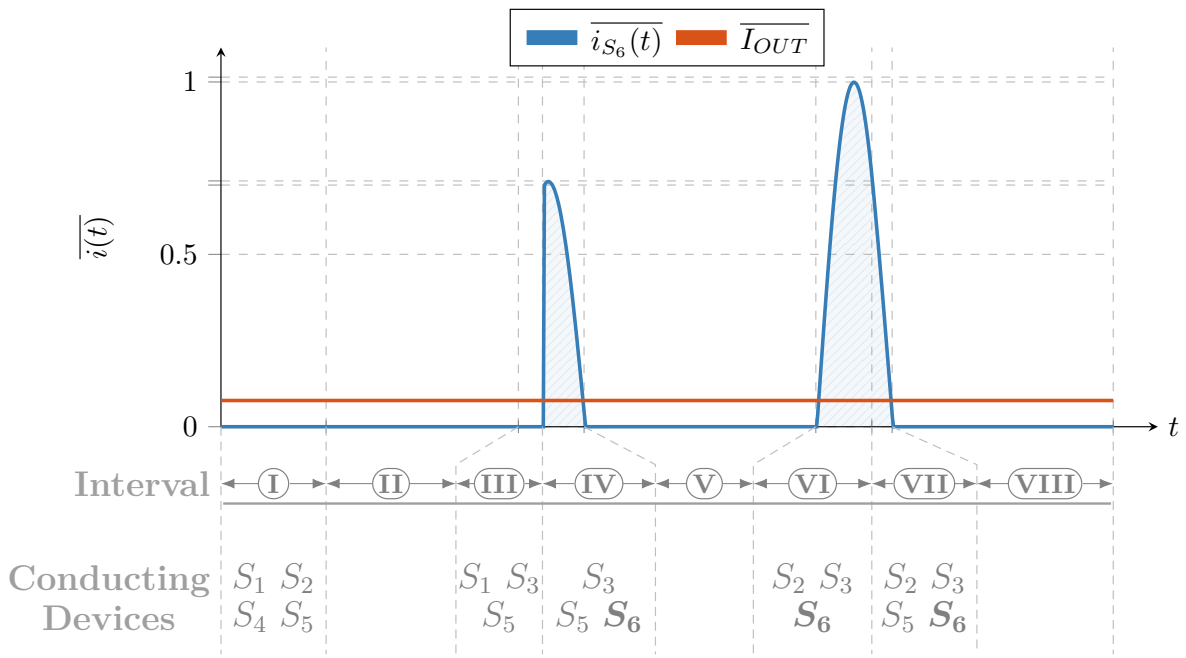
$$\overline{I_{S_6}(t)} = \begin{cases} 0, & t_0 < t < t_3 \\ \left(1-G+G_{i32II}\right)\cdot\sin\left(\omega_o\cdot t\right)+\overline{I_{2II}}\cdot\cos\left(\omega_o\cdot t\right), & t_3 < t < t_4 \\ 0, & t_4 < t < t_5 \\ \sin\left(\omega_o\cdot t\right), & t_5 < t < t_6 \\ \sqrt{2}\cdot\left(1-G+G_{2II}\right)\cdot\sin\left(\omega_1\cdot t\right)+\overline{I_{3II}}\cdot\cos\left(\omega_1\cdot t\right), & t_6 < t < t_7 \\ 0, & t_7 < t < t_8 \end{cases} \tag{4.14}$$

Based on (4.14), an expression for the normalized output current can be derived, as shown in (4.15).

Table 10 – Table of Initial and Final Conditions for State Variables within Region II for Phase-Timing Definition.

Time Interval	State Variables					Phase Timing
	$\overline{i_{L_r}(t)}$	$\overline{v_{C_{r_1}}(t)}$	$\overline{i_{C_{r_1}}(t)}$	$\overline{v_{C_{r_2}}(t)}$	$\overline{i_{C_{r_2}}(t)}$	
t_0	0	G_{1II}	0	G_{1II}	0	
t_1	0	G_{3II}	0	G_{3II}	0	$\frac{\pi}{\omega_1}$
t_2	0	G_{3II}	0	G_{3II}	0	$\frac{1}{3}\cdot\frac{1}{f_{sw}}-\frac{\pi}{\omega_1}$
t_3	$\overline{I_{2II}}$	G_{i32II}	$-\overline{I_{2II}}$	G	$\overline{I_{2II}}$	$\frac{1}{\omega_2}\cdot\left(\pi-\arccos\left(2\cdot(G-G_{3II})-1\right)\right)$
t_4	0	G_{2II}	0	G	0	$-\frac{1}{\omega_0}\cdot\arctan\left(\frac{\overline{I_{2II}}}{1-G+G_{i32II}}\right)$
t_5	0	G_{2II}	0	G	0	$\frac{1}{3}\cdot\frac{1}{f_{sw}}-\Delta T_{43II}-\Delta T_{32II}$
t_6	$\overline{I_{3II}}$	G_{2II}	0	G_{2II}	$-\overline{I_{3II}}$	$-\frac{1}{\omega_0}\cdot\arccos\left(1-G+G_{2II}\right)$
t_7	0	G_{1II}	0	G_{1II}	0	$\frac{1}{\omega_1}\cdot\arccos\left(\frac{\frac{\omega_1}{\omega_0}\cdot\overline{I_{3II}}}{G-1-G_{2II}}\right)$
t_8	0	G_{1II}	0	G_{1II}	0	$\frac{1}{3}\cdot\frac{1}{f_{sw}}-\Delta T_{76II}-\Delta T_{65II}$

Figure 41 – Area representation of Switch S_6 Current waveform within the topological stages under Region II condition.



$$\overline{I_{OUT}} = f_{sw}\cdot\int_{t_3}^{t_4}\overline{I_{S_6}(t)}\,dt + f_{sw}\cdot\int_{t_5}^{t_6}\overline{I_{S_6}(t)}\,dt + f_{sw}\cdot\int_{t_6}^{t_7}\overline{I_{S_6}(t)}\,dt = \tag{4.15}$$

By solving (4.15), Equation (4.16) is derived, which exhibits a dependency to G_{1II}.

$$G = 4 \cdot \frac{r_o \cdot \mu_o}{2 \cdot \pi} \cdot (1 - G_{1II}) \tag{4.16}$$

Therefore, by introducing the energy conservation, as presented in (4.1), $\overline{I_{IN}}$ is derived, as shown in (4.17).

$$\overline{I_{IN}} = \frac{\mu_o}{2 \cdot \pi} \cdot \left[6 + G - 7 \cdot G_{1II}\right] \tag{4.17}$$

By applying (4.17) and the voltage relationship given the State-plane trajectory, the static voltage conversion ratio is derived, as a function of only the 4L-RFLCC operating conditions.

$$G = \frac{1}{8} \cdot \left[7 + 2 \cdot \Lambda + \sqrt{(7 + 2 \cdot \Lambda)^2 - 32 \cdot \Lambda}\right] \tag{4.18}$$

Based on (4.17), the remaining large-signal characteristic can be found.

$$G_{12II} = \frac{1}{8} \cdot \left[7 - \frac{1}{2 \cdot \Lambda} \cdot \left(7 + \sqrt{(7 + 2 \cdot \Lambda)^2 - 32 \cdot \Lambda}\right)\right] \tag{4.19}$$

$$G_{32II} = \frac{1}{8} \cdot \left[9 + \frac{1}{2 \cdot \Lambda} \cdot \left(7 + \sqrt{(7 + 2 \cdot \Lambda)^2 - 32 \cdot \Lambda}\right)\right] \tag{4.20}$$

$$G_{i32II} = \frac{1}{8} \cdot \left[11 + \frac{7}{\Lambda} - 2 \cdot \Lambda + \left(\frac{1}{\Lambda} - 1\right) \cdot \sqrt{(7 + 2 \cdot \Lambda)^2 - 32 \cdot \Lambda}\right] \tag{4.21}$$

Based on (4.18) and 10, the phase-timings can be derived in order to prove the Region II's boundary conditions, as shown in Figure 42.

By interpreting the Phase-timing, shown in Figure 42, there exist a Λ dependency on the maximum peak current stress within Interval III and IV as the State-plane Trajectory crosses in between the $\frac{\pi}{2}$ point.

Based on the state-plane trajectory for Interval III and Interval IV, as shown in Section 3.3.3 and 3.3.4, respectively, the Figure 43 represents the associated state-plane peak point, as a function of Λ. Therefore, it is possible to notice that $\Lambda < -1 + \frac{3 \cdot \sqrt{3}}{3}$ translates into a higher peak current stress.

Based on that, the Figure 44 represents the peak current stresses amongst the three resonant semi-cycles, composed by the Interval I, Interval III and IV and Interval VI and VII. Hence, the derivation of the peak current stresses amongst the Switches $S_1 - S_6$, which are summarize in Table 11.

Figure 42 – Output Static Gain and Phase-Timing Characteristics as a function of Λ within Region II.

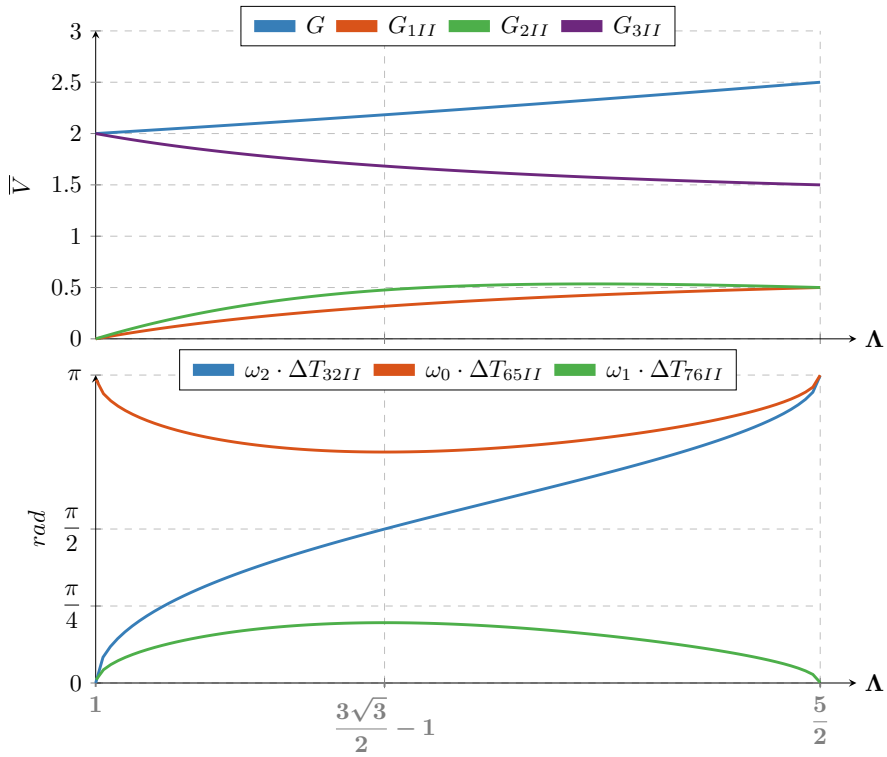
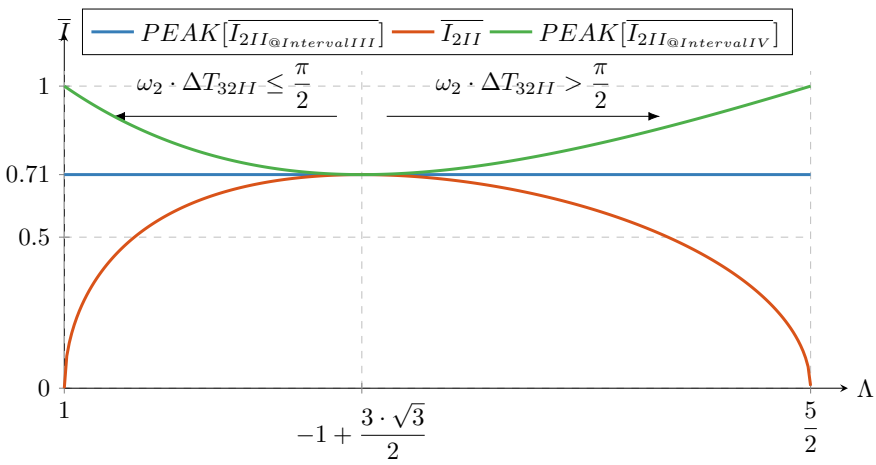


Figure 43 – Interval III and Interval IV Peak current stresses progression based on State-plane Trajectory.



4.0.3 Region III

Based on the Geometrical Representations, and the definition of the initial and final conditions for $\overline{v_{c_{rn}}}$ and $\overline{i_{c_{rn}}}$, the phase-timings are defined as shown in Table 12.

The Passive Switch S_6's current is expressed in the equation (4.22), based on the expressions described in the Section 3.4, and shown in Figure 45.

Figure 44 – Peak current stresses progression based on resonant semi-cycles under Region II condition.

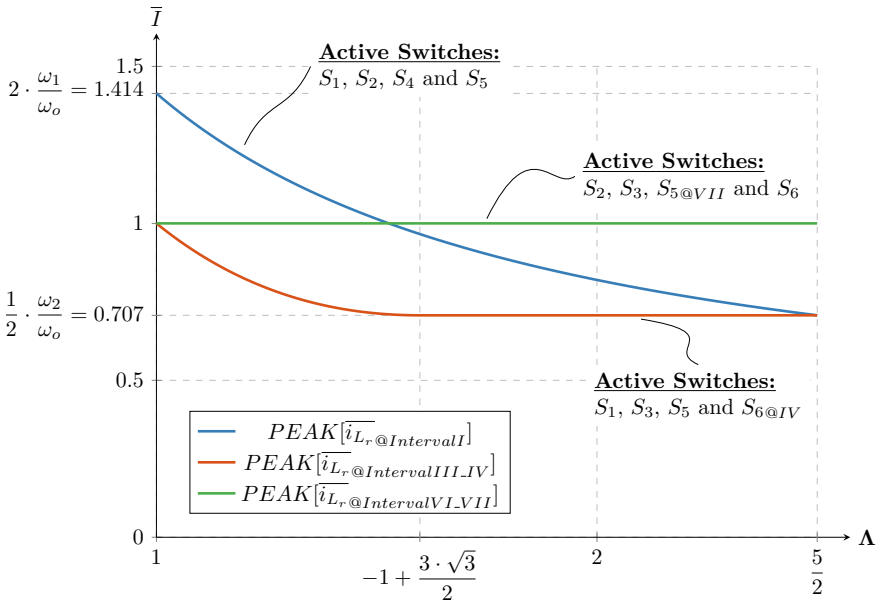


Table 11 – Summary of the distribution of maximum peak voltage and current stresses in the Switches S_1 - S_6 under Region II condition.

	Switches S_1 - S_6					
	S_1	S_2	S_3	S_4	S_5	S_6
V_{MAX}	$G - G_{1II}{}^{(7)}$	$G - G_{2II}{}^{(4)}$	$2 - G_{1II}{}^{(1)}$	$2 - G_{1II}{}^{(3)}$	$G - G_{2II}{}^{(6)}$	$G - G_{1II}{}^{(1)(1)}$
I_{MAX}	$\sqrt{2} \cdot (1 - G_{1II})^{(1)}$	$1^{(6)}$	$1^{(6)}$	$\sqrt{2} \cdot (1 - G_{1II})^{(2)}$	$b_{4II}{}^{(4)\text{ab}}$ / $\frac{\sqrt{2}}{2}{}^{(3)\text{c}}$	$1^{(6)}$

[a] b_{4II} is applicable only if $\Lambda < -1 + \frac{3 \cdot \sqrt{3}}{2}$

[b] $b_{4II} = \sqrt{\left(G - 1 - G_{i32II}\right)^2 + \left(\overline{I_{2II}}\right)^2}$

[c] $\frac{\sqrt{2}}{2}$ is applicable only if $\Lambda \geq -1 + \frac{3 \cdot \sqrt{3}}{2}$

$$\overline{I_{S_6}(t)} = \begin{cases} 0, & t_0 < t < t_5 \\ \left(G_4 + 1 - G\right) \cdot \sin\left(\omega_o \cdot t\right), & t_5 < t < t_6 \\ 0, & t_6 < t < t_7 \end{cases} \tag{4.22}$$

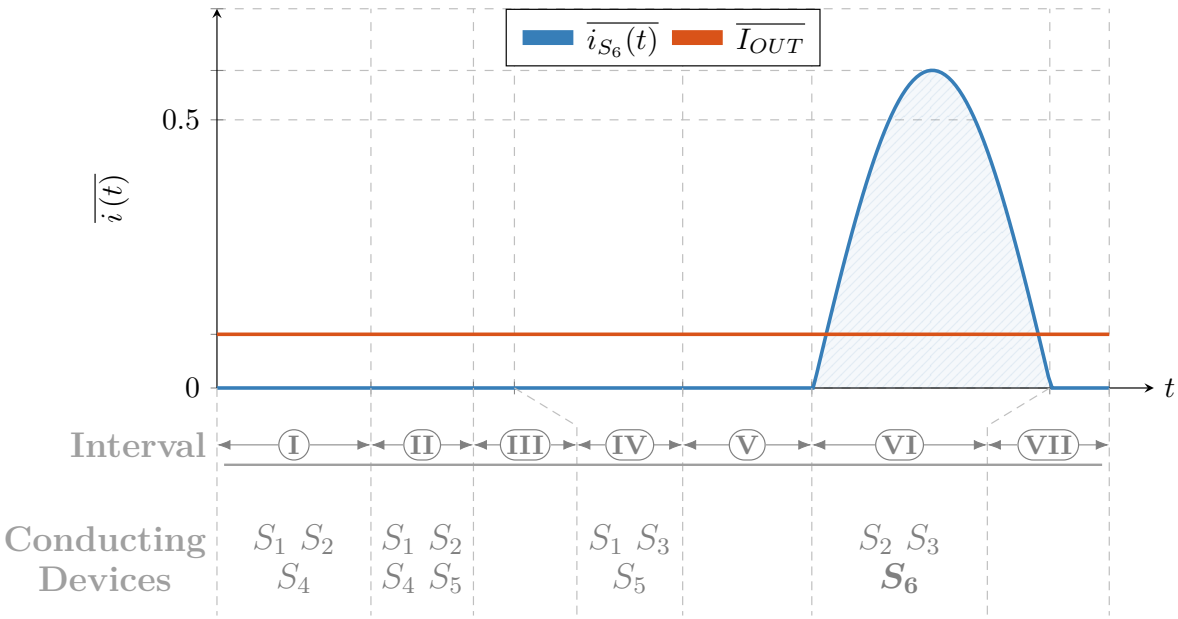
Based on (4.22), an expression for the normalized output current can be derived, as shown in (4.23).

$$\overline{I_{OUT}} = f_{sw} \cdot \int_{t_5}^{t_6} \overline{I_{S_6}(t)}\, dt \tag{4.23}$$

Table 12 – Table of Initial and Final Conditions for State Variables within Region III for Phase-Timing Definition.

Time Interval	State Variables					Phase Timing
	$\overline{i_{L_r}(t)}$	$\overline{v_{C_{r_1}}(t)}$	$\overline{i_{C_{r_1}}(t)}$	$\overline{v_{C_{r_2}}(t)}$	$\overline{i_{C_{r_2}}(t)}$	
t_0	0	G_{1III}	0	G_{2III}	0	
t_1	$\overline{I_{2III}}$	G_{2III}	$\frac{1}{2}\cdot\overline{I_{2III}}$	G_{2III}	$\frac{1}{2}\cdot\overline{I_{2III}}$	$\frac{1}{\omega_0}\cdot\arccos\left(\frac{1-G_{2III}}{1-G_{1III}}\right)$
t_2	0	G_{3III}	0	G_{3III}	0	$\frac{1}{\omega_1}\cdot\arctan\left(\frac{\omega_1}{\omega_0}\cdot\frac{\overline{I_{2III}}}{G_{2III}-1}\right)$
t_3	0	G_{3III}	0	G_{3III}	0	$\frac{1}{3}\cdot\frac{1}{f_{sw}}-\Delta T_{21III}-\Delta T_{10III}$
t_4	0	G_{1III}	0	G_{4III}	0	$\frac{\pi}{\omega_2}$
t_5	0	G_{1III}	0	G_{4III}	0	$\frac{1}{3}\cdot\frac{1}{f_{sw}}-\Delta T_{54III}-\Delta T_{43III}$
t_6	0	G_{1III}	0	G_{2III}	0	$\frac{\pi}{\omega_0}$
t_7	0	G_{1III}	0	G_{2III}	0	$\frac{1}{3}\cdot\frac{1}{f_{sw}}-\Delta T_{76III}-\Delta T_{65III}$

Figure 45 – Area representation of Switch S_6 Current waveform within the topological stages under Region III condition.



By manipulating (4.23), and applying (4.3), (4.24) is derived.

$$G=\frac{1}{1+\frac{1}{\Lambda}}\cdot\left(1+G_{4III}\right) \tag{4.24}$$

Similarly, as shown in Section 4.0.2, $\overline{I_{IN}}$ expression is found, as shown in (4.25), and

manipulated to derive the static voltage conversion ratio is derived, as a function of only the 4L-RFLCC operating conditions.

$$\begin{aligned}\overline{I_{IN}} &= \frac{1}{T_{sw}} \cdot \int_0^{T_{sw}} \overline{i_{L_r}(t)}\, dt = \\ &= \int_0^{\Delta T_{10}} \overline{i_{L_{r_{10}}}(t)}\, dt + 2 \cdot \int_0^{\Delta T_{21}} \frac{1}{2} \cdot \overline{i_{L_{r_{21}}}(t)}\, dt + \\ &+ \int_0^{\Delta T_{43}} \overline{i_{L_{r_{43}}}(t)}\, dt + \int_0^{\Delta T_{65}} \overline{i_{L_{r_{65}}}(t)}\, dt\end{aligned} \tag{4.25}$$

$$G = 1 + \sqrt{1 + \frac{1}{2} \cdot \Lambda} \tag{4.26}$$

As per (4.26), and the Phase-Timings, described in Table 12, the remaining large-signal characteristic can be found.

$$G_{1III} = \frac{1}{\Lambda} - 2 + \left(1 + \frac{1}{\Lambda}\right) \cdot \sqrt{1 + \frac{1}{2} \cdot \Lambda} \tag{4.27}$$

$$G_{3III} = \frac{1}{\Lambda} - 1 + \left(1 + \frac{1}{\Lambda}\right) \cdot \sqrt{1 + \frac{1}{2} \cdot \Lambda} \tag{4.28}$$

$$G_{4III} = \frac{1}{\Lambda} + \left(1 + \frac{1}{\Lambda}\right) \cdot \sqrt{1 + \frac{1}{2} \cdot \Lambda} \tag{4.29}$$

$$G_{2III} = -\frac{1}{\Lambda} + \left(1 - \frac{1}{\Lambda}\right) \cdot \sqrt{1 + \frac{1}{2} \cdot \Lambda} \tag{4.30}$$

Based on (4.26) and 12, the phase-timings can be derived in order to prove the Region II's boundary conditions, as shown in Figure 46

By interpreting the Phase-timing, shown in Figure 46, there exist a Λ dependency on the maximum peak current stress within Interval I and II as the State-plane Trajectory crosses in between the $\frac{\pi}{2}$ point.

Based on the state-plane trajectory for Interval I and Interval II, as shown in Section 3.4.1 and 3.4.2, respectively. Therefore, by solving for the crossing point $\frac{\pi}{2}$ it is possible to notice that $\Lambda < 1 + 2 \cdot \sqrt{2}$ translates into a higher peak current stress, as shown in Figure 47.

Thus, Table 13 introduces the maximum peak voltage and current stresses within Region III, where the indexes correspond to the topological stage.

Figure 46 – Output Static Gain and Phase-Timing Characteristics as a function of Λ within Region III.

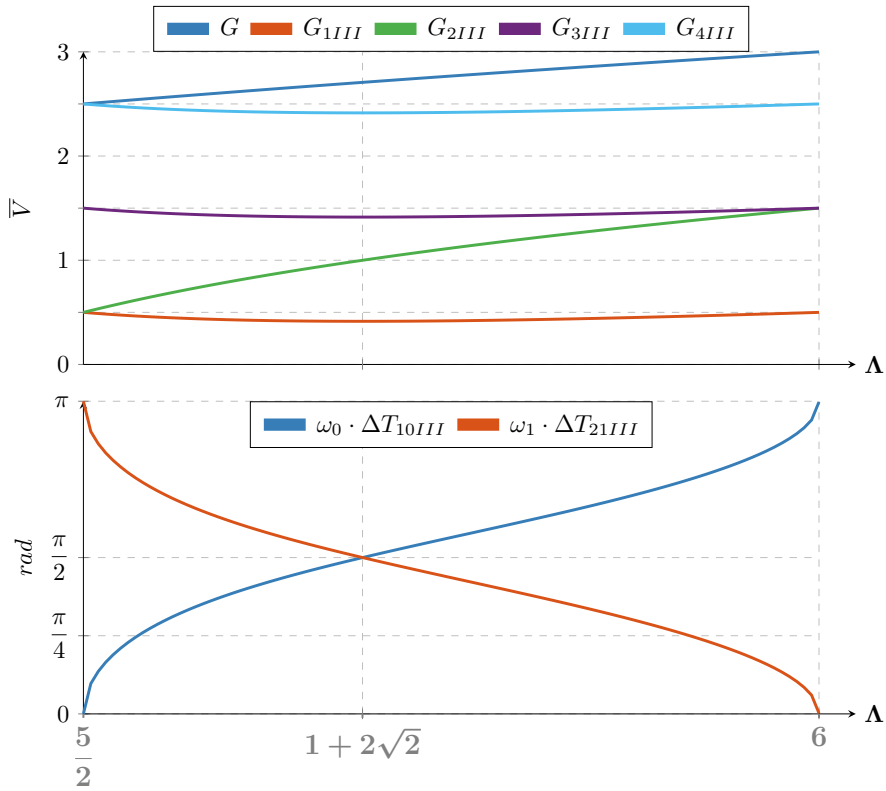
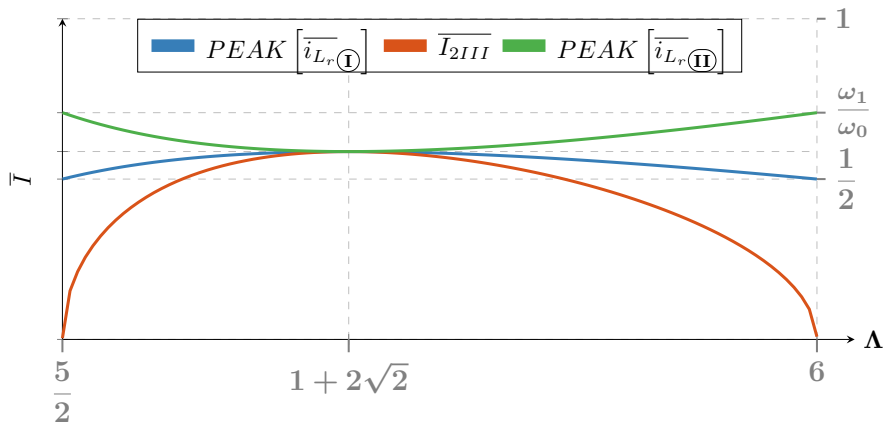


Figure 47 – Interval I and II Peak Current Stress Impact as a function of Λ within Region III.



4.0.4 Region IV

Based on the Geometrical Representations, and the definition of the initial and final conditions for $\overline{v_{c_{r_n}}}$ and $\overline{i_{c_{r_n}}}$, the phase-timings are defined as shown in Table 14.

The Passive Switch S_6's current is expressed in the equation (4.31), based on the expressions described in the Section 3.5, and shown in Figure 48.

Table 13 – Summary of the distribution of maximum peak voltage and current stresses in the Switches S_1 - S_6 under Region III condition.

	Switches S_1 - S_6					
	S_1	S_2	S_3	S_4	S_5	S_6
V_{MAX}	$G-G_2{}^{(6)}$	$2^{(4)}$	$G_3{}^{(2)}$	$G_3{}^{(4)}$	$2^{(6)}$	$G-G_2{}^{(1)(2)}$
I_{MAX}	$\frac{\sqrt{2}}{2}^{(4)}$	$G_4+1-G^{(6)}$	$G_4+1-G^{(6)\text{ab}}$	$2\cdot b_{2III}{}^{(2)\text{ab}}$	$\frac{\sqrt{2}}{2}^{(4)}$	$G_4+1-G^{(6)}$
			$\frac{\sqrt{2}}{2}^{(4)\text{ c}}$	$1-G_1{}^{(1)\text{c}}$		

[a] b_{2III} is applicable only if $\Lambda < 1+2\cdot\sqrt{2}$

[b] $b_{2III} = \frac{\omega_0}{\omega_1}\cdot\sqrt{\left(1-G_{2III}\right)^2+\left(\frac{1}{2}\cdot\frac{\omega_1}{\omega_0}\cdot\overline{I_{2III}}\right)^2}$

[c] is applicable only if $\Lambda \geq 1+2\cdot\sqrt{2}$

Table 14 – Table of Initial and Final Conditions for State Variables within Region IV for Phase-Timing Definition.

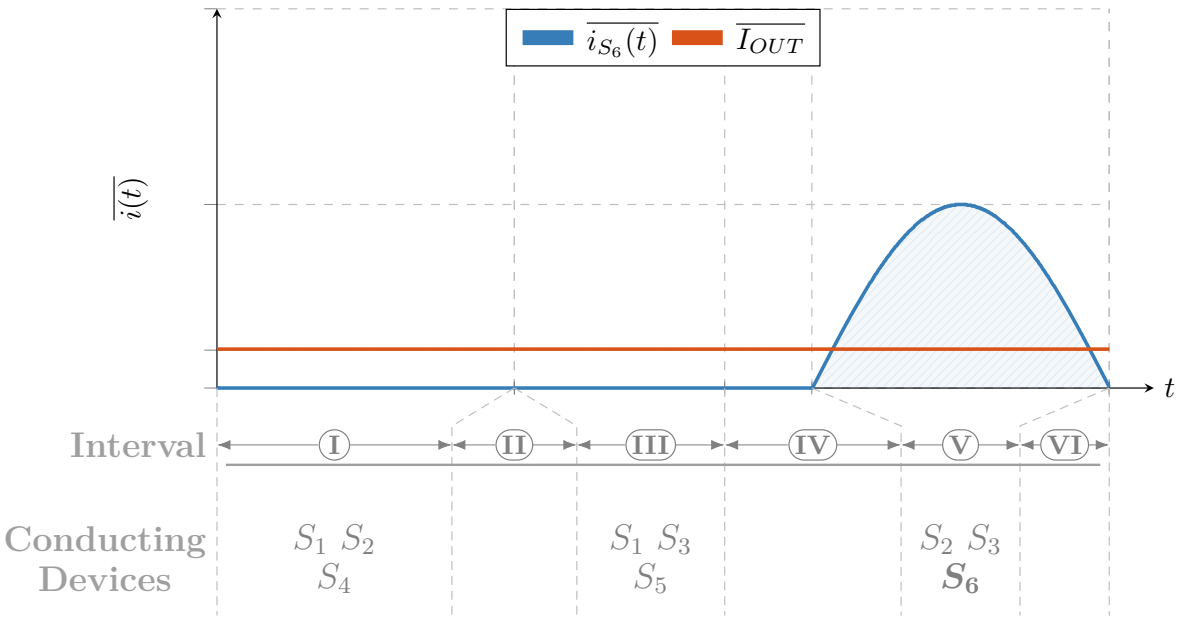
Time Interval	**State Variables**					**Phase Timing**
	$\overline{i_{L_r}(t)}$	$\overline{v_{C_{r_1}}(t)}$	$\overline{i_{C_{r_1}}(t)}$	$\overline{v_{C_{r_2}}(t)}$	$\overline{i_{C_{r_2}}(t)}$	
t_0	0	G_{1IV}	0	G_{2IV}	0	
t_1	0	G_{2IV}	0	G_{2IV}	0	$\frac{\pi}{\omega_0}$
t_2	0	G_{2IV}	0	G_{2IV}	0	$\frac{1}{3}\cdot\frac{1}{f_{sw}}-\Delta T_{10IV}$
t_3	0	G_{1IV}	0	G_{3IV}	0	$\frac{\pi}{\omega_2}$
t_4	0	G_{1IV}	0	G_{3IV}	0	$\frac{1}{3}\cdot\frac{1}{f_{sw}}-\Delta T_{32IV}$
t_5	0	G_{1IV}	0	G_{2IV}	0	$\frac{\pi}{\omega_0}$
t_6	0	G_{1IV}	0	G_{2IV}	0	$\frac{1}{3}\cdot\frac{1}{f_{sw}}-\Delta T_{54IV}$

$$\overline{I_{S_6}(t)} = \begin{cases} 0, & t_0 < t < t_4 \\ (G_{4IV}+1-G)\cdot\sin(\omega_o\cdot t), & t_4 < t < t_5 \\ 0, & t_5 < t < t_6 \end{cases} \tag{4.31}$$

Based on (4.31), an expression for the normalized output current can be derived, as shown in (4.32).

$$\overline{I_{OUT}} = f_{sw}\cdot\int_{t_4}^{t_5}\overline{I_{S_6}(t)}\,dt \tag{4.32}$$

Figure 48 – Area representation of Switch S_6 Current waveform within the topological stages under Region IV condition.



By solving (4.32), the final expression for the normalized output current $\overline{I_{OUT}}$ is derived, as shown in Equation (4.33).

$$\overline{I_{OUT}} = 2 \cdot \frac{\mu_o}{2 \cdot \pi} \cdot (G_{4IV} + 1 - G) \tag{4.33}$$

By manipulating (4.33), and applying (4.3), (4.34) is derived.

$$G = \frac{1}{1 + \frac{1}{\Lambda}} \cdot \left(1 + G_{4IV}\right) \tag{4.34}$$

Similarly, as shown in Section 4.0.3, $\overline{I_{IN}}$ expression is found, as shown in (4.35), and manipulated to derive the static voltage conversion ratio is derived, as a function of only the 4L-RFLCC operating conditions.

$$\begin{aligned} \overline{I_{IN}} &= \frac{1}{T_{sw}} \cdot \int_0^{T_{sw}} \overline{i_{L_r}(t)}\, dt = \\ &= \int_0^{\Delta T_{10IV}} \overline{i_{L_{r_{10}}}(t)}\, dt + \\ &+ \int_0^{\Delta T_{32IV}} \overline{i_{L_{r_{32}}}(t)}\, dt + \int_0^{\Delta T_{54IV}} \overline{i_{L_{r_{54}}}(t)}\, dt \end{aligned} \tag{4.35}$$

$$G = 3 \tag{4.36}$$

As per (4.36), and the Phase-Timings, described in Table 14, the remaining large-signal characteristic can be found.

$$G_{1IV} = 1 - \frac{3}{\Lambda} \tag{4.37}$$

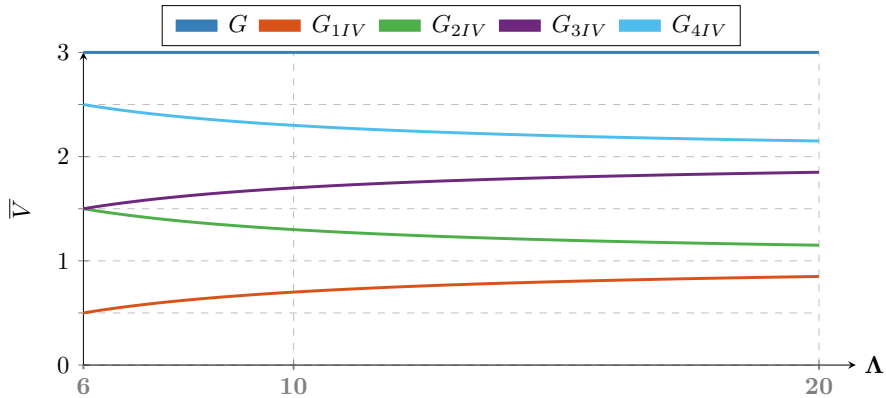
$$G_{2IV} = 1 + \frac{3}{\Lambda} \tag{4.38}$$

$$G_{3IV} = 2 - \frac{3}{\Lambda} \tag{4.39}$$

$$G_{4IV} = 2 + \frac{3}{\Lambda} \tag{4.40}$$

Finally, the later are shown in Figure 49 as a function of Λ.

Figure 49 – Output Static Gain Characteristics as a function of Λ within Region IV.



The derivation of the peak current stresses amongst the Switches $S_1 - S_6$, which are summarize in Table 15, can be extracted from the State-plane Trajectories, presented in Section 3.5.

4.0.5 Large-Signal Analysis Summary

The Table 16 summarizes the output voltage characteristic associated with the different operating conditions, from Region I to Region IV.

The Figure 52 represents the static behaviour of the proposed 4L-RFLCC across Region I to Region IV condition whereas Figures 50 and 51 represent the maximum normalized peak current stress per resonant cycle $MAX\left[\overline{I_{L_r}}_{\textcircled{X}}\right]$ and the maximum normalized peak current $MAX\left[\overline{I_{L_r}}\right]$.

Based on that, and the equivalent circuits across the different topological stages, Figures 53 and 54 represent the current and voltage stresses, respectively within Region I to Region IV.

Table 15 – Summary of the distribution of maximum peak voltage and current stresses in the Switches S_1 - S_6 under Region IV condition.

		V_{MAX}	I_{MAX}
Switches $S_1 - S_6$	S_1	$2 - G_{1IV}{}^{(5)}$	$\frac{\omega_2}{\omega_o} \cdot (1 - G_{1IV})^{(3)}$
	S_2	$3 - 2 \cdot G_{1IV}{}^{(3)}$	$1 - G_{1IV}{}^{(1)(5)}$
	S_3	$2 - G_{1IV}{}^{(1)}$	$\frac{\omega_2}{\omega_o} \cdot (1 - G_{1IV})^{(3)}$
	S_4	$2 - G_{1IV}{}^{(3)}$	$1 - G_{1IV}{}^{(1)}$
	S_5	$3 - 2 \cdot G_{1IV}{}^{(5)}$	$\frac{\omega_2}{\omega_o} \cdot (1 - G_{1IV})^{(3)}$
	S_6	$2 - G_{1IV}{}^{(1)(2)(3)(6)}$	$1 - G_{1IV}{}^{(5)}$

Table 16 – Summary of the Output Voltage Characteristic associated with Region I to Region IV condition.

	Output Voltage Characteristic		
	Operating Condition (Λ)	**G**	**Function Characteristic**
Region I	$[0,1]$	$\Lambda + 1$	Linear
Region II	$\left(1, \frac{5}{2}\right]$	$\frac{1}{8} \cdot \left[7 + 2 \cdot \Lambda + \sqrt{(7 + 2 \cdot \Lambda)^2 + - 32 \cdot \Lambda}\right]$	Quadratic
Region III	$\left(\frac{5}{2}, 6\right]$	$1 + \sqrt{1 + \frac{1}{2} \cdot \Lambda}$	Quadratic
Region IV	$(6, \infty)$	3	Constant

Figure 50 – Cycle-by-Cycle Maximum Normalized Peak Current Large-Signal Characteristic under Region I to IV condition.

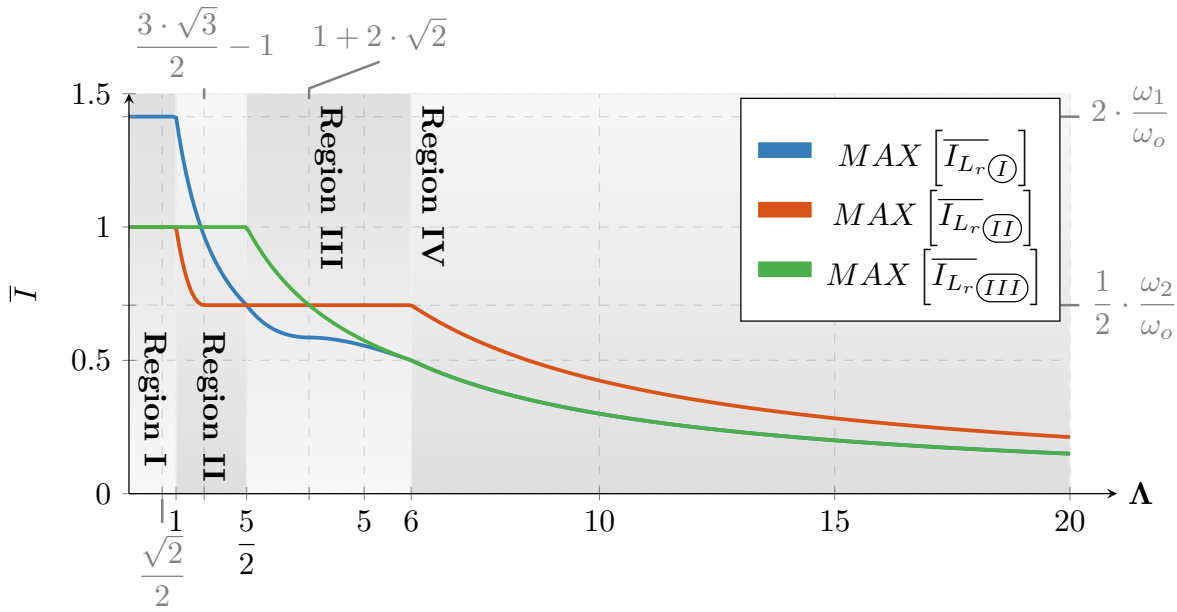


Figure 51 – Global Maximum Normalized Peak Current Large-Signal Characteristic under Region I to IV condition.

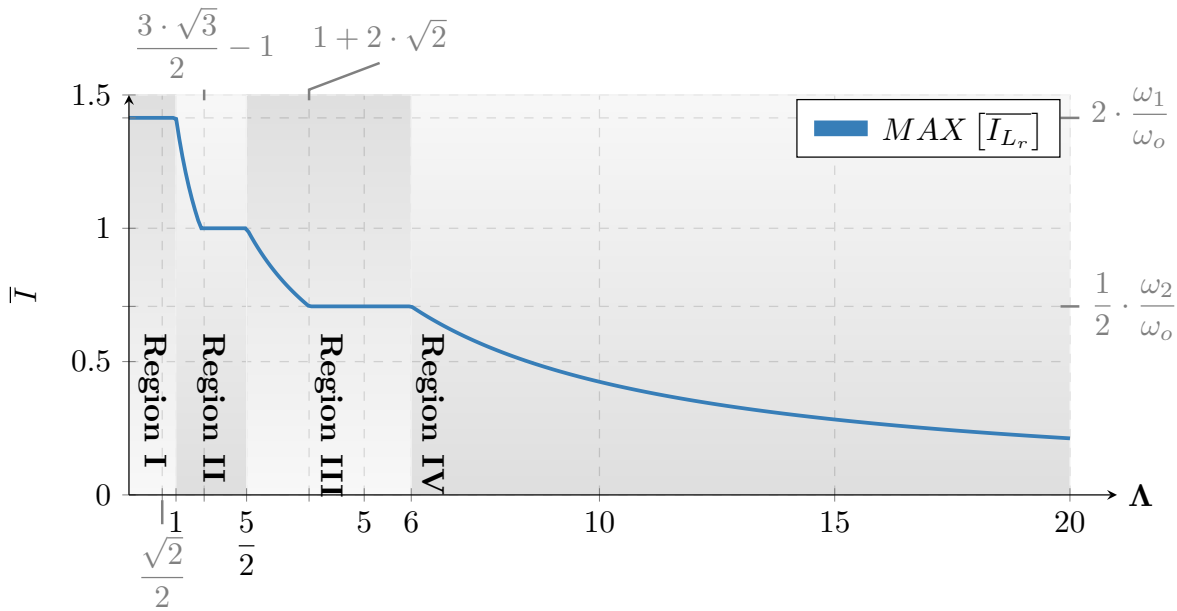


Figure 52 – 4L-RFLCC Static Output and Flying capacitors' Voltage Characteristic under Region I to IV condition.

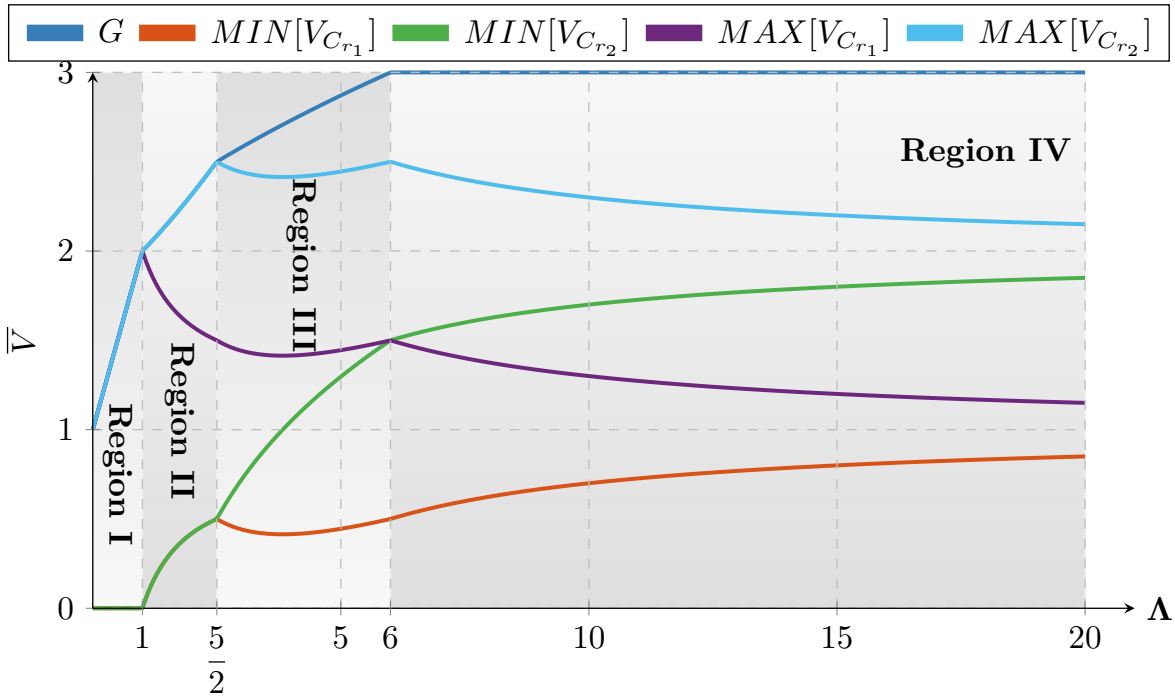


Figure 53 – 4L-RFLCC Switches $S_1 - S_6$ Maximum Current Stress Characteristic under Region I to IV condition.

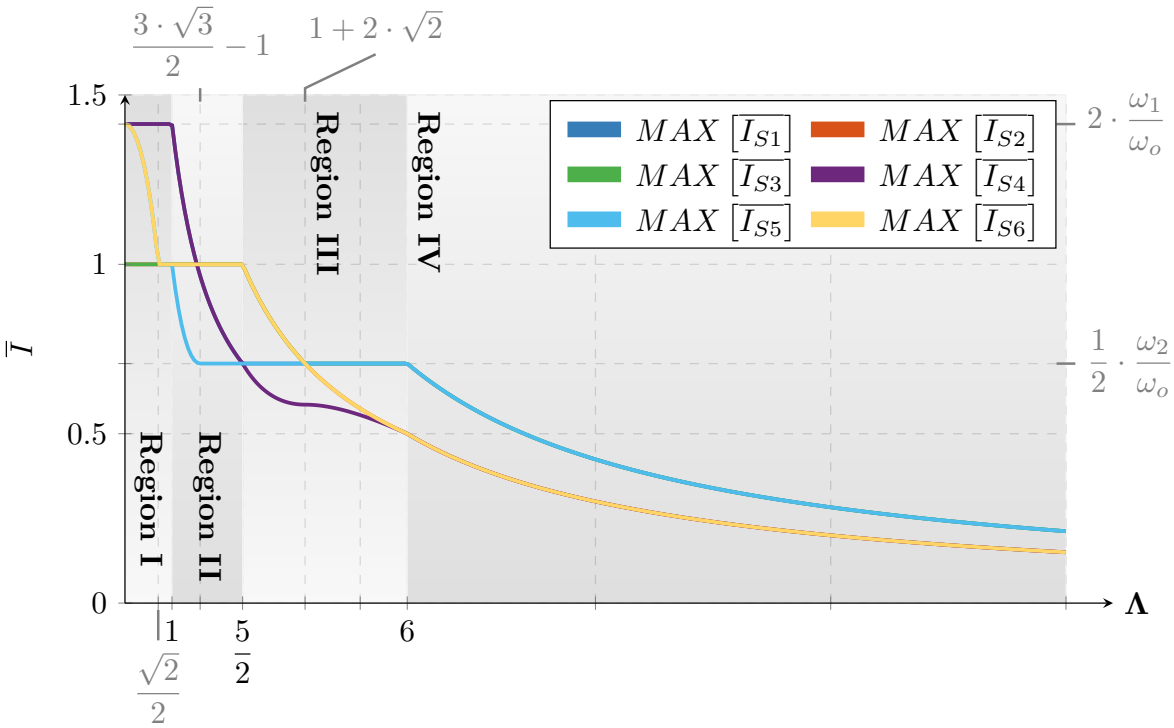
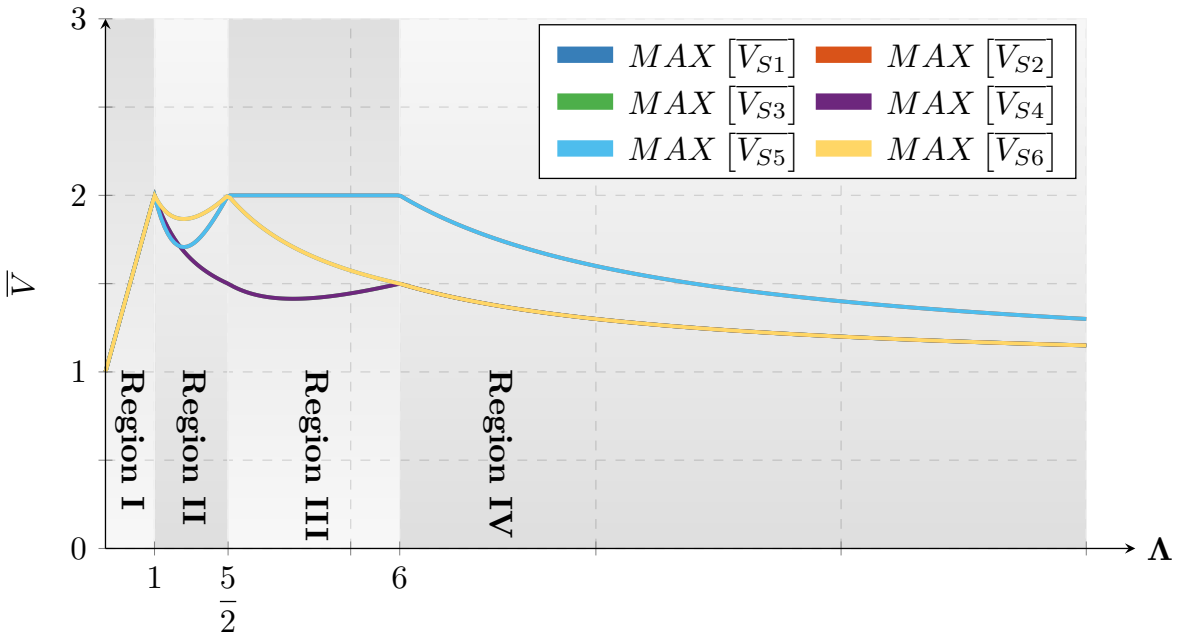


Figure 54 – 4L-RFLCC Switches $S_1 - S_6$ Maximum Voltage Stress Characteristic under Region I to IV condition.



5 PROTOTYPE DESIGN & COMPONENT SELECTION

5.0.1 Project Specification & Design Methodology

As mentioned previously, a potential target application is the interface in between solar photovoltaic panels and a 400V DC microgrid bus, where the proposed converter could potentially track the optimum point for the solar panel and/or limit its energy production. Based on that, the Table 17 comprises the major specification list for the proposed converter. Additionally, with the intention of maximizing the power density, a high switching-frequency is employed to minimize the size of the resonant tank whereas a wide range is utilized in order to explore the output characteristics.

Table 17 – Target 4LRFLCC Prototype Design Specifications.

Target Prototype Design Specification	
Parameter	**Value**
Maximum DC Input Voltage	133.33V
Maximum DC Voltage Gain	3
Maximum Output Power	530W
Switching Frequency	10-500kHz

There exist three design constraints to be fulfilled, as listed below, in order to secure ZCS operation within every Operating Region.

1. The Load Resistance shall be higher or equal to the Equivalent Minimum Load Resistance at the Maximum Voltage Gain; Conditional soft-switching is achieved otherwise, depending on the load and switching frequency condition.

2. The characteristic impedance Z_r is design such that $\mathbf{\Lambda} = 6$ is met at the maximum voltage gain condition and output power; This attribute allows the proposed converter to operate under output voltage regulation region by fulfilling $\mathbf{\Lambda} \leq 6$.

3. The relationship in between the resonant frequency and switching frequency is lower or equal to $3/2$; This attribute relates to the operating condition where the 4L-RFLCC operates in DCM (ZCS condition). Zero-current soft-switching is not achieved otherwise.

The rated equivalent load resistance and the resonant frequency are described as shown in (5.1) and (5.2), respectively.

$$R_o = \frac{{V_{OUT}}^2}{P_{OUT}} = \frac{133.33 \cdot 3^2}{530} = 301.89\Omega \tag{5.1}$$

$$\omega_o = \frac{3}{2} \cdot 2 \cdot \pi \cdot f_{SW} = 4.71 \cdot 10^6 \; rad \cdot s^{-1} \tag{5.2}$$

As per the definition of μ_o, the characteristic impedance Z_r can be calculated as shown in Equation (5.3).

$$Z_r = \frac{R_o \cdot \mu_o}{\pi} \cdot \frac{1}{\Lambda} = 10.68\Omega \tag{5.3}$$

As per the definition of Z_r, it is possible to determine the resonant capacitance C_r and resonant inductance L_r, as shown in Equation (5.4) and (5.5).

$$C_r = \frac{1}{Z_r \cdot \omega_o} = 19.87nF \tag{5.4}$$

$$L_r = \frac{1}{{\omega_o}^2 \cdot C_r} = 2.27\mu H \tag{5.5}$$

5.0.2 Component Stresses

Given the expected wide operating range, the Active Switches $S_1 - S_6$ shall withstand a larger range of peak current and voltage stress, as shown based on the normalized current and voltage stresses in Figure 53 and 54, respectively. Thus, given the design choice's characteristic impedance, derived in Equation (5.3) and the target Maximum Input Voltage, the absolute peak current and voltage within the Operating Region I and IV are as shown in Figure 55 - 60.

Figure 55 – Absolute Peak Current and Voltage Stresses under Target Specification Range for: Active Switch S_1.

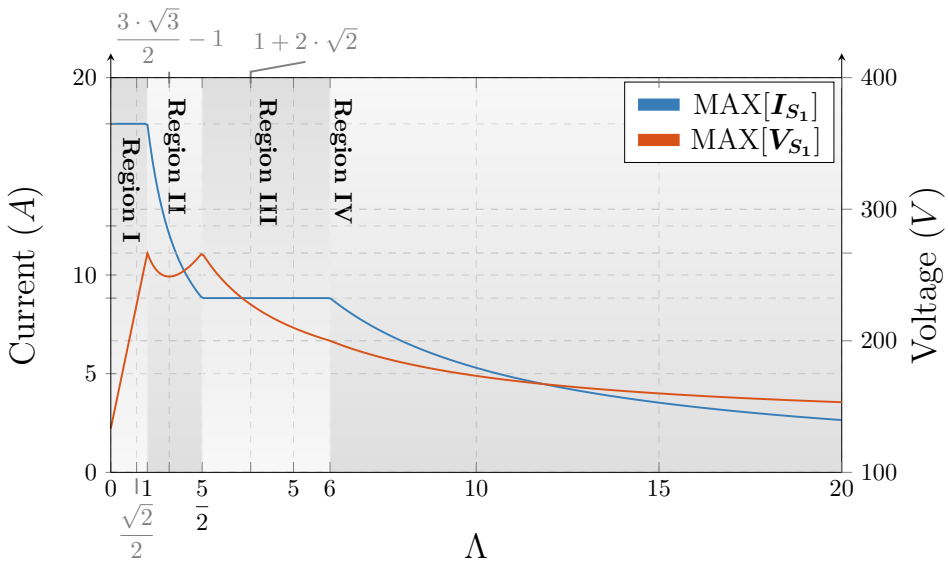


Table 18 displays the maximum peak current and voltage stress, within each target operating region, for the Active Switches $S_1 - S_6$. The maximum absolute values aid in the

Figure 56 – Absolute Peak Current and Voltage Stresses under Target Specification Range for: Active Switch S_2.

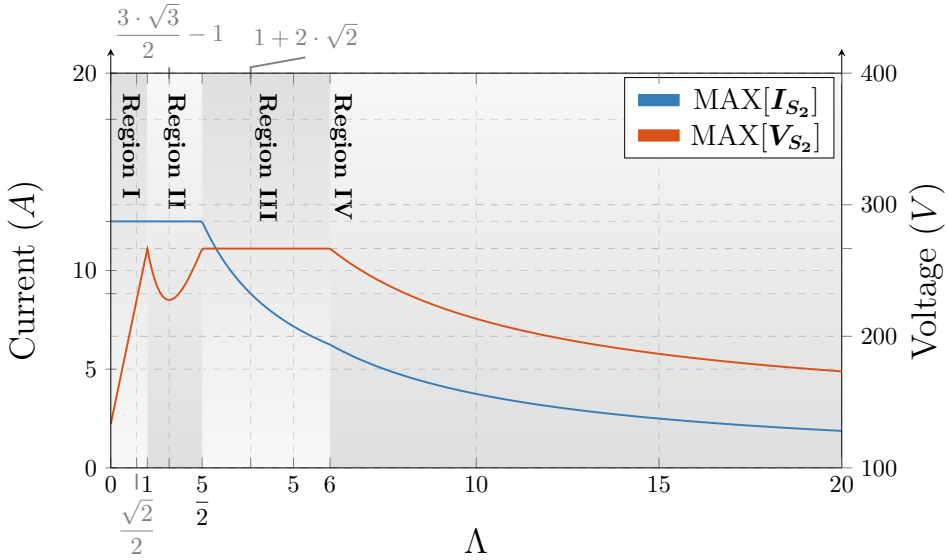
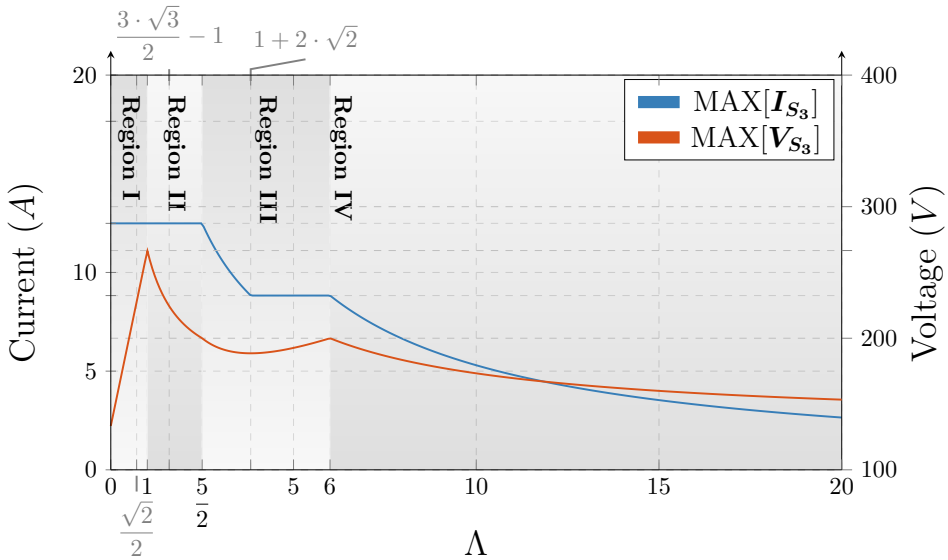


Figure 57 – Absolute Peak Current and Voltage Stresses under Target Specification Range for: Active Switch S_3.



component selection in terms of semiconductor blocking voltage as well as the saturation current for both semiconductors and resonant inductor.

The heating effect, on the other hand, is due to the accumulative current stress over time, which determines how the junction temperature would behave according to the cooling system as well as the components' properties.

Figure 58 – Absolute Peak Current and Voltage Stresses under Target Specification Range for: Active Switch S_4.

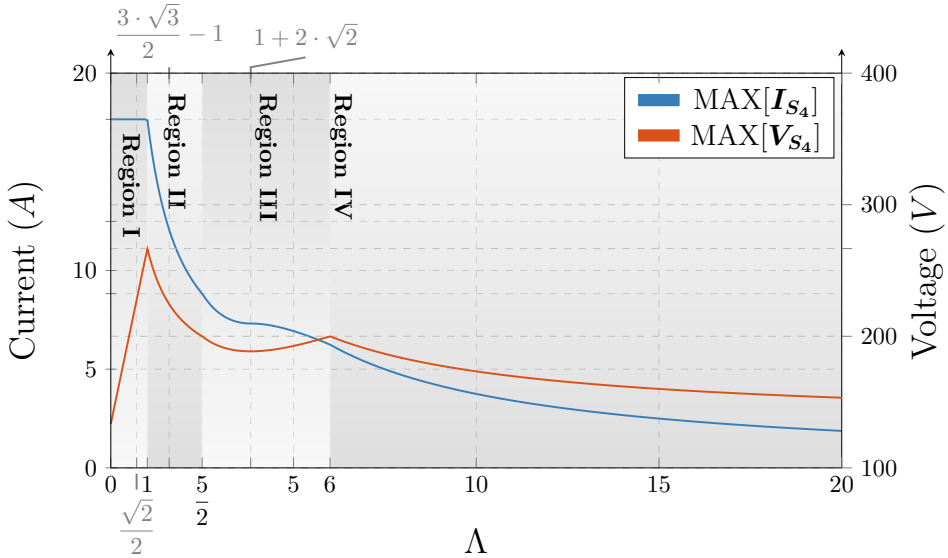
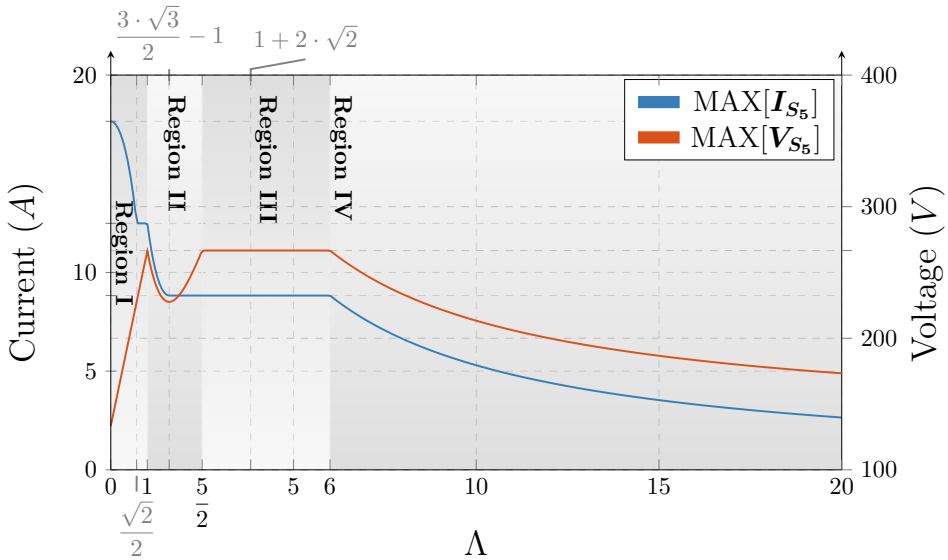


Figure 59 – Absolute Peak Current and Voltage Stresses under Target Specification Range for: Active Switch S_5.



5.0.3 Resonant inductor L_r

A conventional inductor is generally designed in order to sustain a small current ripple ΔI_{pp}, compared to the DC component. Due to that, the magnetic flux swing is small and the design choices can focus on minimizing the winding losses by choosing the right wire's gauge and DC and AC effective resistance in order to avoid overheating. A small magnetic flux swing is also beneficial to the minimum number of turns to avoid saturation while also minimizing the total wire length. Equation (5.6) shows the general rule to be met for the inductor design.

Figure 60 – Absolute Peak Current and Voltage Stresses under Target Specification Range for: Active Switch S_6.

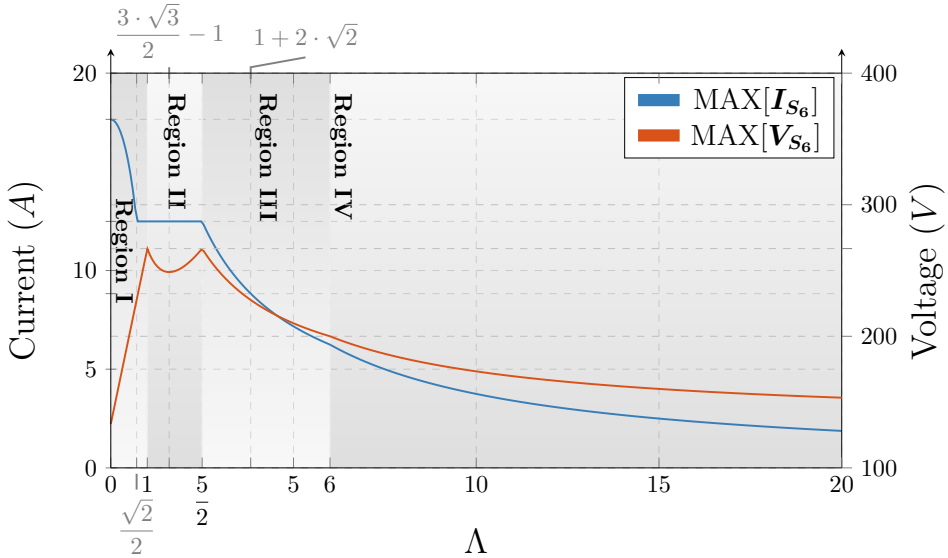


Table 18 – Summary of the distribution of maximum peak voltage and current stresses in the Switches S_1 - S_6 under Region IV condition.

		Operating Region							
		I		**II**		**III**		**IV**	
		V_{MAX}	I_{MAX}	V_{MAX}	I_{MAX}	V_{MAX}	I_{MAX}	V_{MAX}	I_{MAX}
Switches $S_1 - S_6$	S_1	266.67	17.66	266.67	17.66	266.67	8.83	200	8.83
	S_2	266.67	12.49	266.67	12.49	266.67	12.49	266.67	6.24
	S_3	266.67	12.49	266.67	12.49	200	12.49	200	8.83
	S_4	266.67	17.66	266.67	17.66	200	8.83	200	6.24
	S_5	266.67	17.66	266.67	12.49	266.67	8.83	266.67	8.83
	S_6	266.67	17.66	266.67	12.49	266.67	12.49	200	6.24

$$B_s \cdot n \cdot A_e \geq L \cdot I_p \tag{5.6}$$

By choosing a set of number of turns n and an effective core area A_e, while the three remaining parameters, maximum flux density B_s, inductance L and the peak current I_p, are defined as per the system-level target specification and the converter behavior. Therefore, it is important to emphasize the primary objective is to avoid saturation. However, each design choice possibility is associated with a potential core loss and winding loss, which may not fulfill other requirements such as maximum winding and core temperature.

The general rule remains the same if the current ripple is large. However, due to this conditions, the magnetic flux swing is also larger and different precautions need to be taken. In

this case, as an example, the number of turns n shall be higher to reduce the B field and control the core losses.

The proposed 4L-RFLCC increases the effective switching frequency, seen by the inductor, which in turn reduces the inductance requirement and change the characteristic impedance to fulfill a maximum output power. This feature leads to a smaller number of turns to sustain the general rule, shown in Equation (5.6). Additionally, it has been seen the 4L-RFLCC reduces the peak current I_p, in comparison to the 3L-RFLCC, which also leads to a relaxation in the general rule.

To further miniaturize the resonant tank, the target specification sets a high switching frequency, which leads to a reduced inductance requirement and a nominal resonant frequency ω_0 at 1500kHz. The two attributes counter each other as the higher resonant frequency imposes bigger challenges in the frequency characteristic and core losses.

Firstly, the winding concept is defined in order to minimize the high-frequency effects into the conduction performance. The skin-depth, as shown in Equation (5.7), is taken as baseline, which represents the depth below the surface of the conductor at which the current density has fallen to 0.37 of its full density.

$$\delta = \sqrt{\frac{2 \cdot \rho}{\omega \cdot \mu_r}} \tag{5.7}$$

where ρ and μ_r are called the material conductivity and permeability, respectively, whereas ω is the equivalence of the frequency of interest. Therefore, by calculating the skin-depth δ, shown in Equation (5.8), the baseline wire gauge can be defined.

$$\delta = \sqrt{\frac{2 \cdot \rho}{\omega \cdot \mu}} = \sqrt{\frac{2 \cdot 1.68 \mu\Omega \cdot cm}{2 \cdot \pi \cdot 1500 kHz \cdot 0.99}} = 0.053 mm \tag{5.8}$$

Equation (5.8) imposes a restriction which is only suitable for Litz wire. Therefore, while fulfilling the skin-depth prerequisite and the 4L-RFLCC current stresses, a wire-gauge of 0.04mm (46 AWG) is chosen with 1000 strands. The table 19 shows the chosen wire properties.

Due to the very low inductance and the effective switching frequency requirement, a magnetic core-based inductor is very challenging to achieve. The number of turns shall be very high in order to keep the maximum B field up to 50mT or lower. The table 20 shows a list of inductor design iterations to fulfill the target specification.

As shown in Table 20, the bigger the core, the lower the number of turns; as a consequence, the lower the required air gap. However, the core losses increase proportionally for bigger cores, leading to an unreliable design. On the other hand, the smaller cores require a large air gap, making it also very challenging to keep the magnetic properties stable and without sacrificing too much the fringing effect.

Table 19 – 46 AWG Wire Properties utilized for the resonant inductor construction.

46 AWG Wire Specifications	
Properties	**Value**
Nominal Diameter	0.040 mm
Circular Area	0.0012 mm^2
Maximum DC Resistance	14.92 $\Omega \cdot m^{-1}$
Litz-Wire Equivalent	
Maximum DC Resistance	14.92 $m\Omega \cdot m^{-1}$

Table 20 – List of Inductor Magnetic core-based iteration based on the prototype target specification.

Magnetic Core Set		**Construction Paramaters**	
# 1	**# 2**	**Minimum Number of Turns**	**Simplified Air Gap** (mm)
ELP 22/6/16	I 22/2.5/16	11	5.23
ELP 38/8/25	I 38/4/25	5	2.69
EQ 25/5.6/18	I 25/2.3/18	10	4.59
ER 25/6/15	I 25/3/15	12	5.72
PQ 26/25	PQ26/25	7	3.33

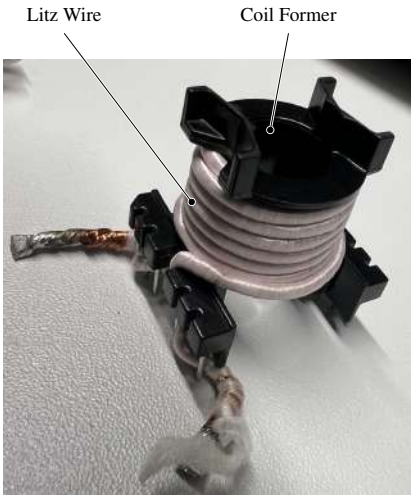
Therefore, given the small inductance requirement, a air-core inductor is also a contender, and the chosen strategy, as it no longer imposes any limitation in terms of core losses due to the very-high effective switching frequency. The major drawbacks are the increased number of turns and the higher magnetic H field radiated from the coils. The air-core inductor has been wound in a PQ26/25 bobbin, as shown in Figure 61, and validated using a Bode100 impedance measurement tool. Equation (5.9) show the measured inductance value based on the built inductor.

$$L_{prototype} = 2.21\mu H \tag{5.9}$$

5.0.4 Resonant flying capacitors C_{r1} and C_{r2} & DC-link Capacitors

The Resonant flying capacitors are fundamental to the operation of the proposed 4L-RFLCC while having a importance as they are intended to transport and delivery the energy packages to the output. As seen in Figure 52, the resonant capacitors are exposed to a wide range of voltage biasing while exhibiting a non-negligible voltage ripple. The aforementioned system-level characteristics impose different requirements in the type of capacitor which are suitable for such application, as described below.

Figure 61 – Resonant Inductor Design and Built for the purpose of validating the proposed 4L-RFLCC.



1. The Capacitor shall have a good AC and DC bias characteristic in order to sustain its capacitance.

2. The dissipation factor shall be very low to minimize losses.

3. The parasitic inductance shall be low to minimize the voltage ringing within adjacent Flying Capacitor Commutation Cells (FCCC).

Film capacitor technology is known for having a great bias characteristic; thus, being suitable for resonant applications. However, its capacitance density and dissipation factor makes it a bulky solution when exposed to higher current stresses. Ceramic capacitors have the best capacitance density and dissipation factor, while the majority exhibits poor or average bias performance. Thus, imposing limitations on which technology and how reliable the ceramic capacitors are for resonant applications.

A *KEMET* MLCC's KC-LINK family exhibits excellent properties which fulfill the requirements listed above. Therefore, in order to achieve the desired capacitance, as shown in Equation (5.4), Table 21 shows the Resonant Capacitors and their main properties.

The DC-link capacitors aim to decouple the high-frequency current content from the DC Power Supply as well as to increase the energy quality to the output load. Given the input current-source and output voltage-source characteristic of the proposed 4L-RFLCC, different requirements are imposed to the input and output DC-link capacitors.

As the input impedance is highly inductive, the input commutation loop, which is composed by the resonant inductor L_r and the input voltage, does not require stringent requirements in terms of ESL. However, by increasing the ESL, the Differential-Mode (DM) conducted emissions to the input power supply will tend to increase. On the other hand, since the Output Characteristic is a Voltage-Source, its Output Current's profile is pulsating. As the Proposed 4L-RFLCC operates under DCM condition, the pulsating characteristic is not as challenge to the

Table 21 – Capacitor's propertiesResonant Capacitor for the Proposed 4L-RFLCC to fulfill the requirements based on the Target Specifications.

Resonant Capacitor Specification						
Manufacturing Part Number	**Type**	**Capacitance (nF)**	**Voltage (V)**	**ESR @ 1MHz $(m\Omega)$**	**ESL (pH)**	**Package Size**
CKC21C123JEGACAUTO	MLCC	12	1200	3.31	650	SM2220
CKC21C682KWGACAUTO	MLCC	6.8	650	7.92	770	SM2220
Total Capacitance (nF)						
18.8						
Resultant Resonant Frequency (kHz)						
784.29						

outermost devices S_1 and S_6. However, by operating under CCM condition, the aforementioned characteristic is very important.

Given the operating characteristics, the Input and Output DC-Link Capacitor requirements are listed below.

1. The Input and Output Capacitor shall withstand high-frequency current content without excessive heat dissipation.

2. The Input Capacitor shall decouple the high-frequency current content in order to minimize the DM conducted emissions.

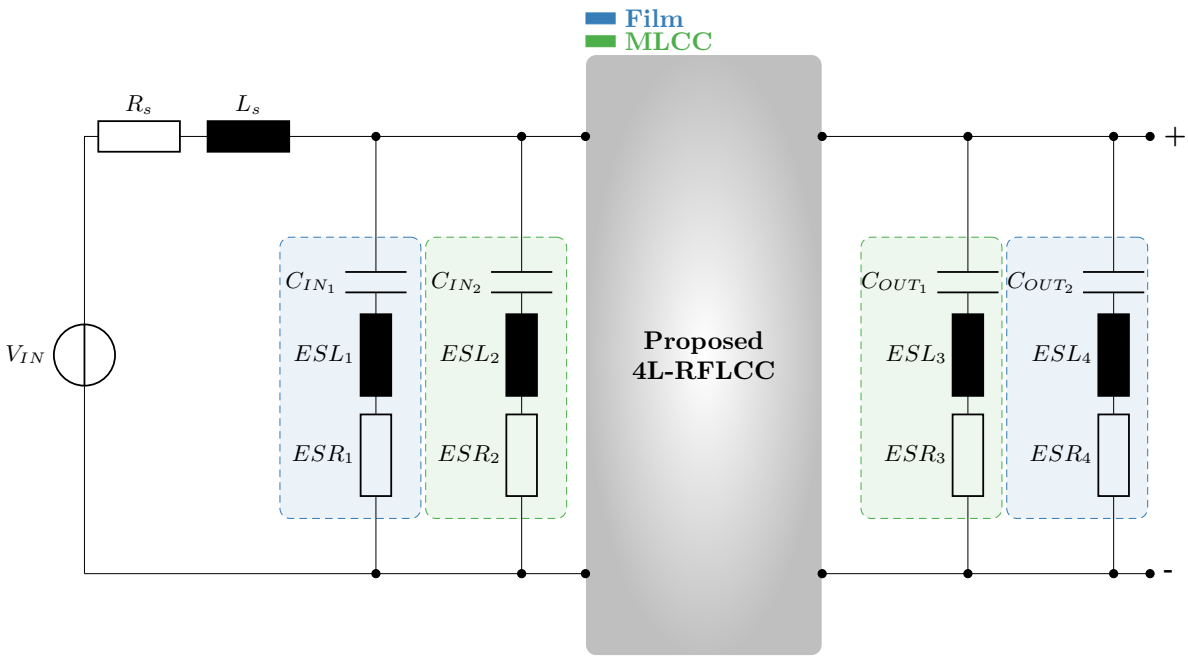
3. The Output Capacitor shall be optimized for ESL and ESR in order to increase the robustness of the outermost FLCCC.

4. The Output Capacitor shall be minimize the Output Voltage Ripple in order to increase the energy quality to the output load.

Different technologies can fulfill the requirements, such as Electrolytic, Film and MLCC. The Electrolytic capacitor exhibits the highest capacitance density. However, at 400V output, its availability, with an average capacitance density, proper derating, and high-frequency current handling, is not large. Therefore, the Eletrolytic capacitor could be utilized for energy-storage purpose in combination with a different technology to suppress the high-frequency current content. The Film Capacitor is becoming more popular for DC-link applications, exhibiting a better high-frequency current handling, compared to the Electrolytic Capacitor, but suffers from the capacitance density and often it does not require a voltage derating as the Electrolytic Capacitor. An emerging MLCC, for DC-Link purposes, is the *CeraLink* from *TDK*. It exhibits high voltage ratings and high capacitance density while maintaining the best high-frequency properties given by the MLCC technology. As a consequence, it can be utilized for both Energy Storage and High-Frequency Decoupling in the Input and Output of the proposed 4L-RFLCC.

Therefore, the proposed DC-link architecture is shown in Figure 62, where two different technologies are employed in order to fulfill the requirements.

Figure 62 – DC-link Capacitor Architecture for the Proposed 4L-RFLCC Prototype.



The Table 22 exhibits the proposed DC-link capacitors that represent the architecture shown in Figure 62.

Table 22 – DC-link Capacitor's properties for the Proposed 4L-RFLCC to fulfill the requirements based on the Target Specifications.

DC-Link Capacitor Specifications							
	Manufacturing Part Number	**Type**	**Capacitance** (nF)	**Voltage** (V)	**ESR** $(m\Omega)$	**ESL** (nH)	**Package Size** (mm)
C_{IN_1}	DCP4G061007I	Film	100	400	2.5	N/A	31x46x41.5
C_{OUT_2}	DCP4G061007I	Film	100	400	2.5	N/A	31x46x41.5
C_{IN_2}	CKC21C682KWGACAUTO	MLCC	0.039	650	3.33	0.75	3.2x4.5x2.5
C_{OUT_1}	B58035U5106	Ceramic	6	650	3	2	30x7.4x9.1

5.0.5 Active Switches $S_1 - S_6$

As describe previously, the active switches $S_1 - S_6$'s main function is to realize the power conversion by switching at $f_{SW.min}$ and $f_{SW.max}$ in order to regulate the output voltage at the required output voltage range, $V_{OUT.min}$ and $V_{OUT.max}$, given a range of output load condition $I_{OUT.min}$ and $I_{OUT.max}$.

As a consequence of the different operating conditions, the Active Switches $S_1 - S_6$ undergo different current and voltage stresses, as described in Section 4, and shown in Table 18,

for the system requirements defined in Table 17. In order to minimize the impact of the current and voltage stresses into the system performance, the choice of semiconductor technology is fundamental since the Active Switches are likely to be the most dissipative component amongst all.

Wide-band-gap (WBG) devices have become popular for several different applications, ranging from low voltage to high voltage as well as low power to high power due to its attractive switching characteristics as well as low ON-resistance. Thus, enabling higher efficiency and higher power density compared to their equivalents Si MOSFETs and IGBTs.

By breaking down the source of losses in a semiconductor device, [Jafari et al. 2020, Cittanti, Vico e Bojoi 2022] defines the major contributions according to the application type (i.e. SSW or HSW) which are utilized in order to interpret different FoMs. The conduction losses are due to the resistive behaviour of the device, shown in Equation (5.10), which is associated from the semiconductor's material properties, mainly dependent upon the electron mobility and energy gap in order to increase the conduction capability of the conduction channel and minimize the channel length, respectively.

$$P_{con} = R_{DS.on} \cdot {I_{RMS}}^2 \tag{5.10}$$

whereas the switching losses are derived based on the terms which are dependent upon the switching frequency f_{sw}, as shown in Equation (5.11), where the P_G is the gate driving loss, P_{dt} is the dead-time reverse conduction loss, P_{oss} is the output capacitance charge/discharge loss, P_{rr} is the reverse recovery loss and P_{vi} is the loss generated by the overlap of voltage and current during the switching transition.

$$P_{sw} = P_G + P_{dt} + P_{oss} + P_{rr} + P_{vi} \tag{5.11}$$

Each of these losses are highly dependent upon the semiconductor technology as well as the operating behaviour of the converter. While in Hard-Switched PWM-based converters the P_{vi} may be the most dominant source of losses in High-voltage applications, the dominance may differ for low-voltage applications in which the semiconductor devices generally possess a greater switching performance due to their thinner drift region, and as a consequence lower $R_{DS.on}$ which leads to a minimization of the chip size. As a consequence, in low-voltage applications the dominance may shift towards P_G instead of P_{oss}.

Likewise, the dominance differs when considering Soft-switched PWM-based converters where the P_{vi} and P_{rr} are negligible due to generally the ZCS or ZVS operating behaviour. Thus, the P_G and P_{oss} becomes more relevant depending on the semiconductor technology as well as the breakdown voltage in the system. However, at very high switching frequency applications, where ZVS condition may not be achievable, the equivalent output capacitance losses P_{oss} become crucial due to its inherent behaviour of charge/discharge loss.

Several different entities have attempted to derive Figure of Merits (FoM) [Shenai 2018] [Wang, Wang e Zhang 2008] [Cittanti, Vico e Bojoi 2022] in order to assist the assessment of the semiconductor's performance irrespective of the application, whereas [Anderson et al. 2020] [Zulauf et al. 2019] [Jafari et al. 2020] propose methods to analyze different semiconductor technologies according to its application ranging from switching mechanism (SSW or HSW) to topology-related mostly based on available data from the semiconductor's manufacturers. [Cittanti, Vico e Bojoi 2022] summarizes different FoMs, which are applicable for hard-switched PWM-based converters, and also proposes a new FoM which correlates the reverse-recovery losses as well as the switching frequency and junction temperature of the device. Despite of being more applicable for HSW applications, the different FoMs can lead to a good assessment of the semiconductor performance mainly due to the fact that some of them are related to the minimum theoretical switching losses which are also applicable for SSW applications due to the inherent dissipative charge/discharge process of the output capacitance C_{oss}. The relevance of different FoMs depends greatly on the operating behaviour, and operating conditions like breakdown voltage and operating current, due to the dominances of different source of losses.

Firstly, the BHFFOM which correlates the conduction characteristic with the hard-switching losses associated with the input capacitance C_{iss}, as shown in Equation (5.12). BHFFOM becomes more relevant when the gate losses P_G becomes dominant in comparison to the P_{oss}. On the other hand, for soft-switching applications [Jafari et al. 2020] the C_{iss} information available in components' datasheet are generally associated with hard-switching applications. As a consequence, the gate driving losses tends to be higher than the real gate driving losses when applicable for soft-switching applications. As a consequence, the tendency is that measurement method where the energy associated with the non-linear input capacitance C_{iss} and the gate driving voltage represents the gate driving losses.

$$BHFFOM = \frac{1}{R_{DS.ON} \cdot C_{iss}} \tag{5.12}$$

Differently from the BHFFOM, [Anderson et al. 2020] addresses FoMs associated with the dominance of the semiconductor's output capacitance C_{oss} in the source of switching losses, based on NHFFOM, as shown in Equation (5.13), and DFOM, as shown in Equation (5.14), respectively.

$$NHFFOM = \frac{1}{R_{DS.ON} \cdot C_{oss}} \tag{5.13}$$

$$DFOM = \frac{1}{\sqrt{R_{DS.ON} \cdot C_{oss,Q}}} \tag{5.14}$$

NHFFOM is a similar representation as the BHFFOM, which does not represent the semiconductor capacitive losses [Kasper et al. 2016] completely due to its interpretation as a

matter of charge-equivalence and energy-equivalence in order to assess the performance of the semiconductor device. Whereas DFOM represents a quantified assessment of the minimized semiconductor losses, under a HSW condition, for a bridge-leg configuration converter in which the charge-equivalent output capacitance [Kasper et al. 2016] is utilized in order to simplify the assessment of the hard switching losses. The utilization of the charge-equivalent output capacitance is due to the interpretation of the capacity of a bridge-leg configuration converter, with an inductive load and high current, to fulfill a ZVS condition where there exist a resonant behaviour in between the inductive load and the output capacitance of both switches. Thus, the higher the $C_{oss,Q}$ the slower the switching transient and the higher the pre-conditions shall be in order to overcome the higher $C_{oss,Q}$, according to Equation (5.15).

$$\frac{1}{2} \cdot L \cdot {I_1}^2 \geq C_{oss,Q}\left(V_{DS}\right) \cdot {V_{DS}}^2 \tag{5.15}$$

Even though DFOM clearly represents the ability of a semiconductor device of switching fast under a HSW condition, it can still be interpreted in a soft-switched converter application due to the possibility of assessing the output capacitance C_{oss} losses under a ZCS condition as it is equivalent to the minimum theoretical hard-switching losses. The turn-OFF mechanism, under a theoretically non V-I overlap corresponds to the energy stored in the output capacitance, which ideally leads to no energy dissipation due to the current flowing as a capacitive displacement rather than a drift current. Upon a subsequent turn-ON mechanism, the short-circuiting of the output capacitance then leads to the energy dissipation. Therefore, despite of ensuring a ZCS condition, the active switches are still exposed to a minimum switching frequency given the $Eoss$ as shown in Equation (5.16).

$$E_{oss} = \int_0^{V_{DS.max}} C_{oss}\left(v\right) \cdot v \, dv \tag{5.16}$$

The DFOM is further generalized to a multi-level configuration [Anderson et al. 2020]. Thus, introducing an interconnection in between the semiconductor technology and the topology configuration, also shown in Equation (5.17). The assessment shows the ability of the topology's choice to enable different semiconductor technologies while optimizing the semiconductor chip area, enabling further optimization of the system according to different system requirements.

$$XFOM\left(V_{DS}, N\right) = N \cdot DFOM\left(\frac{U_{DS}}{N}\right) \tag{5.17}$$

Complementing the aforementioned FoMs, [Cittanti, Vico e Bojoi 2022] proposed a new FoM considering the reverse recovery losses, as shown in Equation (5.18), in order to distinguish the ability of a semiconductor technology of neglecting the reverse recovery. As a consequence, leading to a potential performance comparison in between GaN and SiC devices.

Furthermore, it introduced the switching frequency and the junction temperature as a parameter for the comparison as it impacts the assessment of the reverse recovery losses. The study found that the additional elements introduced clear boundaries in between GaN and SiC with a non-linear boundary line. GaN devices exhibited a dominance in the very high switching frequency but with a dependency towards the junction temperature due to the strong ON-resistance's temperature dependency. Whereas SiC devices exhibited a dominance in the medium to high junction temperature while providing a stable condition at the low switching frequency range.

$$HSFOM = \frac{1}{\sqrt{R_{DS.on} \cdot Q_{oss}} + k_i \cdot \sqrt{f_{sw} \cdot V_{sw}} \cdot \tau_{rr}} \tag{5.18}$$

By exploring soft-switching, the DFOM and/or HSFOM may lead to unclear performance assessment as its main focus is to determine a coefficient that incorporates both minimum theoretical switching losses and the conduction performance as well as the reverse recovery ability, particularly to the HSFOM. As a result, a device, and semiconductor technology, may be misinterpreted purely given by the component level's assessment.

The topology level introduces an important factor to the component definition as it may introduce the aforementioned characteristic, i.e. soft-switching. By ensuring ZVS, within the turn-ON process, the output capacitive stored energy E_{oss} is either no longer dissipated through the FET's channel, during the turn-ON process, or is partially dissipated due to quasi-resonant behaviours. By introducing quasi-resonance, the power loss distribution tilts to the conduction losses.

Other factors, such as power density and mechanical constraints, may also affect the component selection as it introduces additional FoMs.

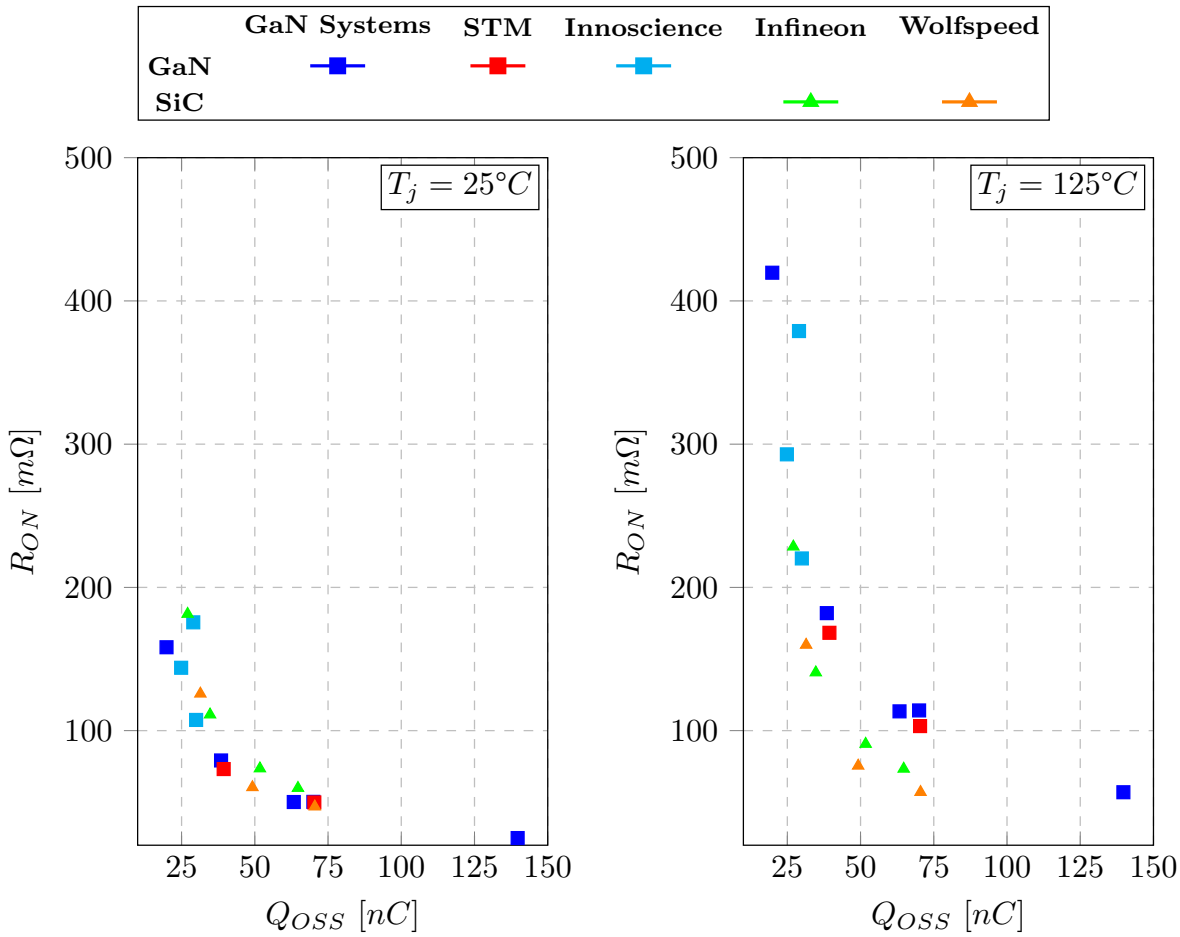
Given the electrical attributes, shown in Table 18, 650V wide band-gap devices are the most suitable candidates due to its high-electron mobility, which in turn lead to a stronger conduction channel in a smaller footprint, compared to their counterpart as Si MOSFETs and/or IGBTs. The Figure 63 display the main attributes that affects the conduction performance and the minimum theoretical switching losses for 650V devices and surface-mounted package type.

There exist an inverse relationship in between the R_{ON} and Q_{oss} independent from the semiconductor technology, indicating that a balance in between switching and conduction performance shall exist.

SiC and GaN devices are comparable in terms of the aforementioned attributes at lower junction temperature conditions, with a small drawback towards the SiC devices due to the package size. On the other hand, as mentioned previously, GaN devices have a worse performance at higher junction temperatures, which is highlighted in the difference between the two distributions, suggesting that SiC devices may be a better fit for applications where a wide operating temperature requirement is existent, independent from the operating switching frequency of the proposed converter.

The proposition is applicable when considering a ZCS condition is fulfilled at any given

Figure 63 – SiC/GaN R_{ON} and Q_{OSS} distribution per device for different junction temperature conditions.



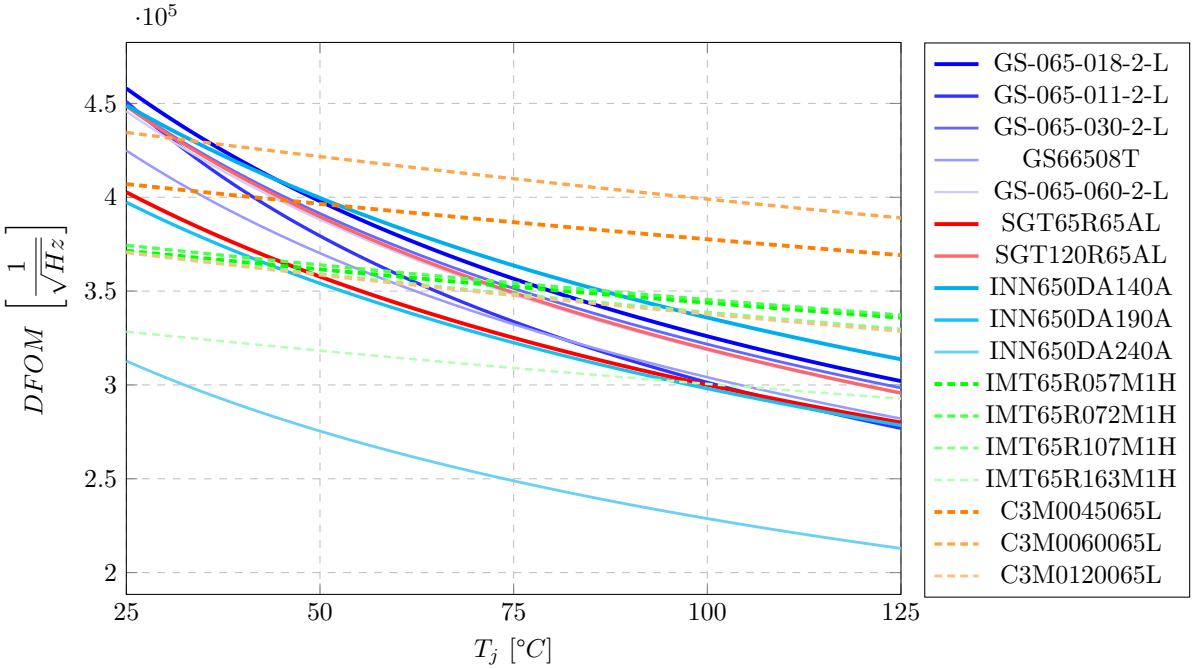
operating condition. By considering the proposed 4L-RFLCC, the ZCS condition is not achieved only at heavier load conditions where the output voltage control loop demands a higher switching frequency. As a consequence, the converter no longer operates in the DCM, leading to reverse recovery and voltage-current overlap.

By utilizing the DFOM, the Figure 64 highlights the junction temperature dependency in the DFOM assessment of the different devices. Correlated to 63, SiC outruns the GaN's DFOM performance as the junction temperature increases.

According to this case study, *Gan Systems*'s *GS-0650-180-2-L* device has the best DFOM performance at the lower junction temperature due to the best balance in between conduction and minimum theoretical switching losses performance under a very small package (PDFN8x8), whereas *Wolfspeed*'s SiC *C3M0060065L* quickly outruns the other devices when the junction temperature increases higher than 37°C. Worth noting that neither of the GaN and SiC candidates aforementioned have the lowest R_{ON}, suggesting that the bigger the die size may not be correlated with better overall performance due to the abrupt increase in the output capacitances.

Despite of the better performance at a wider junction temperature range, SiC devices' drawback is the introduction of higher reverse-recovery and VI's overlap losses in a CCM

Figure 64 – SiC/GaN DFOM performance assessment as a function of junction temperature.



condition scenario. Although the 4L-RFLCC is prompted to operate under ZCS, within its majority of operating range, extra operating conditions, where the converter operates under CCM, are subjected to be evaluated. As a consequence, the extra switching losses may compensate the conduction losses' rise as a function of the junction temperature. Therefore, the component selected for the Active Switches is *GS-0650-180-2-L* from *Gan Systems*.

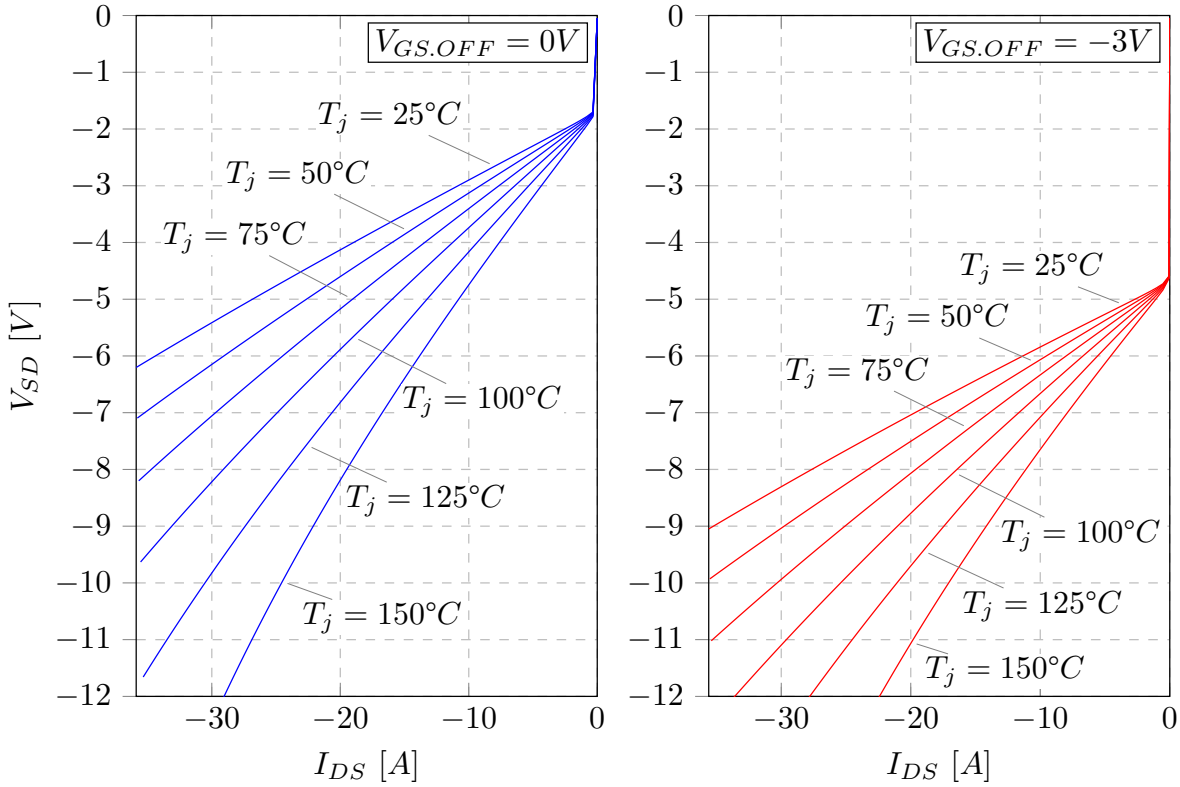
Even though the GaN device is capable of operating in the third quadrant, also known as reverse conduction, its reverse conduction characteristic is highlighted by a large forward voltage drop, similar to one presented in a diode. Thus, leading to a higher conduction losses in the asynchronous switches S_4 - S_6. Figure 65 represents the reverse conduction characteristic for the *GS-0650-180-2-L* at different junction temperatures and OFF-state gate voltage extracted from *LTSpice*® simulation model.

In order to introduce robustness and stability to the 4L-RFLCC, the turn-OFF voltage is chosen as $-3V$. As a consequence, the V_{SD} becomes too high to be manageable, as shown in Figure 65. In order to overcome the excessive voltage drop, a anti-parallel SiC Diode is placed with every asynchronous Active Switch S_4 - S_6.

The addition of the SiC Diode introduces a reduced forward characteristic in comparison to the reverse condition characteristic, as shown in Figure 66, by comparing the Diode-like characteristic of both *GS-0650-180-2-L* and different SiC Diodes' candidates as a function of I_{DS} with junction temperature T_j as a parameter. On the other hand, it introduces an additional capacitive charge to the device as the $C_{o(Diode)}$ is in parallel to the $C_{o(FET)}$. Thus, introducing additional switching losses.

Similarly, the reverse conduction characteristic is underlined by its strong temperature dependency which introduces a forward voltage difference as high as $\Delta V = -8.07V$ at $T_j =$

Figure 65 – *Gan Systems*'s *GS-0650-180-2-L*'s Reverse conduction Performance with junction temperature as a parameter for different turn-OFF gate voltage.

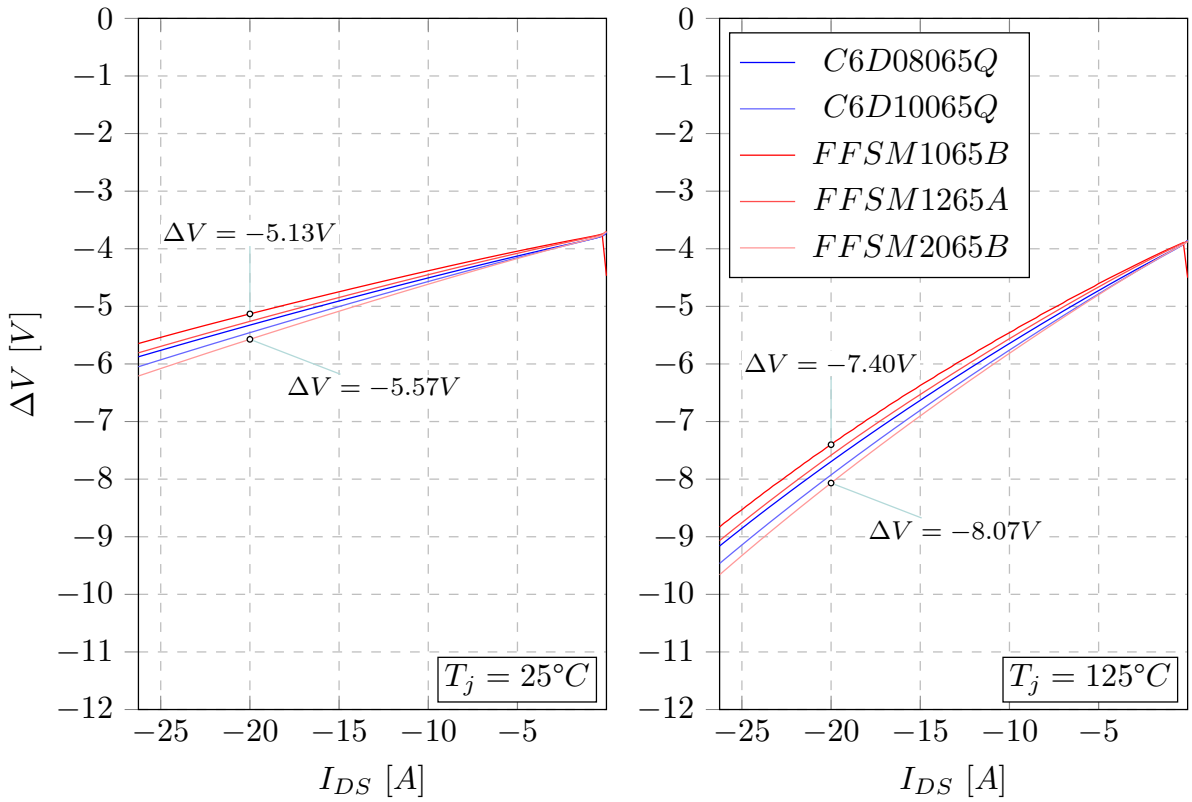


125°C. Different 650V SiC Diodes were analyzed from *Wolfspeed* and *ONSemi* with PDFN8x8 package size; thus, not compromising the target power density.

Due to the component stresses characteristics, amongst Region I to Region IV, the Switches S_4 - S_6 are also subjected to non-ZVS conditions. As a consequence, the contribution of its output capacitance impacts the performance of the converter. The Figure 67 represents the main attributes which impact the performance of the SiC Diode. Amongst the analyzed 650V SiC Diodes, similarly as shown for the FETs, the lower V_F the higher the Q_C. As a consequence, the non-ZVS' s capacitive losses may overrun the better conduction performance at higher switching frequency conditions. Due to the ZCS condition, the SiC Diode does not introduce any additional reverse-recovery losses.

ONSemi 650V devices have a wider range of current rating for the PDFN8x8 package type, going from 10A to 20A average forward current, based on the datasheet. The Device ① corresponds to the *ONSemi*'s *FFSM2065B* with a given electrical characteristic of $V_F\,(10A) = 1.23V$ and $Q_C = 65.37nC$ whereas the device ② corresponds to the *Wolfspeed*'s *C6D10065Q* with a given electrical characteristic of $V_F\,(10A) = 1.27V$ and $Q_C = 35.95nC$. The $\Delta V_F = 46.80mV$ and $\Delta Q_C = 29.42nC$ does not justify the selection of the device ① as the almost double capacitive charge introduces a significant portion of the switching losses at high switching frequency condition. Therefore, the selected component for the Switches S_4 - S_6 is *Wolfspeed*'s $C6D10065Q$.

Figure 66 – *Gan Systems*'s *GS-0650-180-2-L*'s Reverse conduction Performance comparison towards 650V SiC Diodes from different suppliers with forward current I_{DS} as a parameter for different Junction Temperatures T_j.



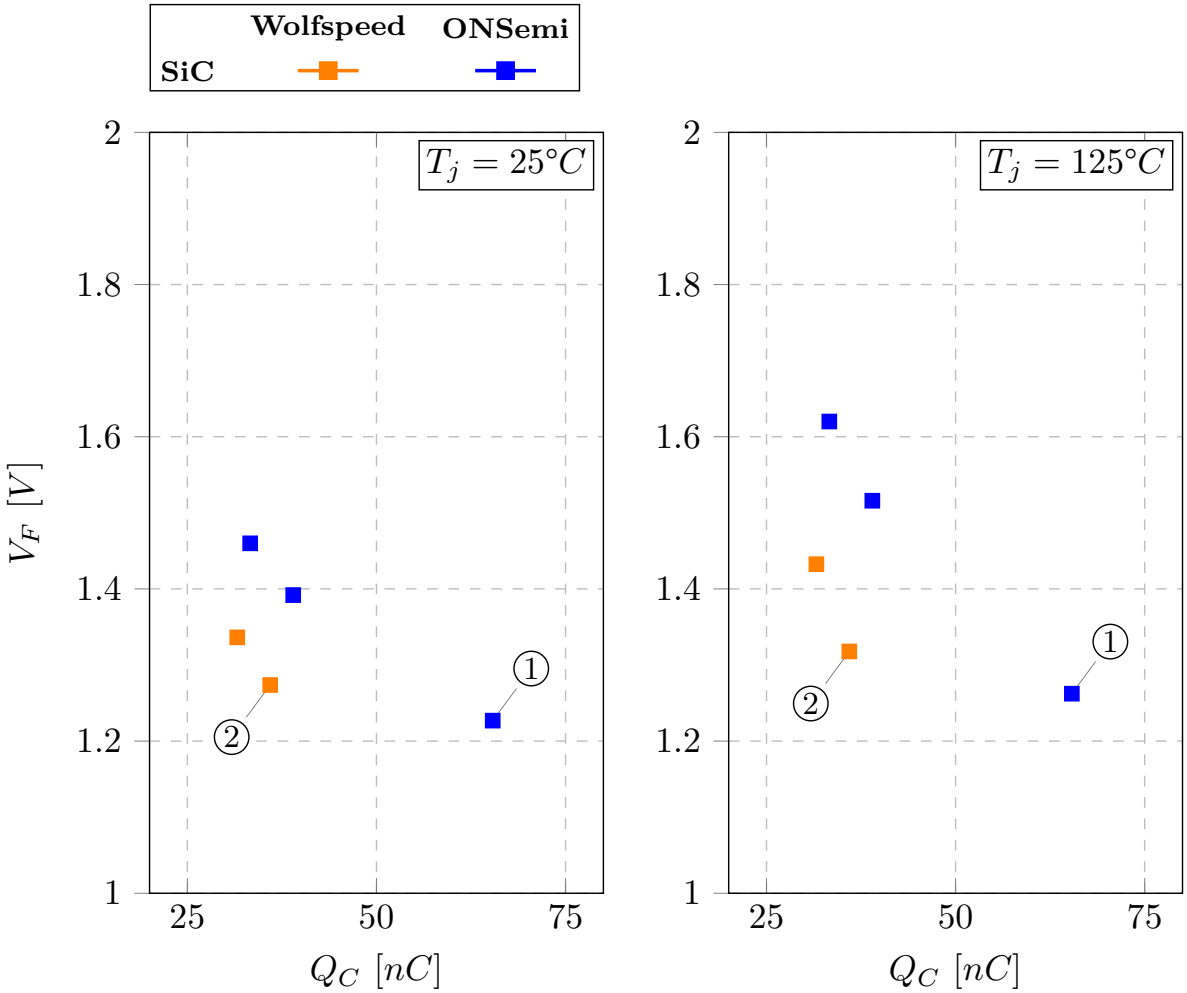
5.0.6 Gate Driver & Auxiliary Circuitries

Given the attribute of multi-level conversion and high-frequency operation, two requirements of floating gate driver power and low dead-time insertion are mandatory to satisfy the operation of the proposed converter. The floating gate driver power characteristic is due to the fact the FET's reference is floating with respect to the power ground reference, which as a consequence makes the drive signal float likewise. In order to overcome the different ground references, the most straight-forward solution is to employ an isolated gate-driver with an external isolated DC/DC solution to provide the required drive voltage. However, such solution reduces the power density, due to the bulky and costly external components, depreciating the potential benefits of a GaN-based and high-frequency operating converter.

Alternatively, a bootstrap solution is widely employed to reduce the system complexity and increase the power density. In a two-level solution, its implementation is simple. However, by increasing the number of levels and the switching frequency, the employment of bootstrap gate driver solution becomes challenging as the forward-voltage drop reduces the available voltage in the successive gate driver stage [Lorenz e Sanchez 2024, Ye et al. 2017], as seen in Figure 68 and also introduces a reduced time for recharging due to the higher switching frequency and widely used interleaved PWM technique.

A known issue, regarding the bootstrap solution, is the overcharge mechanism [Ye e

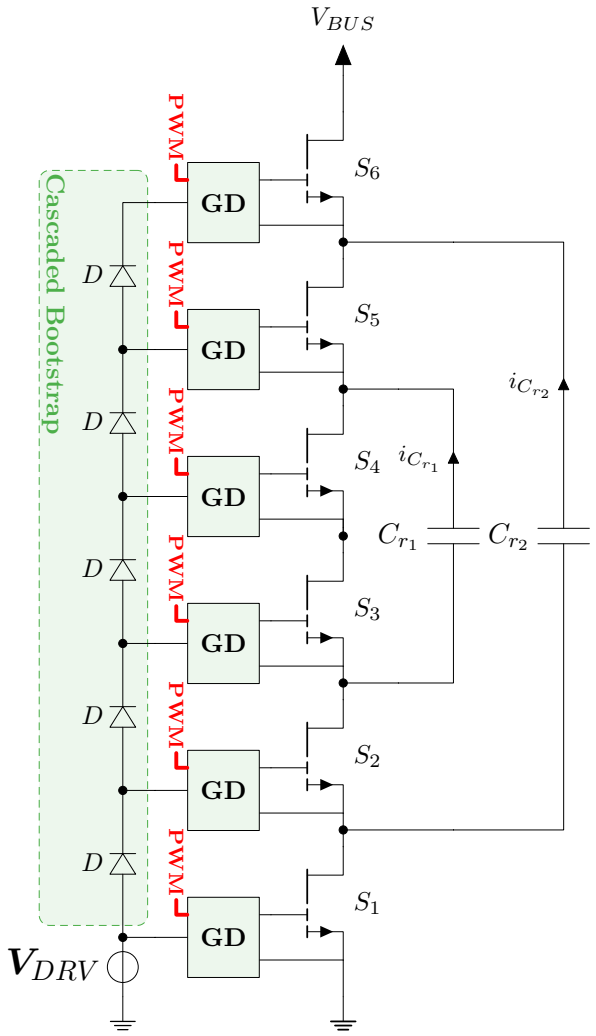
Figure 67 – 650V SiC Diodes V_F and Q_C distribution per device for different junction temperature conditions under 10A forward current condition.



Pilawa-Podgurski 2016], which in practice can aid the cascaded bootstrap solution in multi-level topologies. However, that is topology-dependent and, depending on the inductor current direction, it becomes not applicable for boost-type FCML converter, where the inductor current tends to flow through the high-side devices during the dead-time. Secondly, as it relies on the body-diode reverse conduction, this mechanism can only be used for the low-side devices, and for the first high-side device. Additionally, as this mechanism relies on the reverse conduction of the FET, when the converter operates under ZCS, this mechanism is no longer exploitable. As a consequence, the reverse conduction voltage drop no longer compensates the bootstrap diodes' voltage drop.

Given the limitation due to the inductor current direction and amplitude, [Ye e Pilawa-Podgurski 2016, Ye et al. 2017] introduces a charge pump circuit which explores the differential connection in between high-side and low-side switch in a FCML converter topology, as shown in Figure 69. As a result, the high-side switches are capable of being charged without the use of a isolated DC/DC converter. In non-resonant FCML converter, the flying capacitor are much larger than the bootstrap capacitors; therefore, not interfering with the operating mechanism of

Figure 68 – System-level description of the FCML converter employing Cascaded Bootstrap Gate Drive.



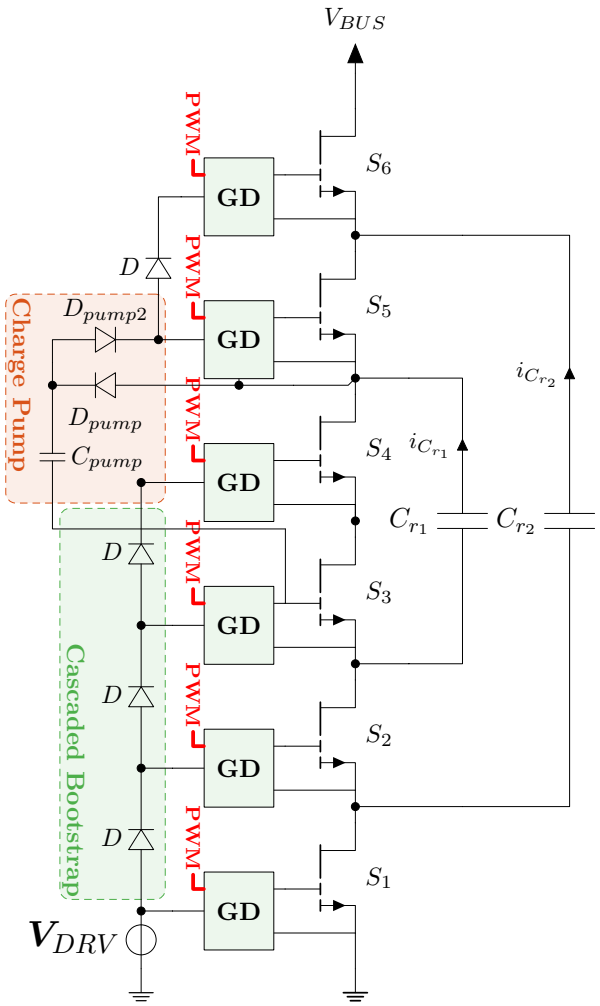
the converter. On the other hand, in resonant FCML converters, the capacitance ratio is much smaller; thus, interfering with the operating mechanism of the resonant converter.

In order to overcome the bootstrap diodes' voltage drop, the GD building block consists of an additional linear conversion stage [Lorenz e Sanchez 2024, Ye et al. 2020] to compensate for the lack of regulation in the bootstrap voltage. Despite of increasing the number of components, it enhances the robustness and reliability of the GaN devices as they require a tightly regulated drive voltage.

The bootstrap solution is widely used for FCML converter, specially the ones associated with buck-type, and lower output voltage condition, where the current direction aids the bootstrap mechanism. As a consequence, a high power density can be achieved due to the simplicity of the structure.

One drawback, associated with the bootstrap solution, is the junction capacitance of the bootstrap diode, which floats in reference to the power ground reference. Due to that, there exist a capacitive charge/discharge depending on the number of levels. The charge-pump architecture

Figure 69 – System-level description of the FCML converter employing Cascaded Bootstrap Gate Drive and Charge-Pump.



can improve this behavior by shifting the ground reference for the bootstrap diodes following the charge-pump connection point. However, it does not eliminate the capacitive charge associated with the junction capacitance. Under lower output voltage conditions, low-voltage schottky diodes can be employed, which reduces the junction capacitance and can support the bootstrap mechanism. However, under high-output voltage condition and high flying capacitors' voltage fluctuation, the floating voltage becomes larger, introducing stricter requirements to the bootstrap capacitor. The table 23 shows potential candidates for the bootstrap diode, and their main attributes and the system characteristic, found in the literature.

Alternatively to the Bootstrap mechanism, as mentioned previously, an isolated DC-DC converter is employed to supply the floating gate power. In the most conventional way, a discrete transformer-based flyback or half-bridge converter fulfills a flexible power requirement as well as CMRR, depending on the transformer design. However, given the low total gate charge $Q_{GD.tot}$, associated with most of the GaN devices, a smaller solution can be utilized. Several FCML converter applications [Ye e Pilawa-Podgurski 2016, Stokowski et al. 2023] utilize *Analog Devices*'s Power Isolator, which combines a Digital Isolator and an Isolated Power Supply. Due

Table 23 – Bootstrap Architecture and Component Selection for FCML converter found in the literature.

Reference	Component	Bootstrap Type	System-level Specification			Component-level Specification
			V_{OUT} (V)	I_{OUT} (A)	f_{SW} (kHz)	C_J (nF)
[Ye et al. 2017]	40V Schottky	Cascaded	12	40	121	6
[Lorenz e Sanchez 2024]	100V Schottky	Cascaded	400	7.50	100	6
[Ye et al. 2022]	40V Schottky	Cascaded	6	40	75	6

to the lower demand of GaN devices, the integrated on-chip power supply can be shrunk and fit in a small package IC. The Power Isolator is followed by a single-channel non-isolated Gate Driver, which often features a very small size. The Table 24 shows the utilized Isolators and Gate Drivers found in the literature review.

Table 24 – Digital Isolator and Gate Driver Architecture and Component Selection for FCML converter found in the literature.

Reference	GaN Device		Gate Driver Architecture			
	Description	Q_{GD} (nC)	Digital	Power		GD
				V_{DRV} (V)	P_{DRV} (mW)	
[Stokowski et al. 2023]	EPC 2034C 200V 6mΩ	11.10	ADuM5241	5	50	LM5114
[Ye e Pilawa-Podgurski 2016]	EPC 2016C 100V 16mΩ	3.40	ADuM5210	5	150	LM5113
[Lei et al. 2016]	EPC 2033 150V 7mΩ	12	ADuM5210	5	150	LM5113
[Brooks et al. 2022]	EPC 2018 100V 3.20m Ω	12	ADuM5240	5	50	LMG1020
[Li et al. 2017]	EPC 2023 30V 1.45m Ω	19	ADuM6200	5	400	LM5113
[Modeer et al. 2020]	EPC 2034 200V 7m Ω	8.80	ADuM5210	5	150	LM5114

Based on the Power Isolator architecture, the main limitation becomes the maximum rail-to-rail drive voltage. Due to the low ON-threshold gate voltage level, it is often advisable to turn-OFF under a negative voltage condition to ensure the GaN device does not false turn-ON due to cross-talking.

Allegro's AHV85110 gate driver solution introduces a power-thru mechanism which includes both the power isolator and the gate driver output stage. It covers sufficient rail-to-rail voltage to support negative turn-OFF drive voltage whilst supporting frequencies up to 800MHz with sufficient head-room as per the datasheet specification. Differently from the *Analog Devices*' power isolators, the AHV85110 utilizes the PWM line to supply the power to the secondary side. As a consequence, the output voltage regulation becomes dependent on the switching frequency.

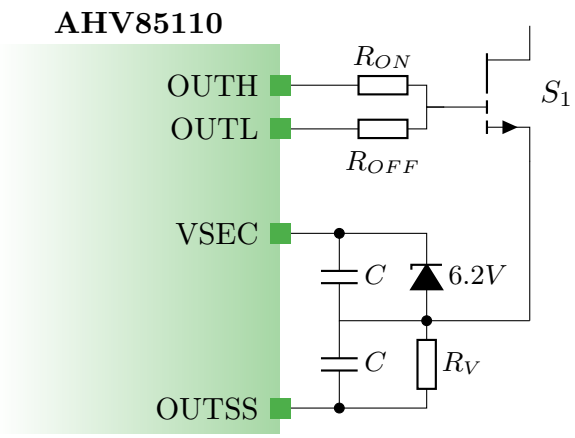
Depending on the total gate charge, there may have conditions where the turn-OFF drive voltage is sufficient low, bringing a lack of flexibility to the system-level design. By comparing different attributes, amongst different solutions, as shown in Table 25, the AHV85110 has an equivalent performance in the propagation delay and superior performance in the CMRR.

Table 25 – Gate Driver Performance Attribute Comparison List Amongst different solutions.

Gate Driver Solution		**Performance Attributes**	
# 1	**# 2**	**Propagation Delay** (ns)	C_{IO} (pF)
AHV85110 (Allegro)		50	$\leq$1
ADuM5210 (Analog Devices)	LM5113 (TI)	23 + 26.50	2.20
ADuM5210 (Analog Devices)	LM5114 (TI)	23 + 12	2.20
ADuM5210 (Analog Devices)	LMG1020 (TI)	23 + 2.50	2.20
ADuM5210 (Analog Devices)	UCC44273 (TI)	23 + 13	2.20
ADuM5210 (Analog Devices)	UCC27611 (TI)	23 + 14	2.20

Therefore, the *Allegro*'s gate driver AHV85110 is chosen as the gate driver IC for the prototype design and validation. In order to comply with the bipolar drive voltage, a zener-based architecture is utilized to shift the ground reference for the driving mechanism, as shown in Figure 70.

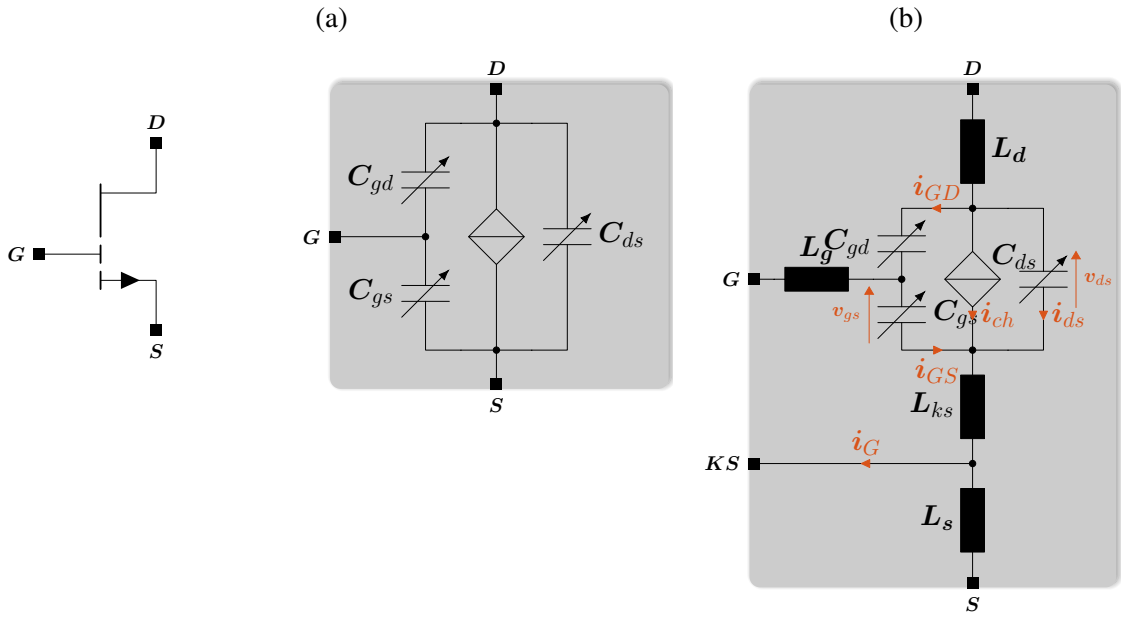
Figure 70 – System-level Implementation of AHV85110 Bipolar Drive Supply for GaN Systems' GS-065-018-2-L.



5.0.7 PCB Design

The Schematic & PCB layout design are done using *Altium*. As mentioned previously, a higher switching-frequency and higher power density can be achieved by introducing GaN switches into the concept. Since the higher switching frequency is achieved by having a very low switching losses, it is translated into the ability of the device to switch faster and, as a consequence, very steep switching transients.

Figure 71 – GaN Device Model Representation for:
(a) Level 1 - Including the non-linear transconductance and intrinsic capacitances.
(b) Level 2 - Including the Parasitic elements associated with packaging.

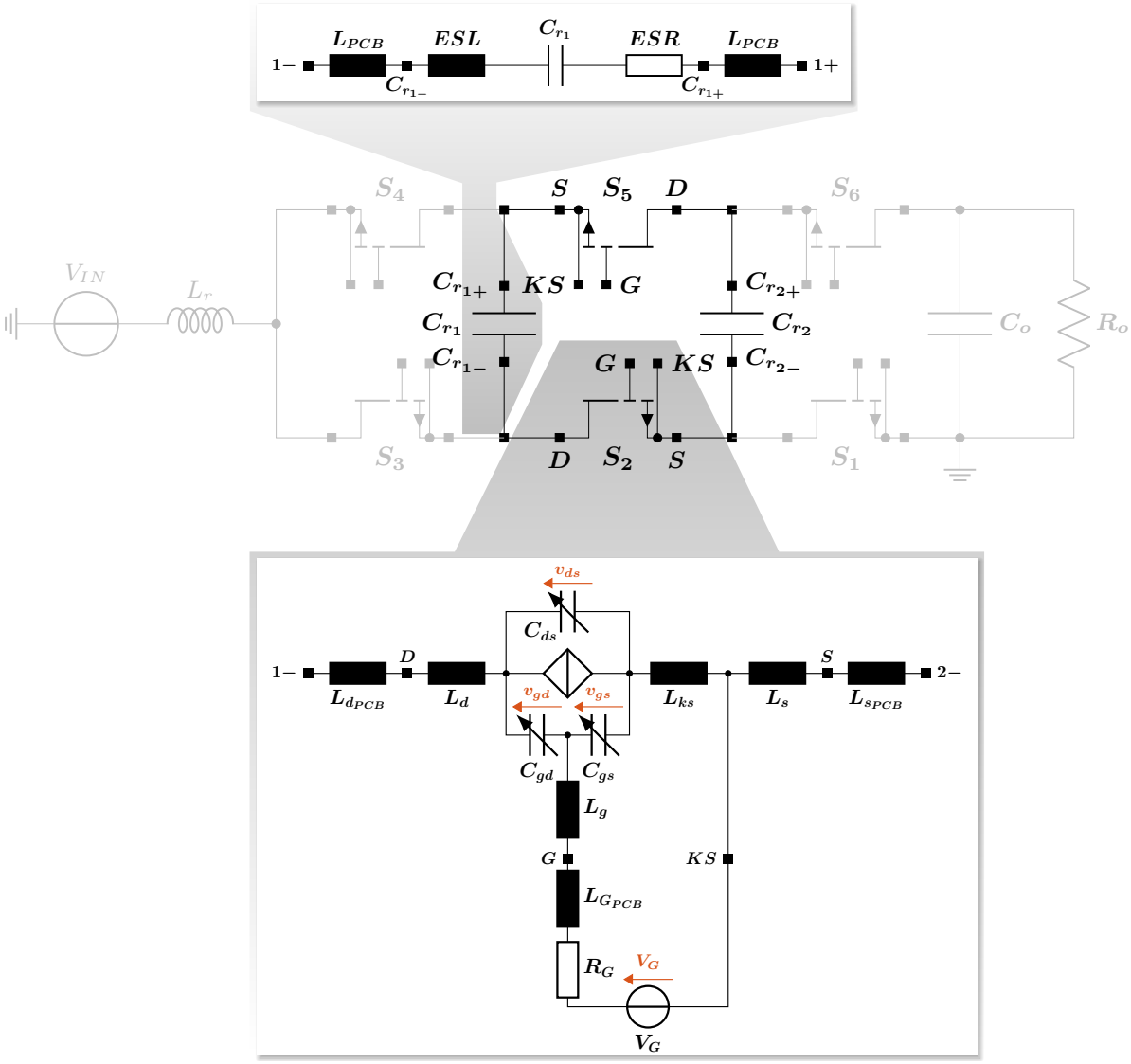


The switching transient depends on the devices' intrisic characteristics, where its current switching transient depends primarily on the transconductance behavior, in which a voltage-controlled current-source drives the device's channel's current i_{ch}. Secondly, its voltage switching transient depends primarily on the non-linear voltage-dependent intrisic capacitances C_{oss}, C_{rss} and C_{iss}. A general representation of a GaN Device is shown in Figure 71a.

Several past work have been focusing on how to describe precisely the switching transients, mainly employing a Half-Bridge configuration with a sufficiently inductive current load [Hu e Biela 2022] [Hofstetter, Maier e Bakran 2019] [Christen e Biela 2019] [Hu e Biela 2023] [Dong et al. 2020]. The major objective is on how to maximize the accuracy of the switching losses' estimation as a necessary step into very-high power density converter design. As an intermediate step, the switching transients are calculated, under three different methods: (1) Full Analytical, (2) Semi-Analytical and (3) Numerical [Hu e Biela 2022]. Within each of the works, the great effort is on the identification of what set of assumptions and simplifications and what set of data shall be done in order to minimize the estimation error. A higher complexity tends to require a numerical solution, yielding the highest accuracy, but compromising the processing time. Nevertheless, every recent work has described which parameters can influence the switching transients; thus, altering the switching performance.

Based on that, the Device model representation can be more complex, as exemplified in Figure 71b. Moreover, the switching performance depends on how the system-level affects the GaN devices' switching behavior. Since the GaN device is considered as an element into the system-level description, where in the present work, the 4L-RFLCC, is composed by three main FLCCC, the system-level is brokendown as shown in Figure 72.

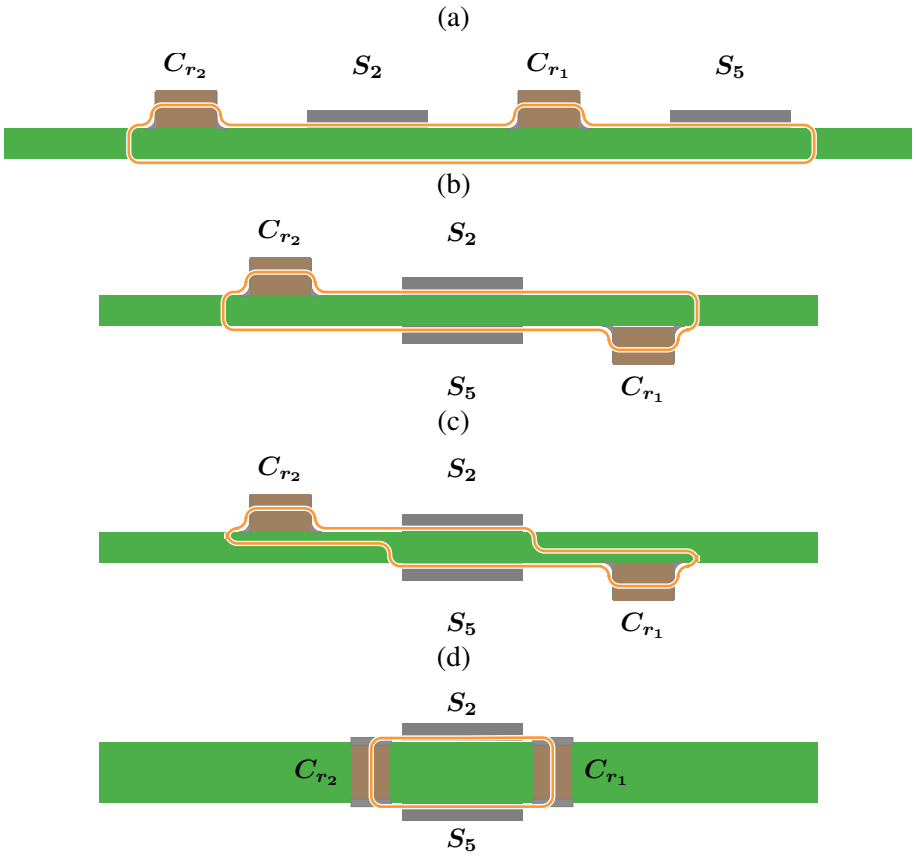
Figure 72 – System-Level Description Model including Parasitic Elements in a single Flying Capacitor Commutation Cell (FLCCC).



In order to address the parasitic elements, and minimize its impact on the switching transient, recent works [Cittanti et al. 2022], [Horowitz e Pilawa-Podgurski 2022], [Pallo, Modeer e Pilawa-Podgurski 2017] have explored the vertical commutation loop, which tends to cancel the magnetic field generated by the two adjacent planes; thus, reducing the mutual inductance. The objective is achieving a tight magnetic coupling between complementary devices [Pallo, Modeer e Pilawa-Podgurski 2017] while securing the isolation coordination. A high-voltage systems possesses challenges in order to achieve the tight magnetic coupling due to the limitation in the prepreg material as its thickness and/or dielectric withstand have risks to safety; thus, increasing the mutual inductance.

Single-sided [Cittanti et al. 2022] approach is explored with a string-connection of Switches and Capacitors with the adjacent layer being the return path, as represented in Figure 73a, whereas Double-sided approach [Horowitz e Pilawa-Podgurski 2022] [Pallo, Modeer e

Figure 73 – Flying Capacitor Commutation Cell (FLCC) PCB Vertical Commutation loop concept:
(a) Single-sided.
(b) Double-sided with Mechanically-thin concept.
(c) Double-sided with Electrically-thin concept.
(d) Double-sided with Embedded Passive Components concept.



Pilawa-Podgurski 2017] is also explored with an enhancement in terms of cooling and area utilization. The Double-sided approach introduces concepts of "electrically-thin" and "mechanically-thin" [Pallo, Modeer e Pilawa-Podgurski 2017], where the "electrically-thin" concept, as shown in Figure 73c attempts to tighten the magnetic coupling between adjacent sides of the board which lacks in the mechanically-thin approach, as represented in Figure 73b. The doubled-sided approach has also been explored with the possibility of multiple-branches [Modeer et al. 2017], which would effectively reduce the PCB stray inductance. Ultimately, [Stokowski et al. 2023] introduced a concept with embedded passive components in order to further increase the magnetic coupling's tightness, as observed in Figure 73d.

In order to explore double-sided components and attempt to shrink the area utilization, the Double-sided Electrically-think concept has been utilized for the proposed 4L-RFLCC prototype PCB design. Figure 74 and Figure 75 exhibits the final PCB design's Top and Bottom Layer 2D view and 3D view, respectively.

Figure 74 – 4L-RFLCC Prototype PCB Design:
(a) Top Layer.
(b) Bottom Layer.

(a) (b)

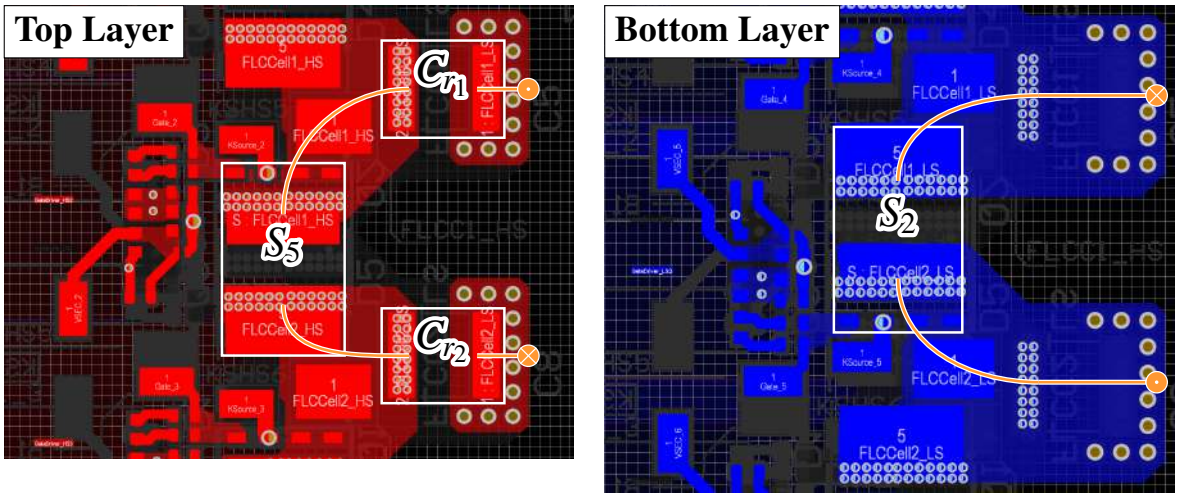
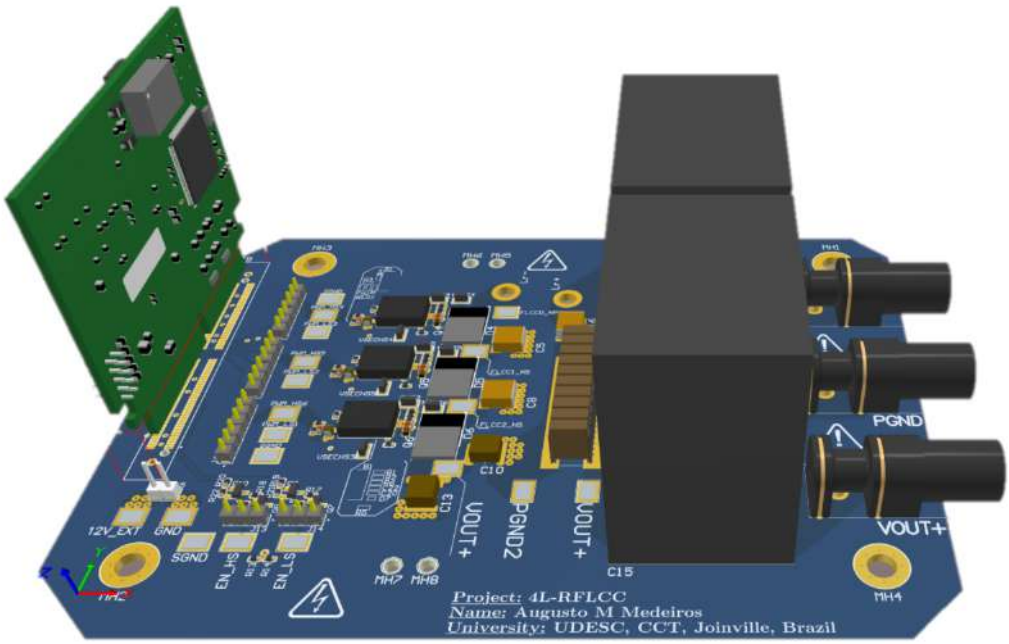


Figure 75 – Prototype Board Altium 3D view.



6 EXPERIMENTAL RESULTS AND VALIDATION

This chapter aims to describe the experimental results and 4L-RFLCC validation according to the theoretical analysis based on the prototype design's specifications shown in the previous Chapters. Figure 76 shows the experimental setup, whereas Figure 77 shows the assembled prototype board utilized to validate the project.

Figure 76 – Experimental Testing Setup for 4L-RFLCC validation.

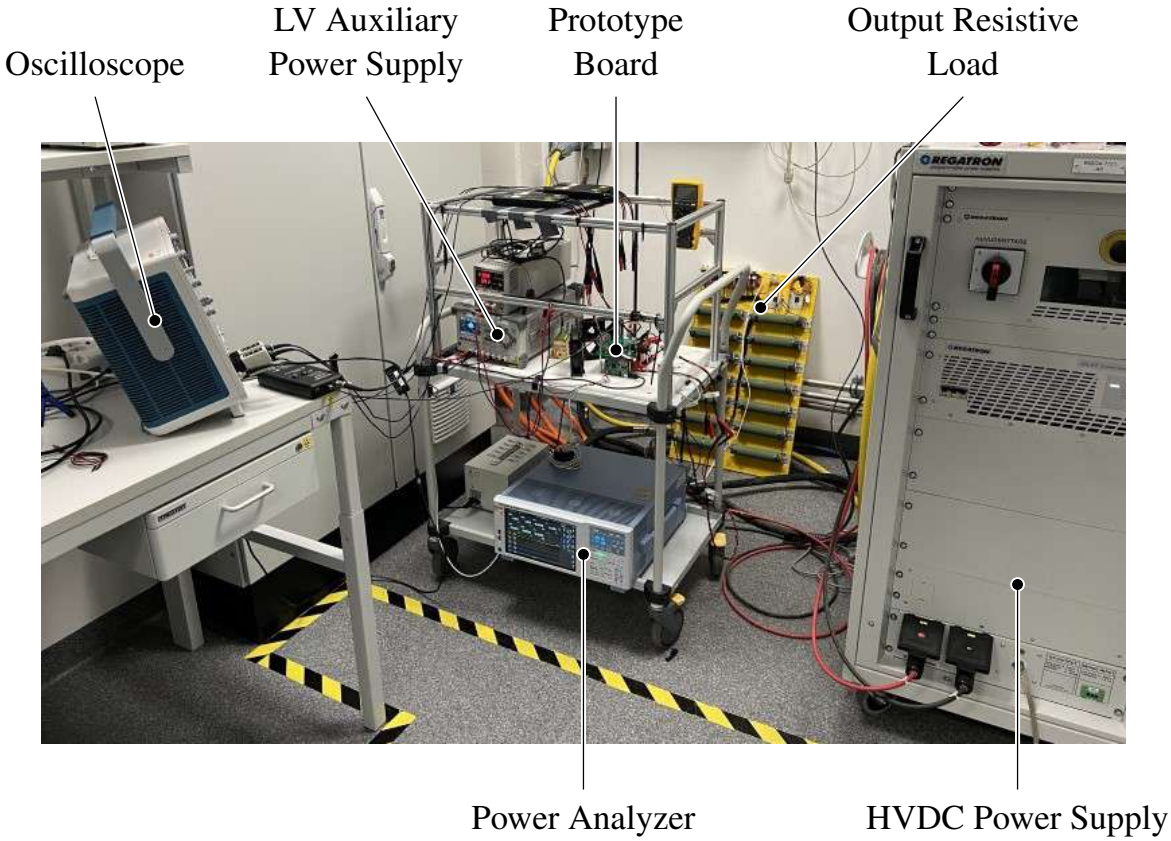


Table 26 consists of the list of instruments utilized during the prototype testing campaign.

6.0.1 Operating Region & Output Voltage Regulation

This section aims to present the different operating conditions expected based on the Theoretical Analysis and operating regions given a set of output resistive load [321.4Ω, 346.08Ω, 520.94Ω, 1017Ω different switching frequency conditions and PWM sequence. Figure 78 shows the different operating conditions explored during the validation process, classified by the output resistive load condition, whereas the oscilloscope's channels' scale is set as following, otherwise specified.

1. V_{OUT} - 50 Volts/Div.
2. V_{IN} - 50 Volts/Div.
3. $v_{C_{r1}}$ - 50 Volts/Div.

Figure 77 – Prototype Board for 4L-RFLCC validation.

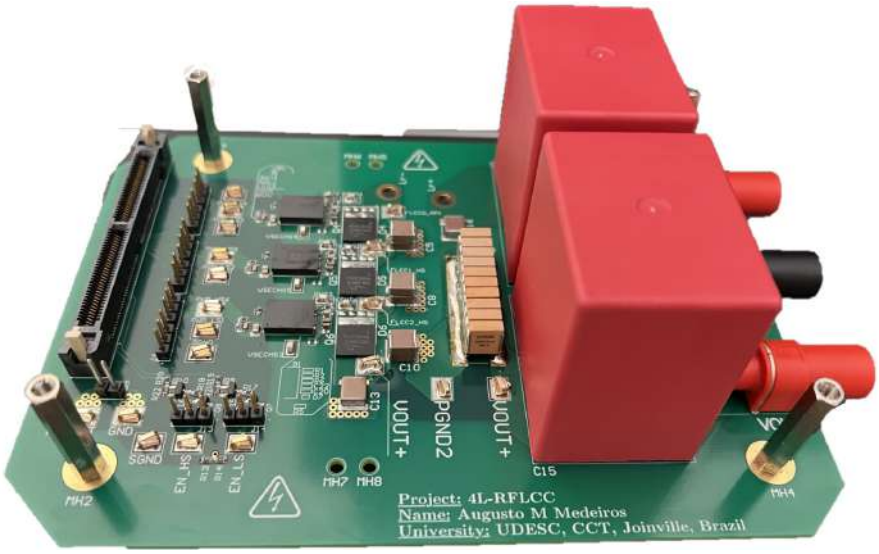


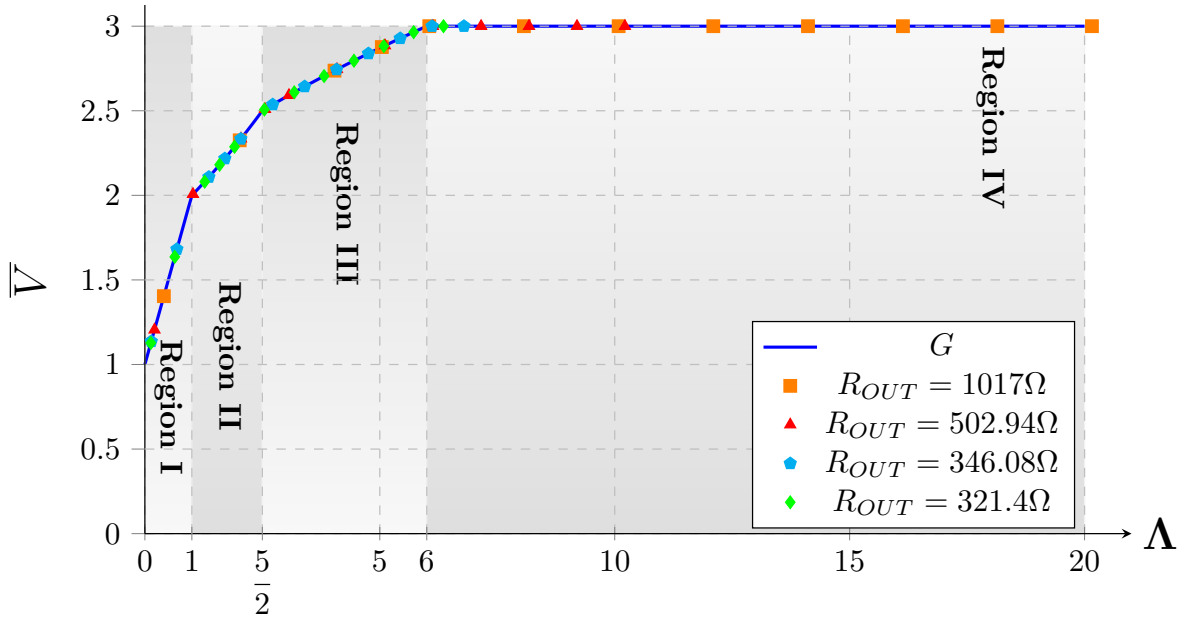
Table 26 – List of Instruments for prototype testing.

Description	Model	Supplier	Purpose
6GHz 6-channel Oscilloscope	MSO66B	Tektronix	Acquisition of measurement signal and storage of data
IsoVu 1GHz Isolated Voltage Probe	TIVP1	Tektronix	Measurement of floating high-frequency and fast transient dynamics components' voltage
HV 200MHz Differential Voltage Probe	THDP0200	Tektronix	Measurement of DC and high-frequency components' voltage
IsoVu 200MHz Isolated Voltage Probe	TIVP02	Tektronix	Measurement of floating high-frequency and fast transient dynamics components' voltage
1GHz 300V Passive Voltage Probe	TPP1000	Tektronix	Measurement of high-frequency and fast transient dynamics components' voltage
Rogowski Current Probe	TRCP0600	Tektronix	Measurement of high-frequency resonant current
Power Analyzer	WT5000	Yokogawa	Measurement of static variables for voltage regulation and efficiency
LV Power Supply	DP832A	Rigol	Supply the auxiliary low-voltage to the gate driver and cooling Fans
HVDC Power Supply	G5.18.1000.54	Regatron	Supply the Input Voltage to the power converter
DSP DaughterBoard	TMDSCNCD-280039C	TI	Control and PWM generation to the power converter

4. $v_{C_{r2}}$ - 50 Volts/Div.

5. v_{DS} - 50 Volts/Div.

Figure 78 – Experimental Test Condition Points utilized during the 4L-RFLCC prototype validation.



6. v_{GS} - 5 Volts/Div.

7. i_{L_r} - 5 Amps/Div.

Figure 79 shows the resonant state variables under the same testing conditions and different PWM sequence. The Active Switches $S_1 - S_3$ transition events are highlighted by the notation **1x** to **3x** in which **x** refers to the PWM sequence type. The Table 27 show the test condition sets under evaluation within the 6.0.1

Figure 79a validates the expected results from the theoretical and simulation environment for the 4L-RFLCC operating under Test Condition 1 corresponding to Operating Region I, whereas Figure 79b corresponds to the Test Condition 2. The major difference is observed in the charge pump / ladder charge orientation in which the charge orientation's couplings are upwards and downwards, respectively.

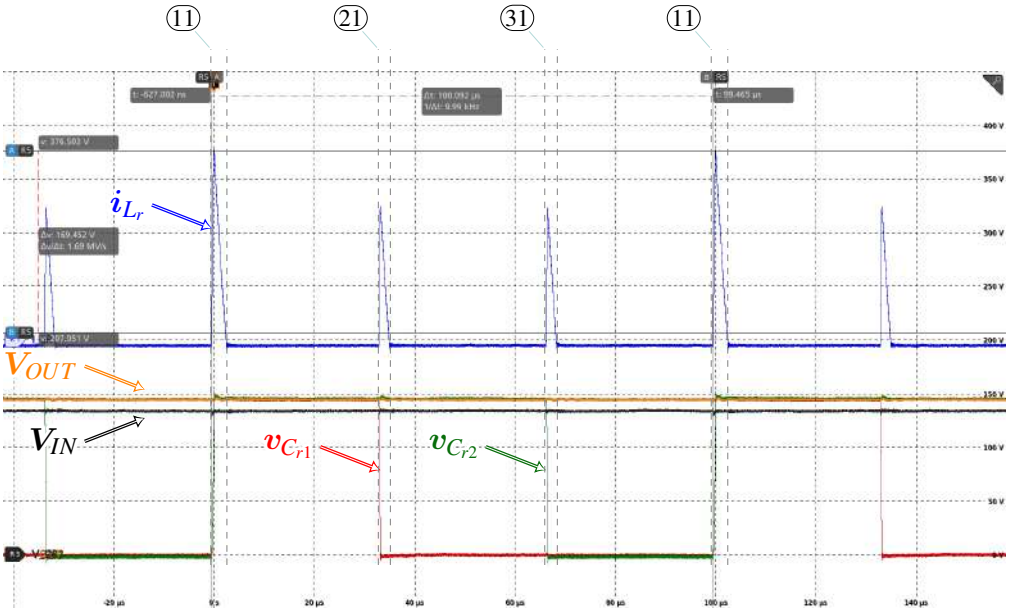
At **11**, due to the resonant state variables' initial condition, resonant capacitors' C_{r_1} and C_{r_2} start to charge up to V_{OUT} simultaneously, as shown in Figure 80. At the end of ΔT_{10I}, the resonant capacitors' voltages are clamped to V_{OUT}, and is followed by a small High-Frequency oscillation due to the capacitors' current discontinuity. The following topological stage also validates with the theoretical assessment where the resonant inductor's current decreases linearly.

At **21** and **31**, given the resonant state variables' initial conditions, the resonant capacitors' C_{r_1} and C_{r_2} start to discharge down to 0V upon their transient event trigger, as shown in Figure 81 and 82, respectively. Similarly to the end of the 1st topological stage, there exist a small High-Frequency oscillation due to the capacitors' current discontinuity.

The topological stages, shown in Figure 79b, can be further validated based on the PWM sequence type. At **12**, as shown in Figure 83, given the resonant state variables' initial conditions,

Figure 79 – Experimental results under:
(a) $R_{OUT} = 321.4\Omega$ and $f_{SW} = 10kHz$ based on Clock-wise PWM Sequence Type.
(b) $R_{OUT} = 321.4\Omega$ and $f_{SW} = 10kHz$ based on Counter Clock-wise PWM Sequence Type.

(a)



(b)

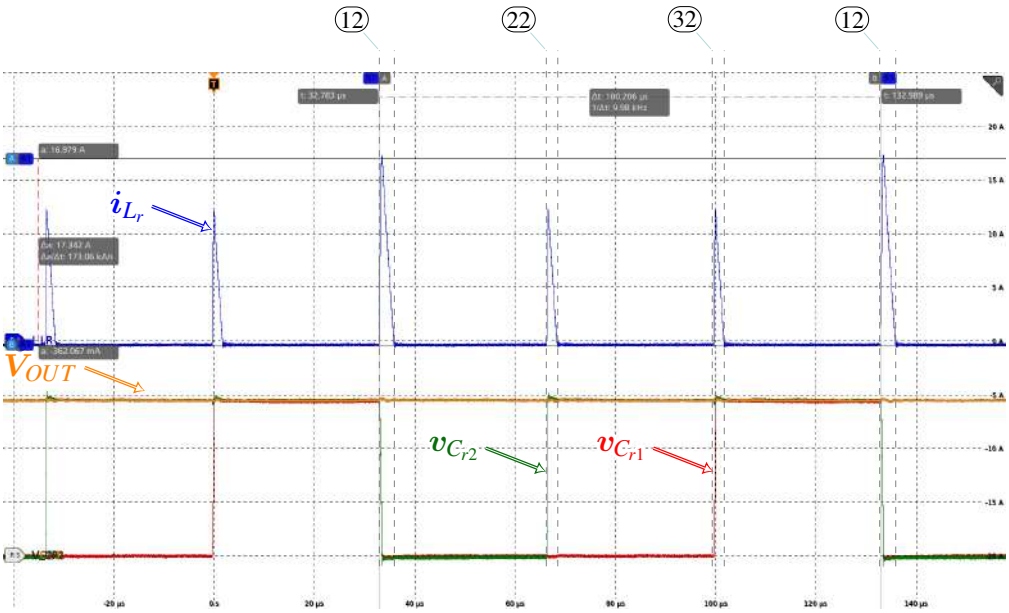
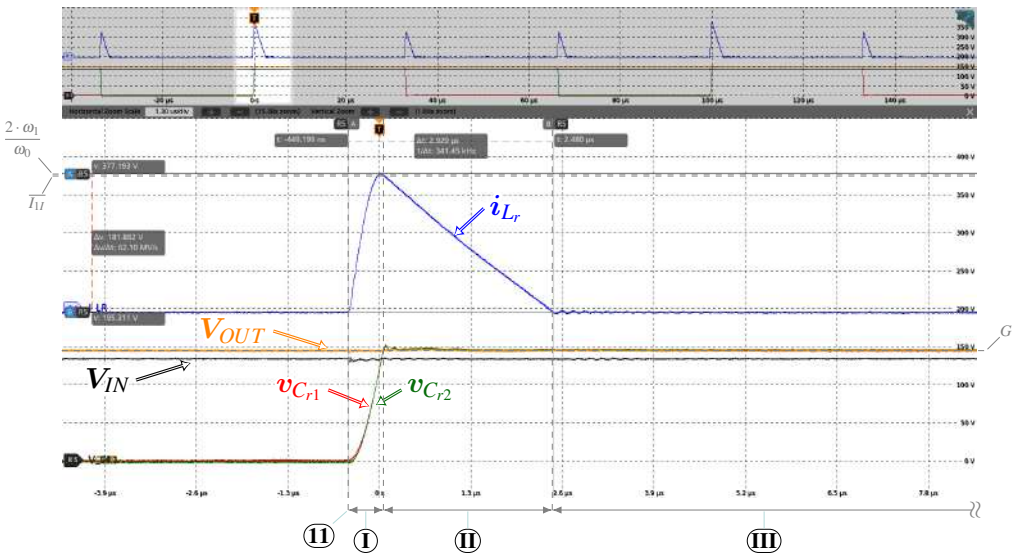


Table 27 – List of Test Condition Sets utilized for the Operating Region and Output Voltage Regulation Validation assessment.

Test Condition Set	Operating Conditions		
	PWM Sequence	f_{SW} $[kHz]$	R_{OUT} $[\Omega]$
①	CW	10	321.4
②	CCW	10	321.4
③	CW	50	321.4
④	CW	150	321.4
⑤	CCW	150	321.4
⑥	CW	300	321.4
⑦	CW	400	321.4
⑧	CW	250	525
⑨	CW	500	301.9
⑩	CW	300	1017
⑪	CW	500	1017
⑫	CW	500	321.4

Figure 80 – 1st to 3rd Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 10kHz$ based on Clock-wise PWM Sequence.



the resonant capacitors' C_{r_1} and C_{r_2} start to discharge down to 0V simultaneously. The process encounters a mirrored state trajectory as compared to the one seen in Figure 80, whereas the linear region, within **IIb**, remains identical to the Clock-wise PWM sequence.

Similarly, at ㉒ and ㉜, due to the resonant state variables' initial condition, resonant capacitors' C_{r_2} and C_{r_1} start to charge up to V_{OUT} upon their transient event trigger, as shown in Figure 84 and 85, respectively.

Figure 81 – 4th to 6th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 10kHz$ based on Clock-wise PWM Sequence.

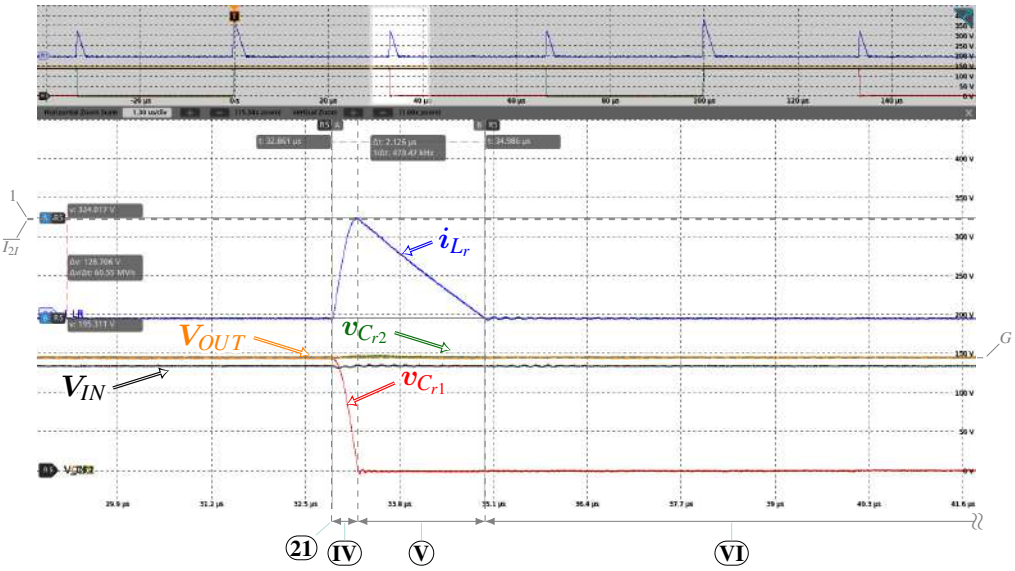


Figure 82 – 7th to 9th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 10kHz$ based on Clock-wise PWM Sequence.

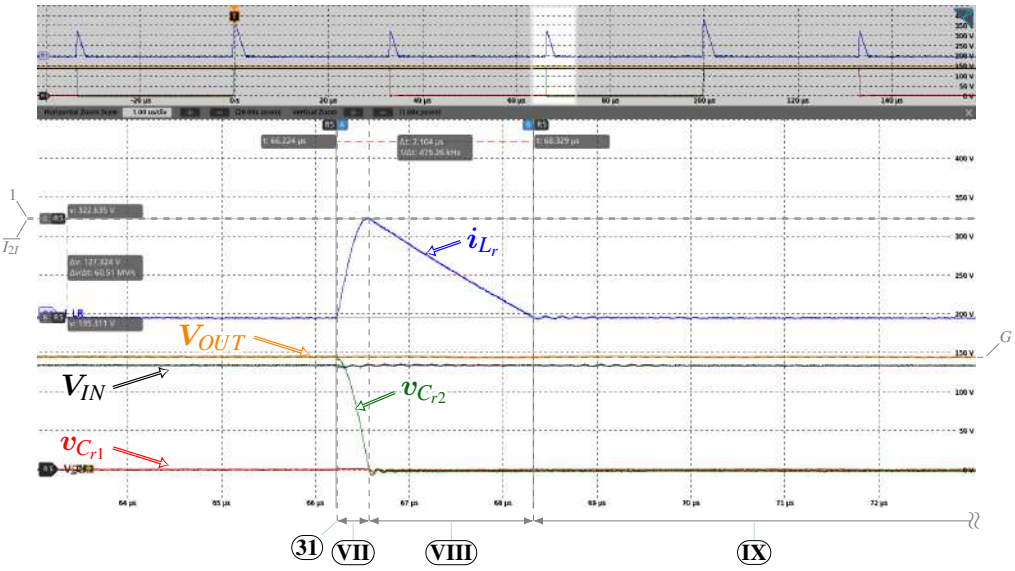


Figure 86 addresses the experimental results for the test condition set 3 under Clock-wise PWM sequence type. It remains operating under the Operating Region I. The major difference being in the ΔT_{xy}, as expected from the theoretical assessment, but also in the increased oscillation in the resonant inductor's current upon a discontinuity during intervals IIIb, VIb and IXb.

Similarly to the test condition set 1, at 21 and 31, C_{r_1} and C_{r_2} discharge to 0V sequentially upon the transient event, as shown in Figure 87 and 88, respectively. These two dynamic changes are followed by a stronger High-frequency Oscillation at the moment which the resonant state variable i_{L_r} becomes zero. The oscillation's excitation is due to the higher step in the disabled Active Switch's voltage at instant t_8.

Based on the theoretical assessment, there exist additional operating regions, where

Figure 83 – 1st to 3rd Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 10kHz$ based on Counter Clock-wise PWM Sequence.

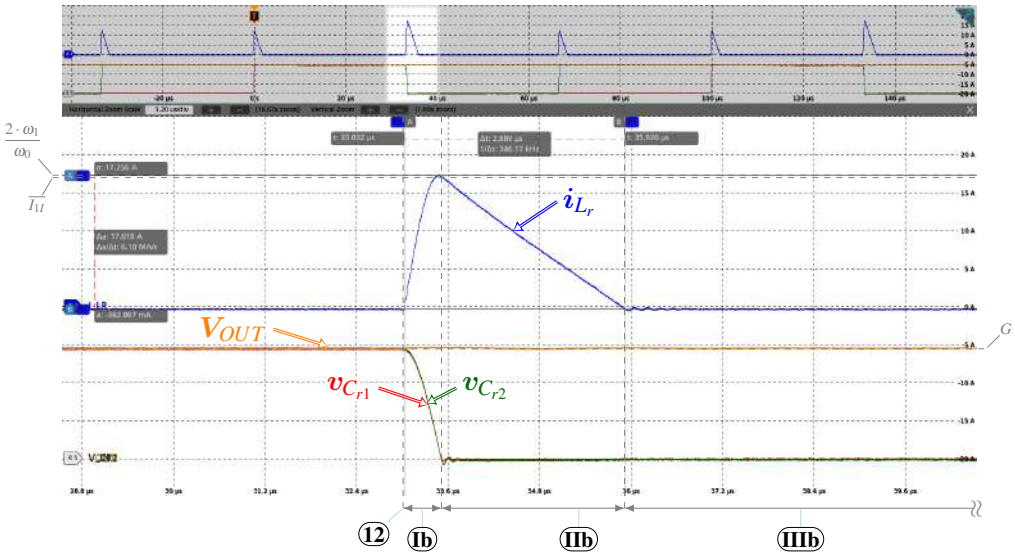
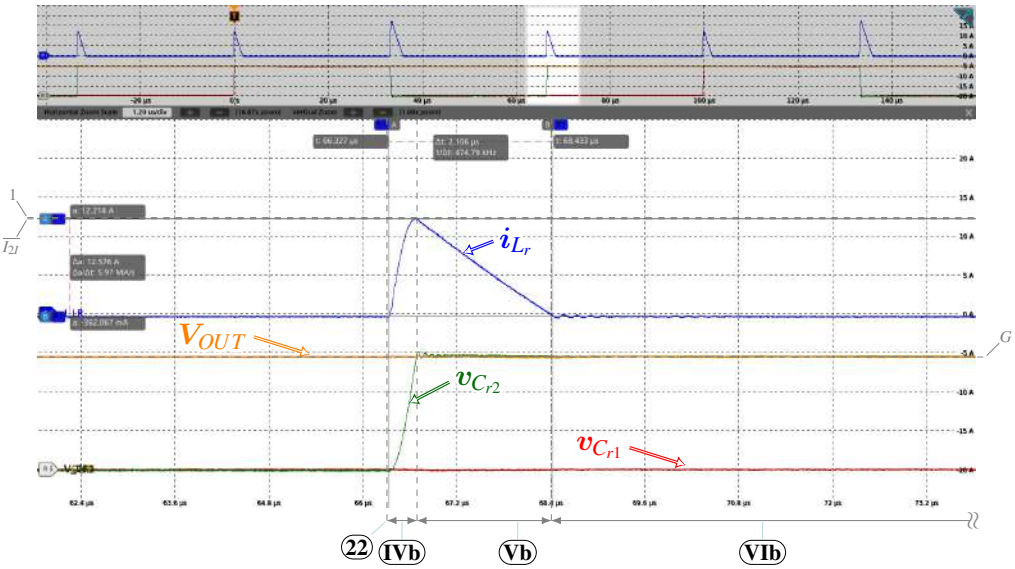


Figure 84 – 4th to 6th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 10kHz$ based on Counter Clock-wise PWM Sequence.



the state variables behave distinctively, by varying the coefficient Λ. Test condition set ④ corresponds to a condition within the Operating Region II and is validated as shown in Figure 89.

As observed in Figure 89, and similar to the test condition set ③, the High-frequency oscillation persists. Due to its small damping factor and the higher switching frequency, the oscillation remains within the entirety of the idle states.

Test condition set ⑤ corresponds to changing the PWM sequence type, under the same Λ condition. By doing so, as observed in Figure 90, the charge pump / ladder mechanism changes its polarity and, most important, the resonant capacitors' state variables mirror within the V_{OUT} and 0V. Therefore, it is noticeable C_{r_2} no longer clamps up to V_{OUT} while C_{r_1} clamps down to

Figure 85 – 7th to 9th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 10kHz$ based on Counter Clock-wise PWM Sequence.

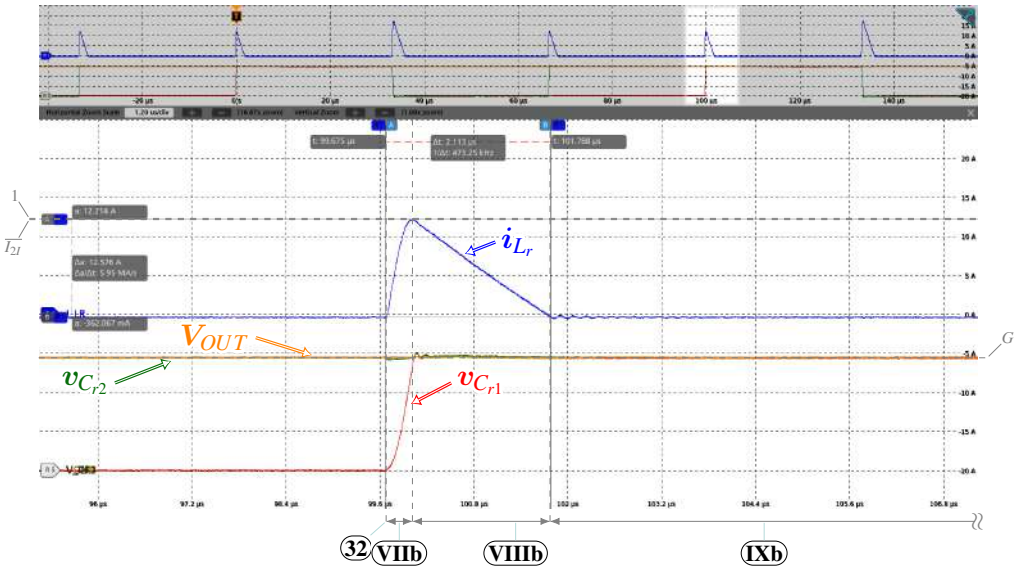
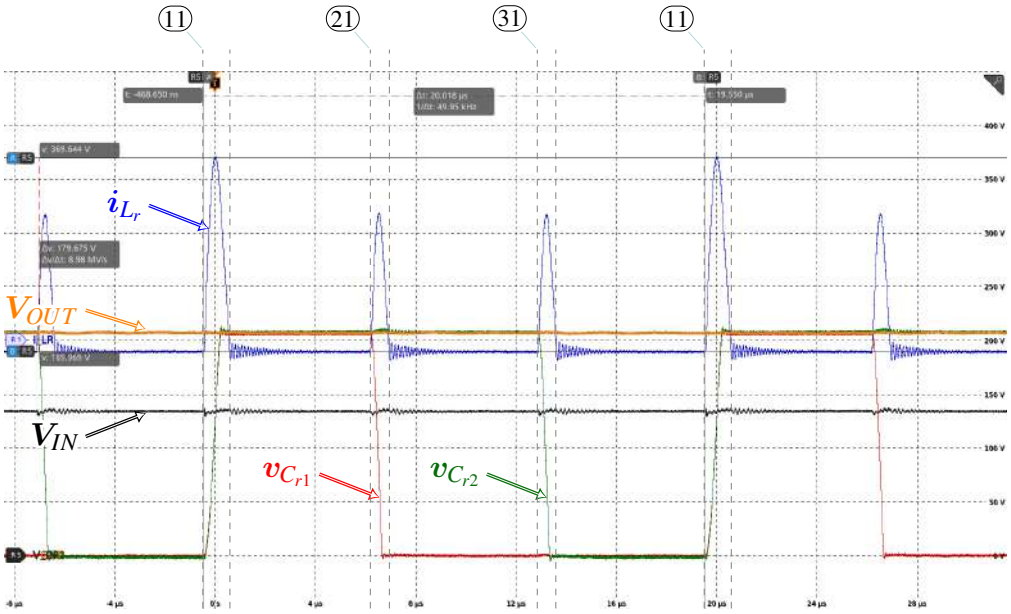


Figure 86 – Experimental results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 50kHz$ based on Clock-wise PWM Sequence Type.



0V.

Table 28 compares the experimental results and relative voltage in reference to the clamping rail, depending on the PWM sequence type, whereas Figure 91 - 96 show the resonant state variables in between two nearest transition events. Despite of a small deviation in ΔV_3, the assumption matches and the 4L-RFLCC behaves in an identical way but mirrored.

By increasing further the coefficient Λ, the 4L-RFLCC is expected to change its operation behaviour as identified in the previous sections. Therefore, test condition set 6 is utilized to validate the behaviour of the 4L-RFLCC under Operating Region III and is shown in Figure 97. The resonant state variables validate with the theoretical assessment which is highlighted due to

Figure 87 – 4th to 6th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 50kHz$ based on Clock-wise PWM Sequence.

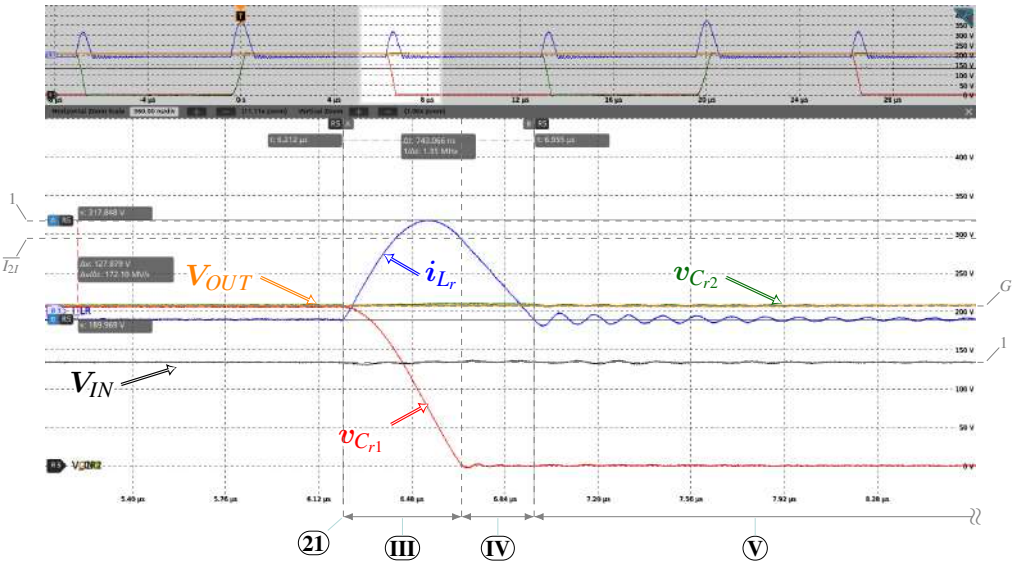
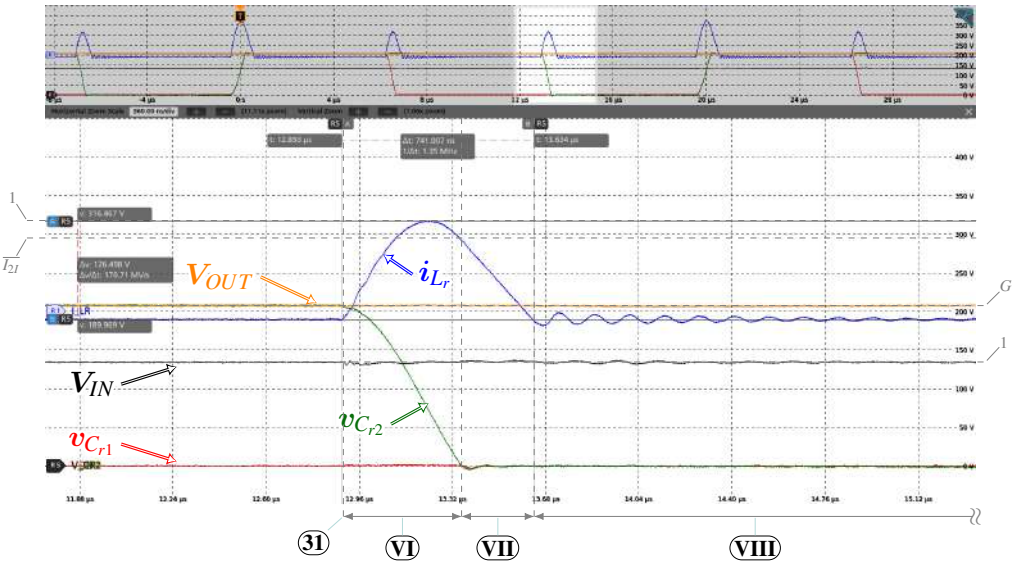


Figure 88 – 7th to 9th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 50kHz$ based on Clock-wise PWM Sequence.



the fact that the state variable $v_{C_{r2}}$ no longer clamps to V_{OUT}.

Similarly as shown previously, Figure 98 - 100 represent the validation results for the 1st to 7th topological stages, according to the theoretical assessment with no visible differences, except the high-frequency oscillatory current during the idle stage within the 3rd, 5th and 7th due to the DCM behaviour. Similar to the previous experimental results, the oscillation intensity also differs amongst the different idle states due to different excitation, which are further described in the 6.0.2.

At 11, as shown in Figure 98, given the resonant states' initial condition, resonant capacitors' C_{r_1} and C_{r_2} voltage are V_{1III} and V_{2III}, respectively. Distinctively from the theoretical assessment, Topological stage 2nd starts when v_{S5} forward-biases under a positive non-zero

Figure 89 – Experimental results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Clock-wise PWM Sequence Type.

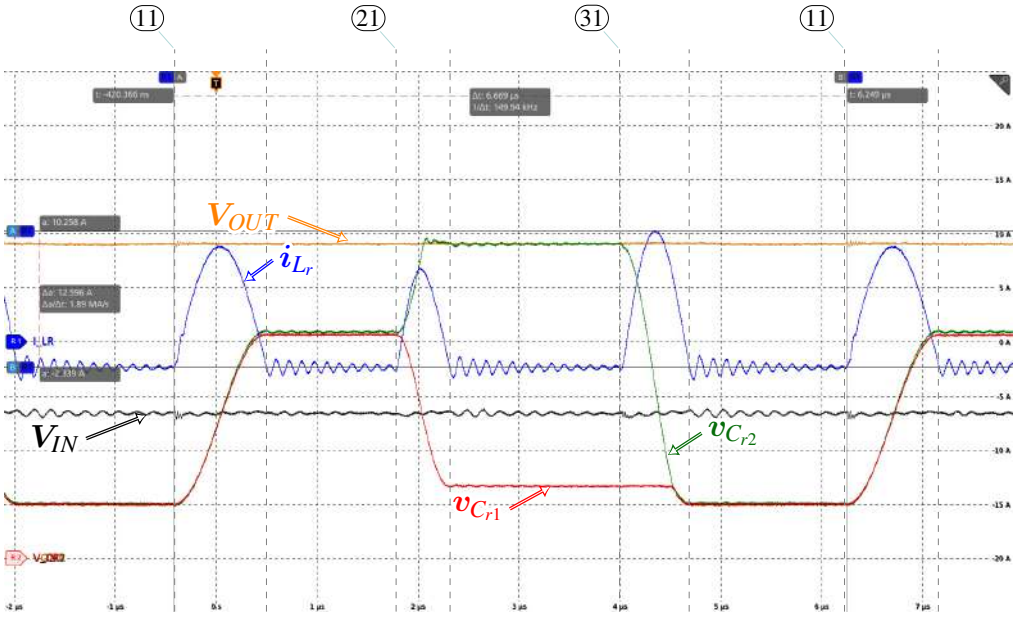
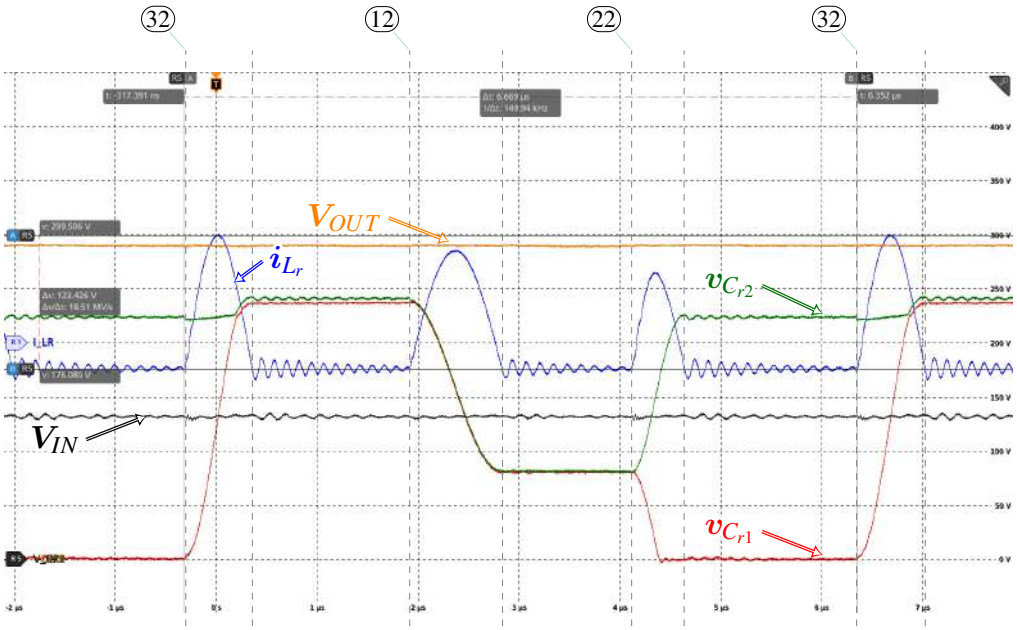


Figure 90 – Experimental results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Counter Clock-wise PWM Sequence Type.



forward voltage condition. Within that interval, both resonant capacitors charge up to V_{3III}. The static resonant variables are shown in Table 29.

At (21), as shown in Figure 99, the resonant capacitor C_{r_1} charge is partially transferred to C_{r_2} under a full resonant semi-cycle. By the end of the interval (III), C_{r_1} and C_{r_2} resonant capacitors' voltage are V_{1III} and V_{4III}, respectively.

At (31), as shown in Figure 100, the C_{r_2} resonant capacitor charge is partially transferred to the output and its final voltage condition, by the end of interval (VI), is V_{2III}.

Based on the theoretical assessment, the static state variables have identical results given

Figure 91 – 1st to 2nd Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Clock-wise PWM Sequence.

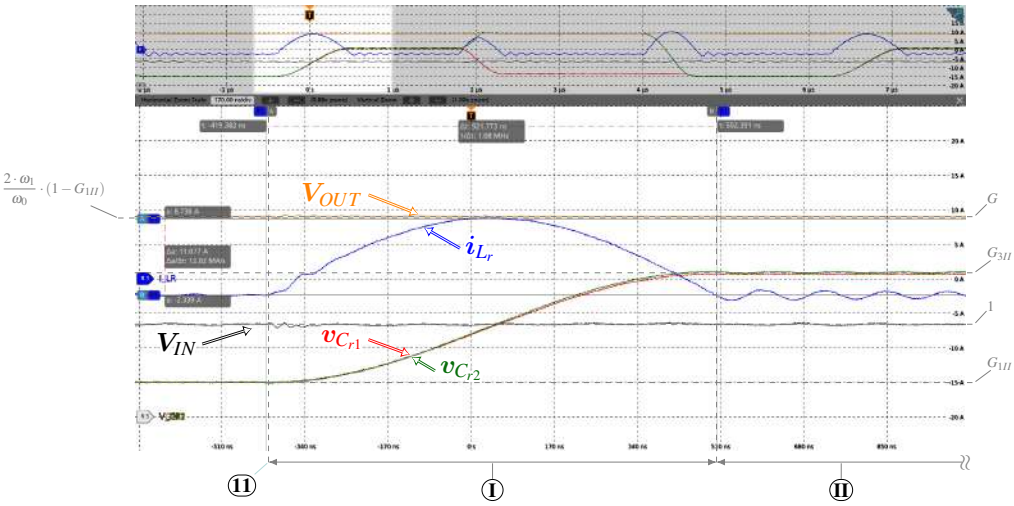


Table 28 – Operating Region II relative voltage comparison in between Counter Clock-wise and Clock-wise PWM Sequence type.

	PWM Sequence	
	CW	CCW
$V_{ref}\,[V]$	GND	V_{OUT}
$V_{OUT}\,[V]$	290.54	289.81
$\Delta V_n = \lvert V_{ref} - V_n \rvert$		
$\Delta V_1\,[V]$	49.34	48.91
$\Delta V_2\,[V]$	66.41	66.15
$\Delta V_3\,[V]$	206.61	209.39

Figure 92 – 3rd to 5th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Clock-wise PWM Sequence.

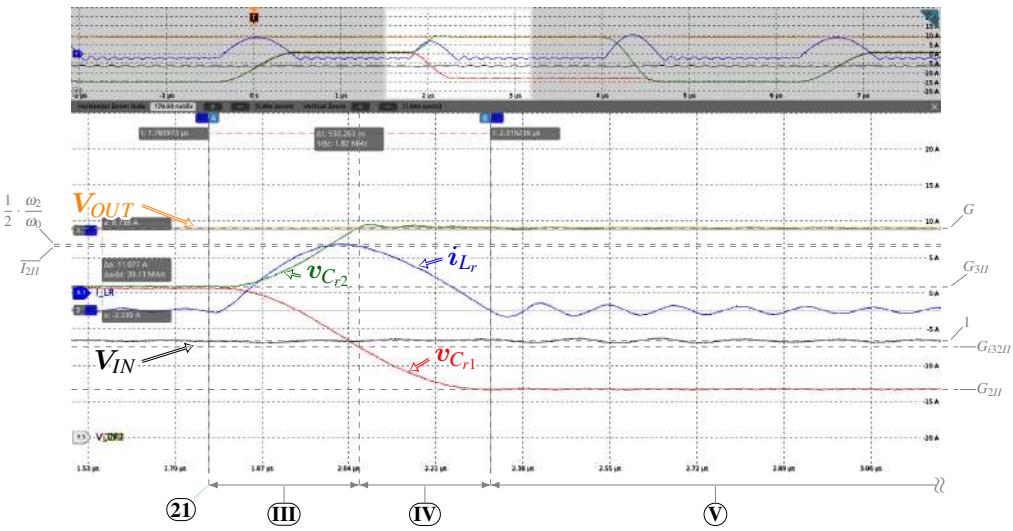


Figure 93 – 6th to 8th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Clock-wise PWM Sequence.

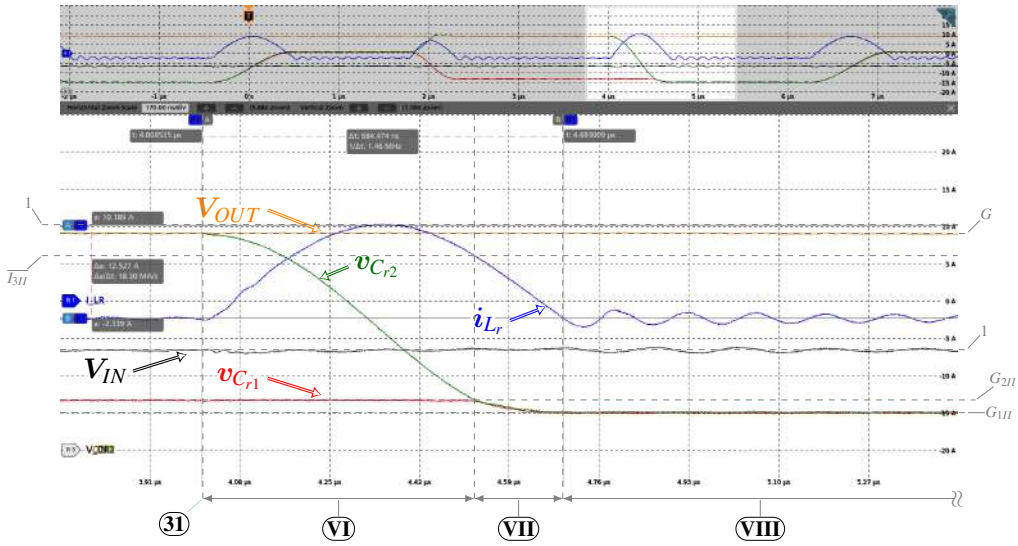


Figure 94 – 1st to 3rd Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Counter Clock-wise PWM Sequence.

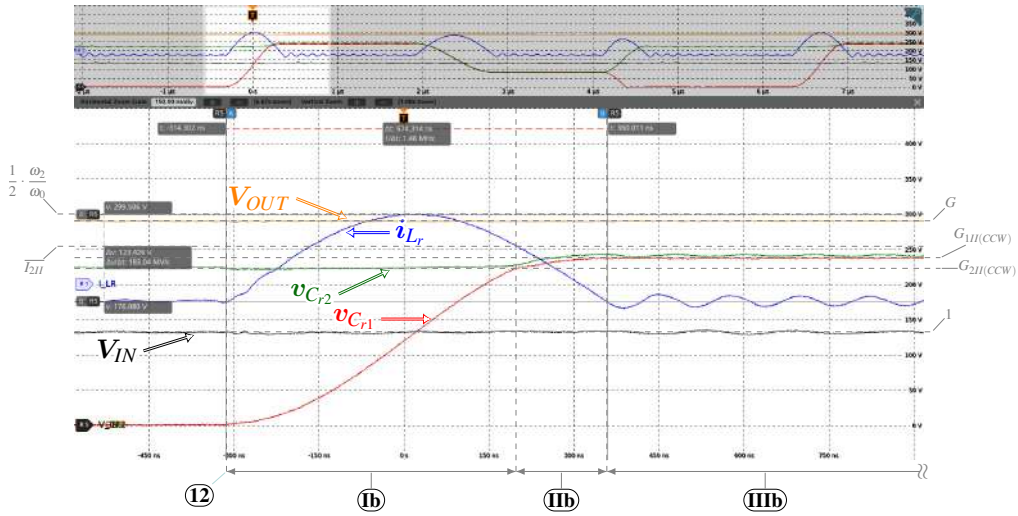


Table 29 – Test Condition set 6 Static Resonant Variables Comparison in between Theoretical and Experimental Results.

	Theoretical [V]	**Experimental [V]**	**Error [%]**
V_{OUT}	346.52	359.99	3.89
V_{1III}	54.70	55.12	0.77
V_{2III}	132.55	123.80	7.07
V_{3III}	188.2	181.36	3.77
V_{4III}	321.28	312.64	2.76

an infinite combination of output load R_{OUT} and switching frequency f_{SW}, which translates into the coefficient Λ above-mentioned in the previous sections.

Figure 95 – 4th to 5th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Counter Clock-wise PWM Sequence.

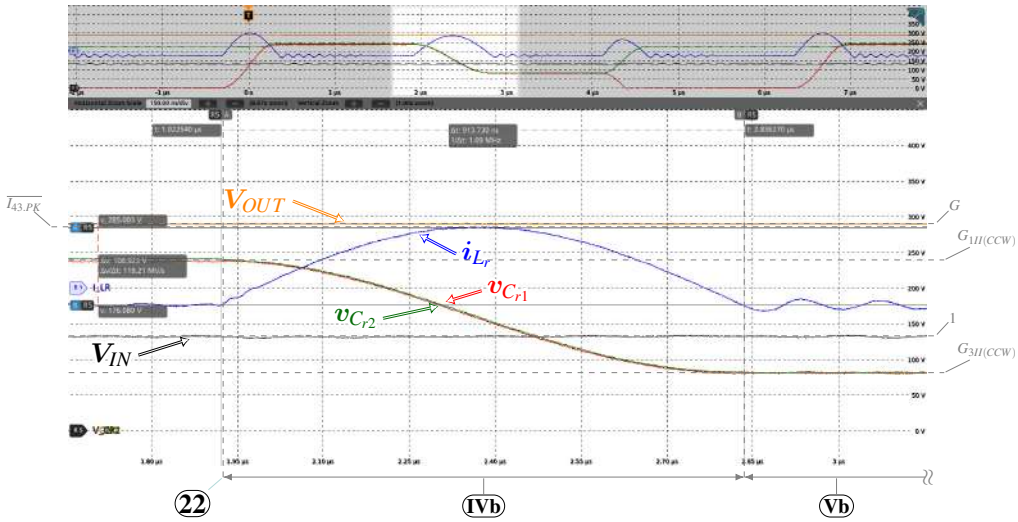
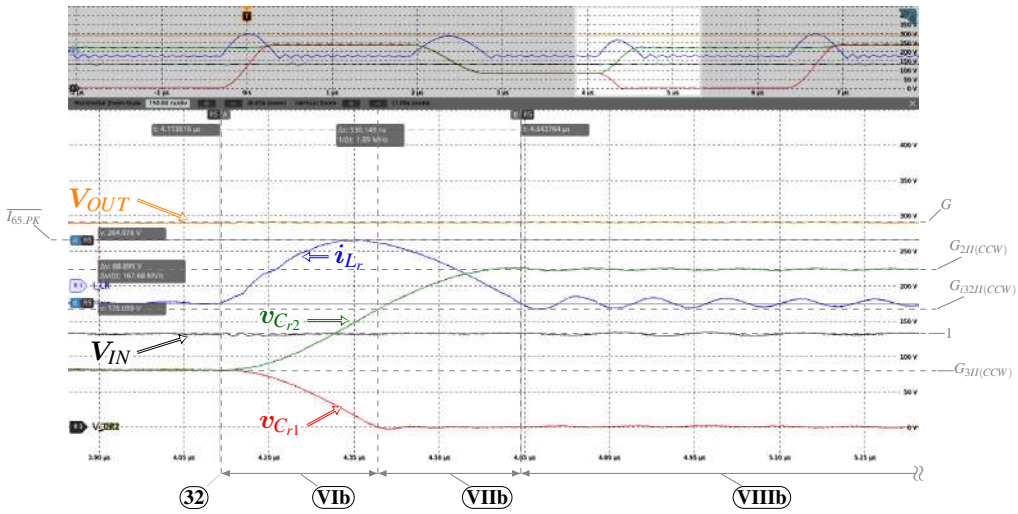


Figure 96 – 6th to 8th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 150kHz$ based on Counter Clock-wise PWM Sequence.



Within Operating Region III, test condition set 7 and 8 meet the statement above. Figure 101a and 101b show the experimental results for the test condition set 7 and 8, respectively. By visual inspection, it is noticeable the static sate variables have similar values whereas the idle states, represented by the Intervals III, V and VII are the major differences.

The static variables are compared and shown in Table 30.

Based on the rated load condition and rated switching frequency, the design, shown in Section 5, shall operate in the boundary between Operating Region III and Region IV at $R_{OUT} = 301.9\Omega$ and $f_{SW} = 500kHz$ with an equivalent $\Lambda = 6$. Due to the limited output load conditions available for testing, the Test Condition 9 corresponds to an equivalent $\Lambda = 6.35$ where the converter is operating under a heavy load condition and requires a high switching frequency in order to maintain the 4L-RFLCC operating at its maximum permissible conversion ratio.

Figure 97 – Experimental results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 300kHz$ based on Clock-wise PWM Sequence Type.

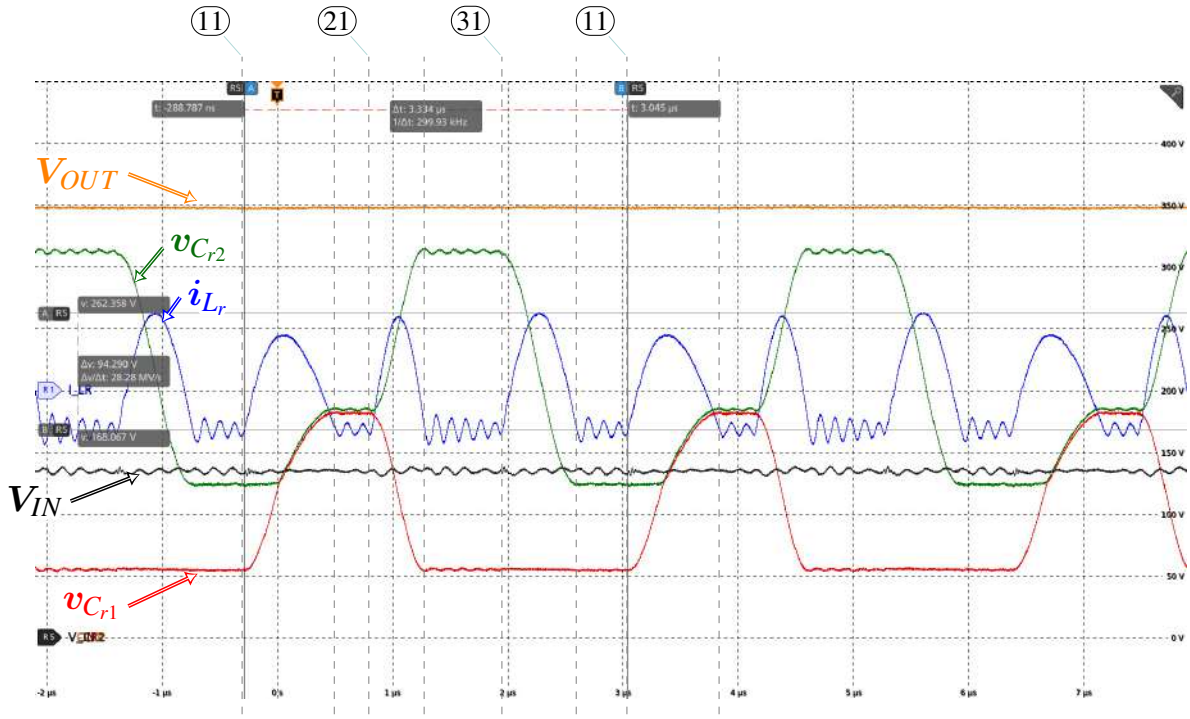


Figure 98 – 1st to 3rd Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 300kHz$ based on Counter Clock-wise PWM Sequence.

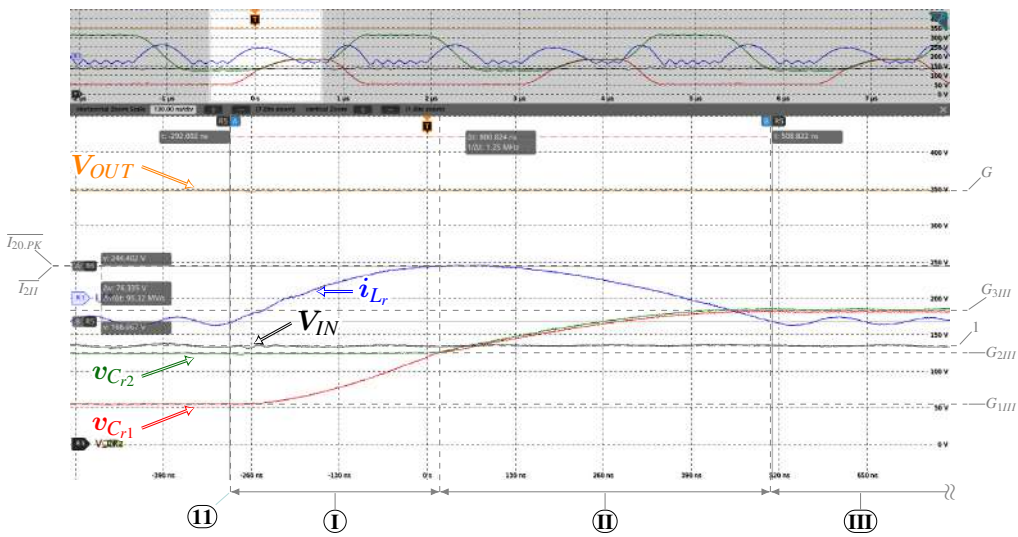


Figure 102 represents the experimental results for the Test Condition 9 in which the resonant state variables are shown. As predicted based on the $\Lambda = 6.35$, the 4L-RFLCC operates within the Operating Region IV but relatively close to the Operating Region III. The complete decoupling in between the resonant capacitors' voltage underlines the 4L-RFLCC operating region. Additionally, it is visible the ZCS condition under the rated switching frequency operation where there exist a synchronization in between the current discontinuity and the Transient Events 11 and 21.

Figure 99 – 4th to 5th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 300kHz$ based on Counter Clock-wise PWM Sequence.

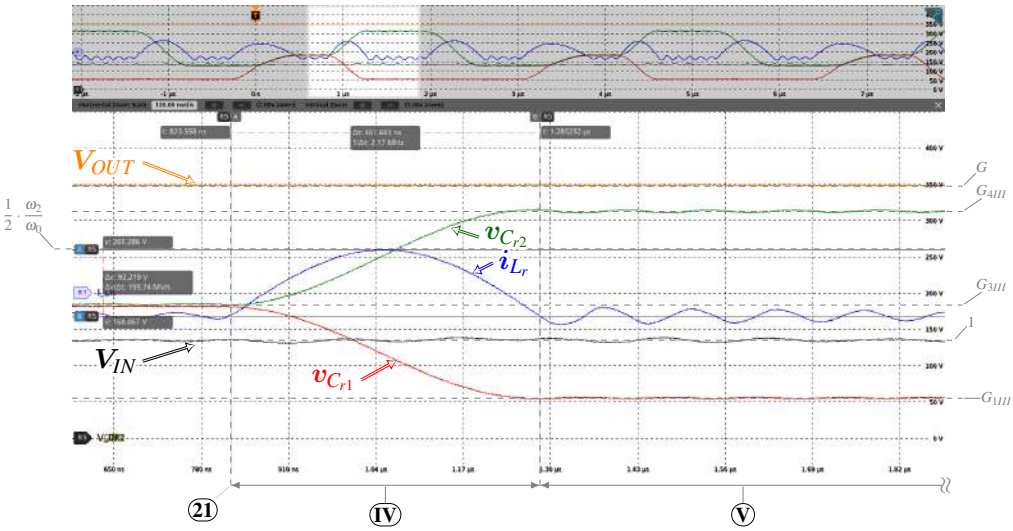


Figure 100 – 6th to 7th Topological Stage validation results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 300kHz$ based on Counter Clock-wise PWM Sequence.

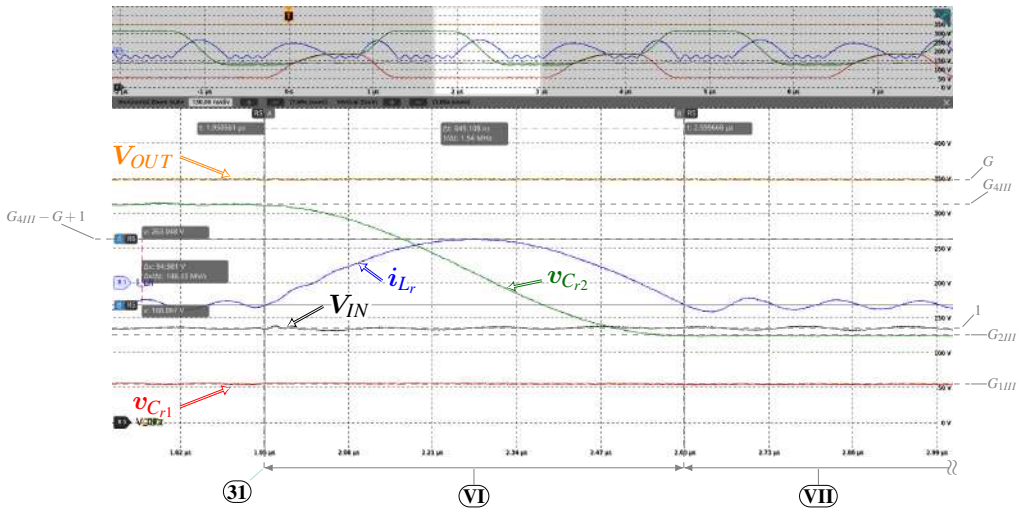
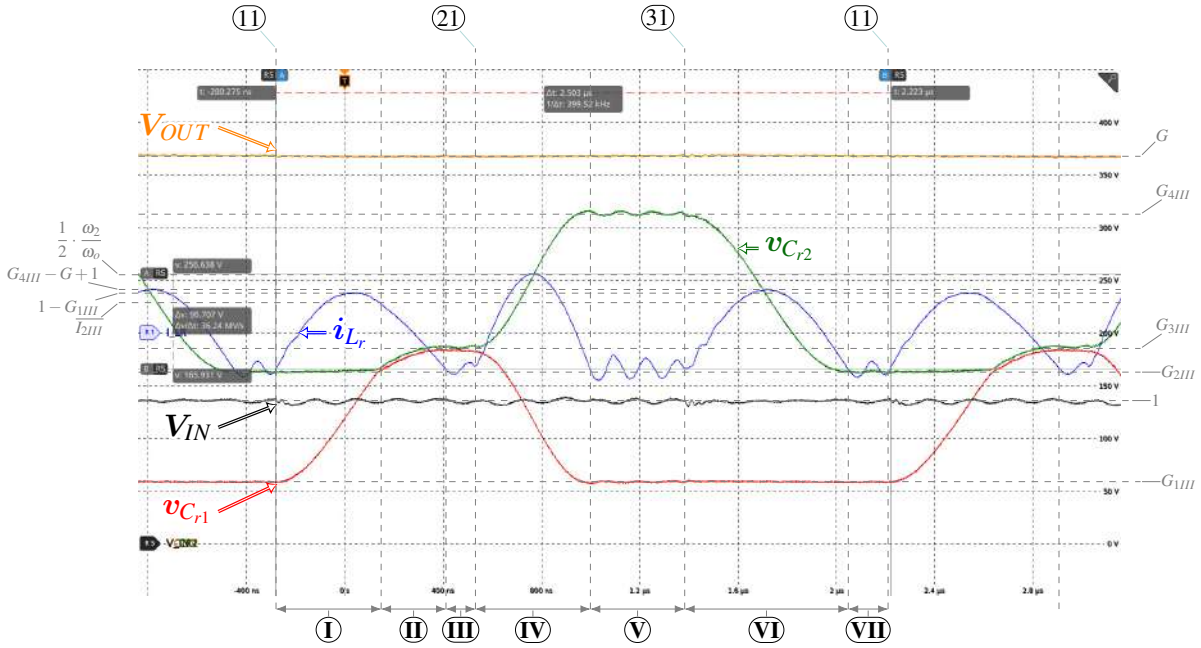


Table 30 – Test Condition set ⑦ and ⑧ Static Resonant Variables Comparison in between Theoretical and Experimental Results under the same Λ condition .

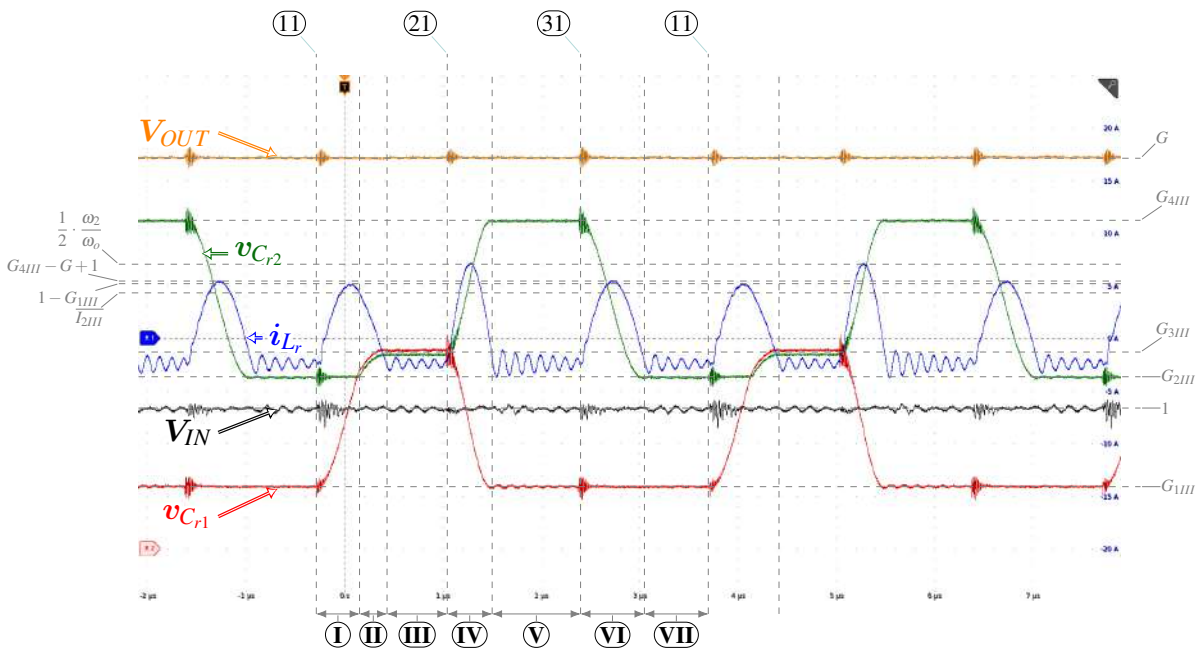
				Large-Signal State Variables				
			Λ	$V_{OUT}\,[V]$	$V_{1III}\,[V]$	$V_{2III}\,[V]$	$V_{3III}\,[V]$	$V_{4III}\,[V]$
Test Condition	⑦	Theoretical	5.09	383.47	59.74	175.03	192.78	325.83
		Experimental		366.62	58.37	163.12	183.22	313.32
		Error [%]		4.56	2.34	7.31	5.22	3.99
	⑧	Theoretical	5.11	384.17	59.93	175.84	193.07	326.22
		Experimental		369.58	58.77	162.78	188.38	311.68
		Error [%]		3.95	1.98	8.02	2.49	4.66

Figure 101 – Experimental Results Comparison for two different test conditions under the same Λ condition for:
(a) Resonant State Variables under Test Condition ⑦.
(b) Resonant State Variables under Test Condition ⑧.

(a)



(b)



At ⑪ the Resonant Capacitor C_{r_1} begins to charge from G_{1IV} to G_{2IV}. In contract to the Operating Region III, upon a Transition State ⑪, the Resonant Capacitor C_{r_2}'s voltage condition is always higher than G_{2IV}. Due to that, the Interval Ⓘ completes a full resonant cycle, as shown in Figure 103.

Differently from the theoretical results, there exist a subtle coupling of the resonant ca-

Figure 102 – Experimental results under Test Condition ⑨ highlighting the Resonant State Variables.

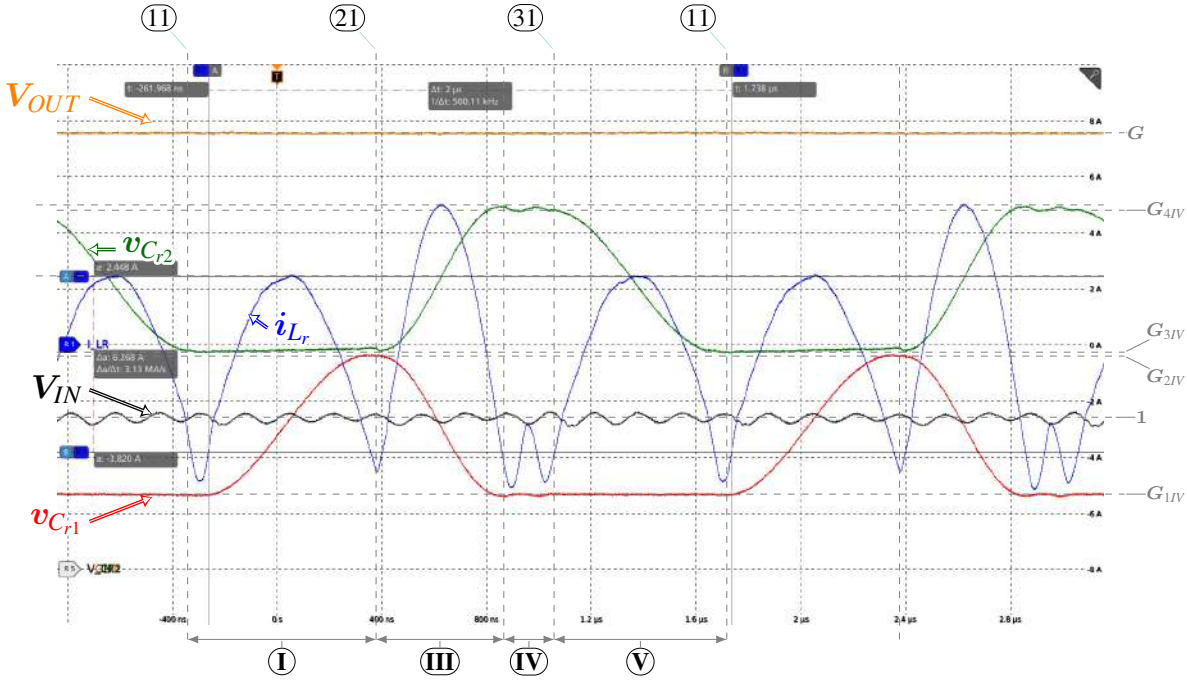
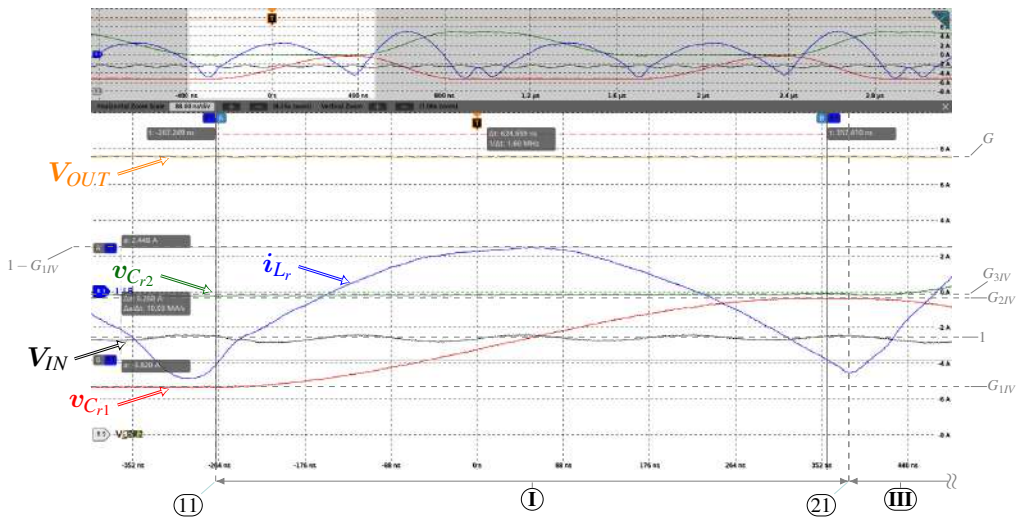


Figure 103 – 1st to 2nd Topological Stage Resonant Variables Experimental results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 500kHz$ based on Counter Clock-wise PWM Sequence.



pacitor C_{r_2} despite of its theoretical floating characteristic within Interval Ⓘ. Its coupling derives from the intrinsic output capacitance C_o of the reverse-biased Diode S_5 in series connection with the resonant capacitor C_{r_2}, forming a parallel capacitive branch to the main resonant capacitor C_{r_1}, as represented in Figure 104.

Due to the Operating Characteristic, under Operating Region IV, and the designed resonant frequency, the Transition State ㉑ triggers at the same time i_{L_r} reaches discontinuity, securing ZCS. Given this condition, the behaviour, shown in Figure 105, is identical as shown in

Figure 104 – 4LRFLCC Equivalent Circuit upon Transition State (11) including Reverse-biased Diode D_5's intrisic output capacitance C_o in which the orange dashed lines represent the current loops where i_1 is the resonant inductor's current, i_2 is the main resonant capacitor's C_{r_1} current and the i_3 is the current contribution of the non-ideal capacitive network.

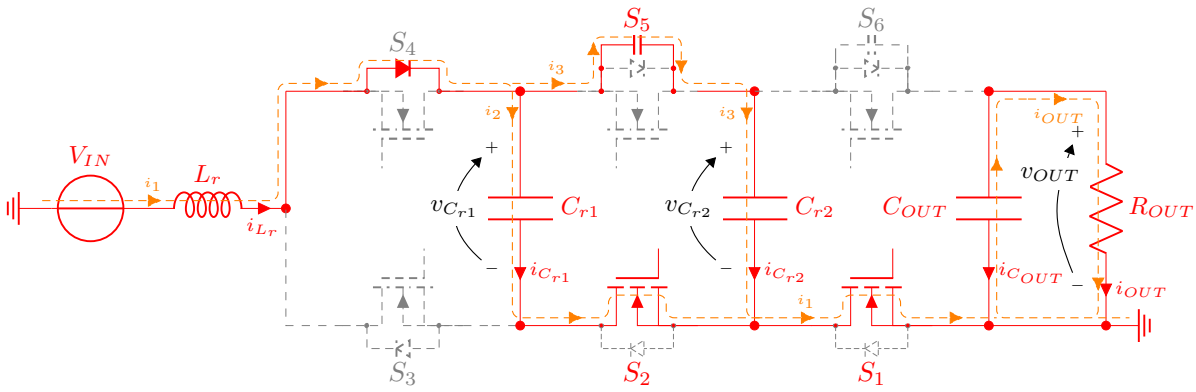
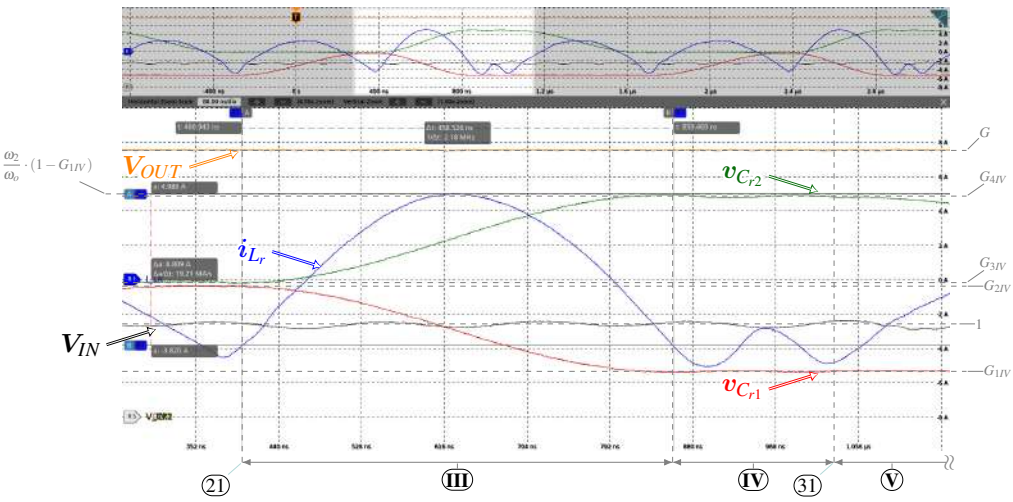


Figure 99 for the Operating Region III. Due to the resonant characteristic, Interval (III) always sustain the ZCS behaviour and Interval (IV) remains in idle state.

Figure 105 – 3rd to 4th Topological Stage Resonant Variables Experimental results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 500kHz$ based on Counter Clock-wise PWM Sequence.



The idle state becomes important due to the DCM oscillation in the inactive switch, given its dynamics and condition at the Transition State (31). The transition condition is analyzed in the following section. Figure 106 shows the resonant variables behaviour upon the Transtion State (31), its dynamics remains similar to the behaviour shown in Figure 100 for Operating Region III. Table 31 corresponds to the static resonant variables comparison with respect to the theoretical results.

Within the Operating Region IV, with non-overlapping PWM strategy, the output conversion ratio becomes constant, irrespective to the Λ condition, and its resonant variables become synchronized with the Transition States (11) and (21) in which the load condition and state vari-

Figure 106 – 5th to 6th Topological Stage Resonant Variables Experimental results under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 500kHz$ based on Counter Clock-wise PWM Sequence.

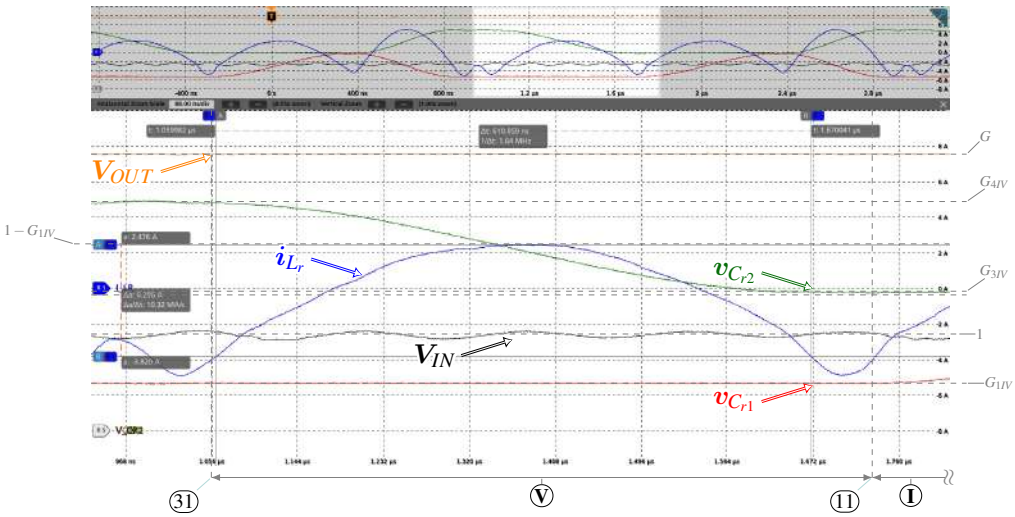


Table 31 – Test Condition set ⑨ Static Resonant Variables Comparison in between Theoretical and Experimental Results.

				Large-Signal State Variables				
			Λ	V_{OUT} $[V]$	V_{1IV} $[V]$	V_{2IV} $[V]$	V_{3IV} $[V]$	V_{4IV} $[V]$
Test Condition	⑨	Theoretical	6.36	399.05	70.23	195.80	203.24	328.82
		Experimental		387.02	66.38	190.13	195.20	320.97
		Error [%]		3.11	5.79	2.98	4.12	2.48

ables balance each other to maintain the synchronous ZCS condition within every Transition State. Figure 107 shows the output state variables for different conditions within Operating Region IV in comparison to the theoretical results.

The results are satisfactory and the experimental results validate the theoretical results' trend. There exist a visible conversion loss amongst all Operating Regions but more predominant within Operating Region III and less prevailing in Operating Region I. Amongst all Operating Regions, the conversion loss depends on the Λ condition. On the other hand, other conditions, such as under the same Λ condition, the conversion loss remains unchanged, suggesting that the load and switching frequency condition counter-measure each other, similarly to the static state variables.

Under the Operating Region IV, there exist a visible conversion loss reduction which is associated with the reduction in the effective input/output impedance of the 4LRFLCC due to the soft-charging and discharging of the resonant capacitors. Figure 108 and 109 show the experimental results for test condition ⑩ and ⑪, respectively.

Figure 107 – Experimental and Theoretical results comparison for the proposed converter within Operating Regions I to IV. The x-axis is the Λ in which each of the scatter data points represent one test condition where the different load conditions are represented by the different shapes.

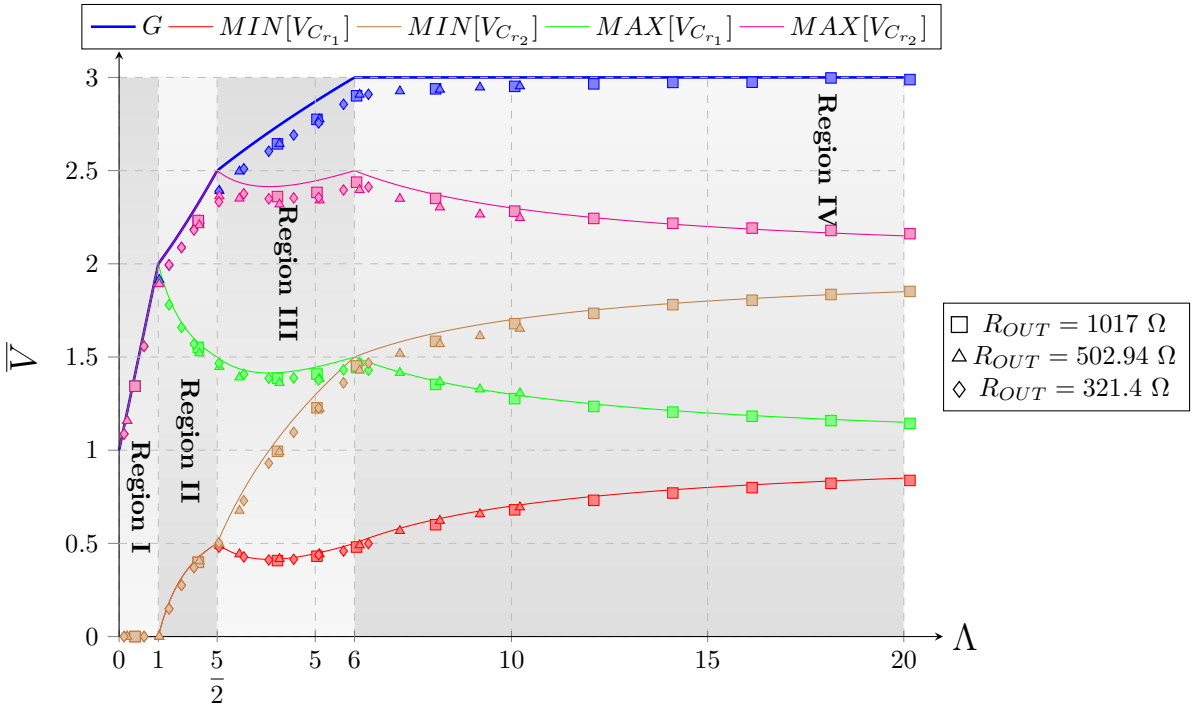
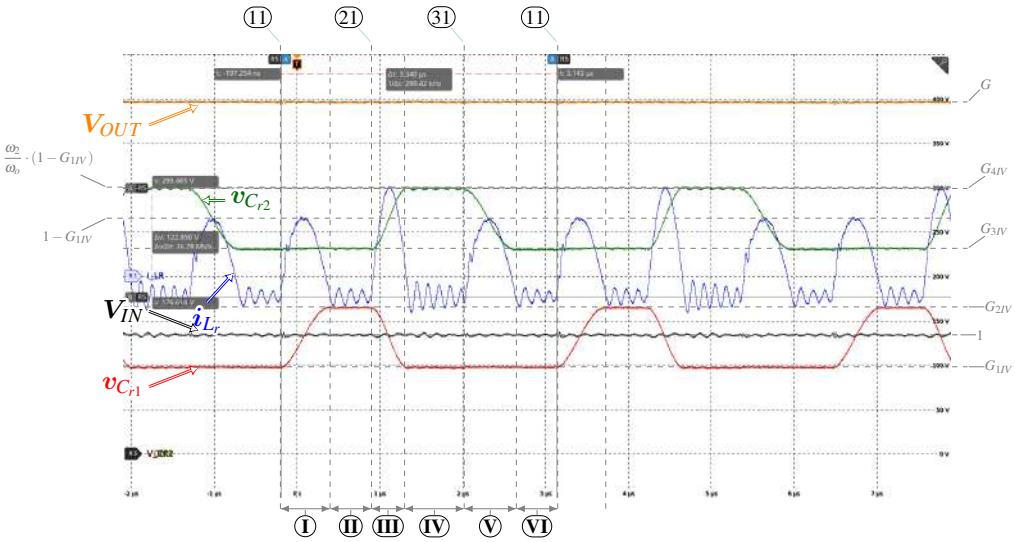


Figure 108 – Experimental results under Test Condition (10) highlighting the Resonant State Variables.



6.0.2 Switches $S_1 - S_6$'s Voltage Stresses

This chapter aims to verify the voltage stresses in the semiconductor devices $S_1 - S_6$ while assessing the difference between CCW and CW PWM Sequence in the switching losses within the same operating condition. Figure 110 depicts the voltage measurement setup for an individual Active Switch $S_1 - S_3$ in which both floating gate and drain to source are measured

Figure 109 – Experimental results under Test Condition ⑪ highlighting the Resonant State Variables.

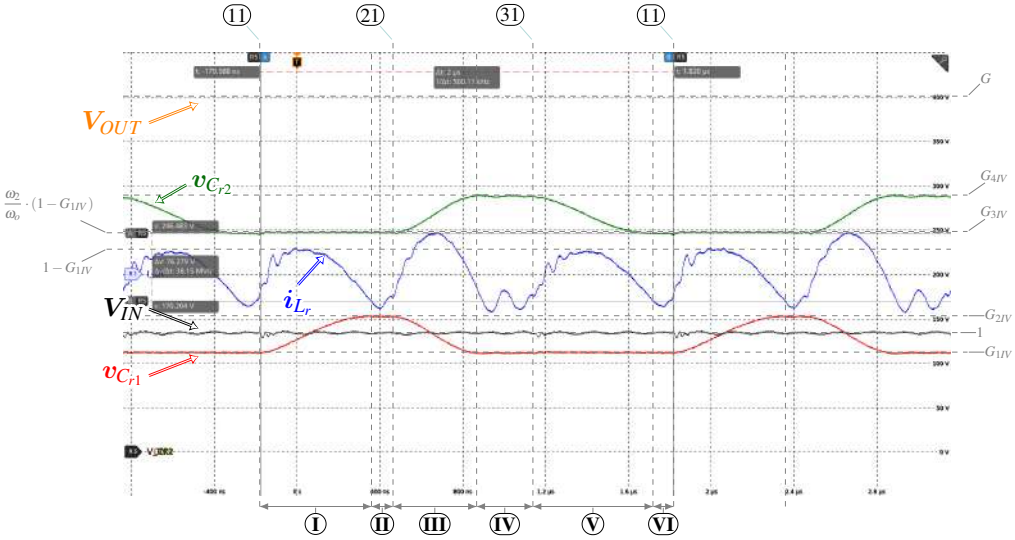


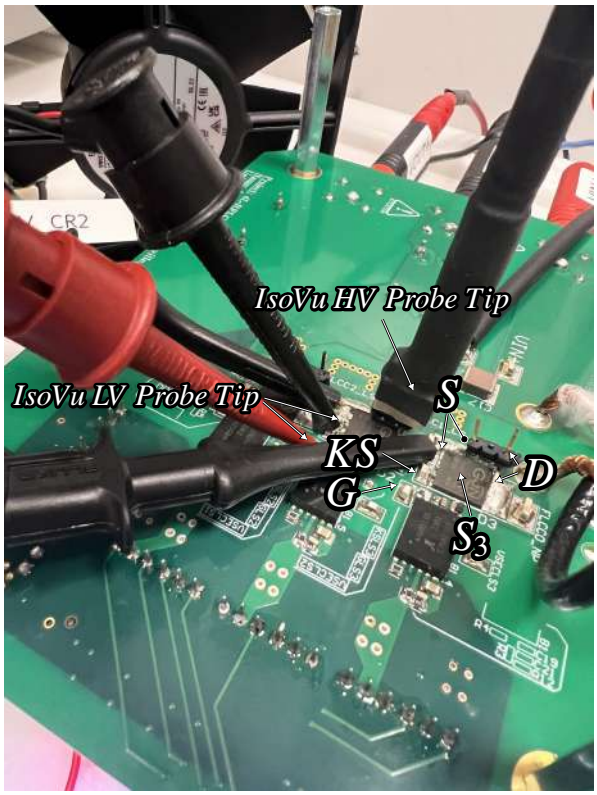
Table 32 – Test Condition set ⑩ and ⑪ Static Resonant Variables Comparison in between Theoretical and Experimental Results within Operating Region IV in order to assess the conversion loss error due to the input/output impedance.

				Large-Signal State Variables				
			Λ	$V_{OUT}\,[V]$	$V_{1III}\,[V]$	$V_{2III}\,[V]$	$V_{3III}\,[V]$	$V_{4III}\,[V]$
Test Condition	⑩	Theoretical	12.09	399.64	100.18	166.25	233.39	299.46
		Experimental		395.03	97.38	164.49	230.99	298.87
		Error [%]		1.17	2.88	1.07	1.041	0.197
	⑪	Theoretical	20.16	399.63	113.38	153.04	246.59	286.24
		Experimental		398.09	111.58	152.34	246.68	287.97
		Error [%]		0.38	1.61	0.46	-0.04	-0.60

with the a 200MHz and 1GHz IsoVu probe, respectively.

Due to common-mode interference, the measurements have been performed individually for each device, for the CW PWM Sequence, due to setup limitations which the aim was to validate and verify the experimental results as well as the robustness of the devices under different operating conditions. Upon validation, the floating gate to source has no longer been measured for the CCW PWM Sequence. Thus, a grouping of drain-to-source measurement have been made without injecting common-mode noise in the measurement instrument. Figure 111 represents the grouping in which the Active Switches $S_1 - S_3$ are measured by a 1GHz low-capacitance passive probe, 200MHz and 1GHz IsoVu probe, respectively, whereas the Passive Switches $D_4 - D_6$ have been grouped in duo due to the floating measurement and common-mode noise interference risk.

Figure 110 – Active Devices $S_1 - S_3$ High-frequency and Floating Voltage Measurement setup.



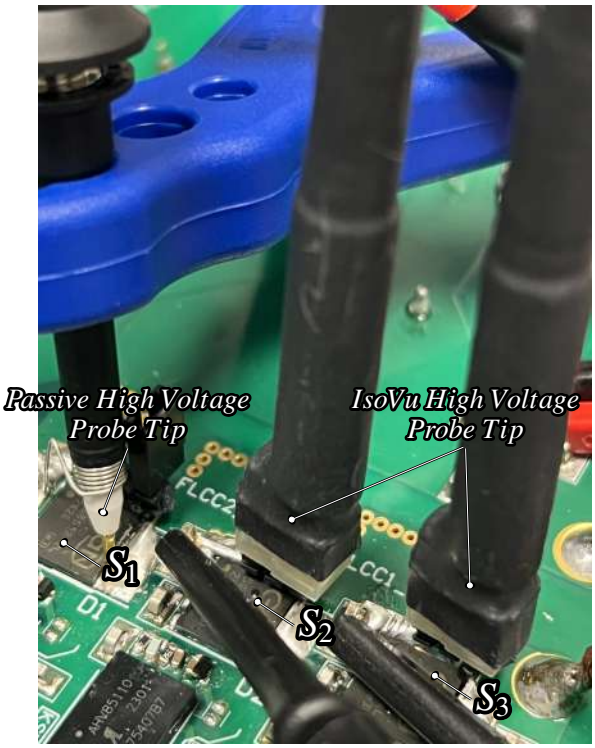
6.0.2.1 Region I

According to Test Condition ①, the Figure 112 show the outermost flying capacitor commutation loop network S_1's and D_6's voltage stresses under CW PWM Sequence, whereas Figure 113 show the innermost flying capacitor commutation loop network S_3's and D_4's voltage stresses and Figure 114 show the flying capacitor commutation loop network S_2's and D_5's voltage stresses.

According to the Table 2, upon a Transition Event ⑪, the Active Switch S_1 and Active Switch S_3 turns-ON and turns-OFF, respectively, for the CW PWM Sequence.

Prior to the Transition Event ⑪, the 4LRFLCC is in Idle State, which makes the Active Switch S_1's and Passive Switch D_6's voltage tend to V_{IN} and $V_{OUT} - V_{IN}$, respectively. Upon the Transition Event, the Active Switch S_1 hard-switches, and discharges its C_{out}'s energy within its 2DEG channel, as shown in Figure 115a leading to a loss mechanism. Simultaneously, the Passive Switch D_6, given its topology connection, hard-charges its C_{out} up to the differential voltage $V_{OUT} - v_{C_{r_2}}$ with a rising time associated with the Active Switch S_1. As the resonant capacitor C_{r_2}'s initial condition is $0V$, it charges from $V_{OUT} - V_{IN}$ to V_{OUT}, as shown in Figure 115b. This hard-charge is associated with an energy that is dissipated along the path, which includes the Active Switch S_1, Output Capacitor C_{OUT}, Resonant Capacitor C_{r_2} and the PCB resistances. Additionally, it is also underlined by a very high-frequency oscillation derived due to the total commutation loop stray inductance and the Passive Switch D_6's output capacitor's C_{out}, upon a given steep charge/discharge current.

Figure 111 – Passive Devices $D_4 - D_6$ High-frequency and Floating Voltage Measurement setup.



Similarly, prior to the Transition Event (11), and the Resonant Capacitor C_{r_1}'s voltage condition, the Passive Diode D_4's blocking voltage is 0V, as shown in Figure 116b. Due to that, upon the Transition Event (11 ↓), the Active Switch S_3 turns-OFF under ZVS and ZCS condition. Upon the Transition Event (11 ↑), the Passive Diode D_4 forward-biases and the Active Switch S_3's blocking voltage follows the Resonant Capacitor C_{r_1}'s voltage, leading to a soft-charge in the Active Switch S_3's output capacitor C_{out}, events highlighted in Figure 116a.

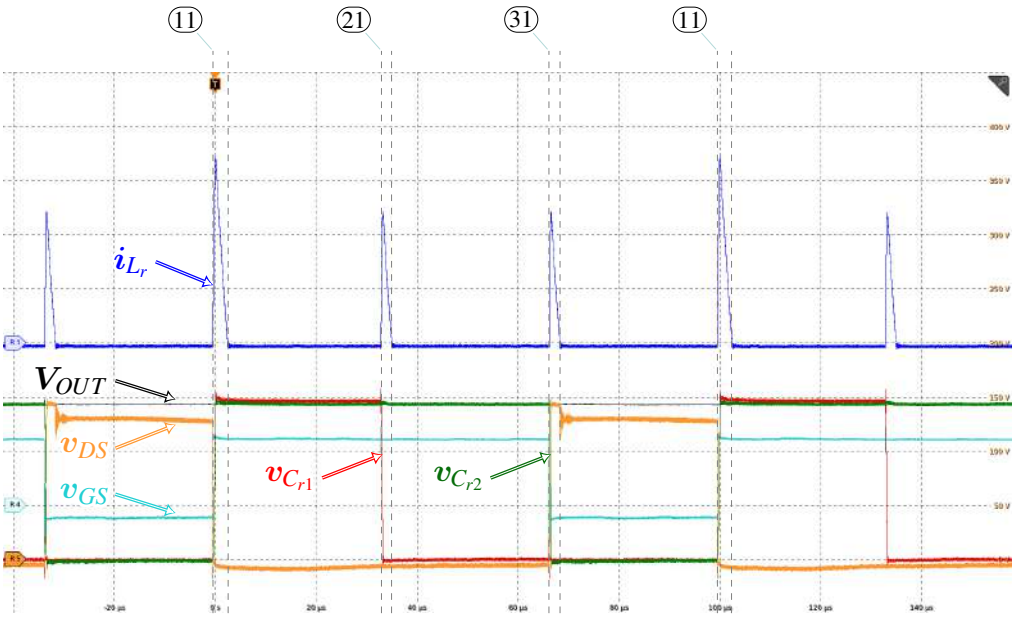
Within the Interval (I), the Passive Switch D_6's voltage decreases due to its topology connection, leading to a complete soft-discharge due to the 4L-RFLCC behaviour within the Operating Region I. Upon the complete soft-discharge, it coincides with its foward-biases mechanism, leading to a ZVS turn-ON condition upon transition to the Interval (II), as shown in Figure 117.

Upon entrance into the Interval (III), the Passive Diode D_4 reverse-biases under ZCS condition while the Active Switch S_3 remains in OFF-state. Due to the Passive Diode D_4 reverse-bias mechanism, the Active Switch S_3's voltage changes from V_{OUT} to V_{IN}. The voltage step-down, and its dynamic, are underlined by a high-frequency oscillation derived from the resonant inductor L_r and the Active Switch S_3's output capacitor C_{oss}, highlighted in Figure 116a. Simultaneously, the Passive Diode D_4's voltage changes from $0V$ to $V_{OUT} - V_{IN}$ also underlined by the same high-frequency oscillation, as shown in Figure 116b.

Following the PWM sequencing, the Active Switch S_3 and S_2 turn-ON and turn-OFF, respectively, at the Transition State (21). Similarly to the previous transition state, preceding the

Figure 112 – Switch S_1 and D_6 Voltage Stresses Experimental Results within Operating Region I and Test Condition ①:
(a) Active Switch S_1 under Test Condition ①.
(b) Passive Switch D_6 under Test Condition ①.

(a)



(b)

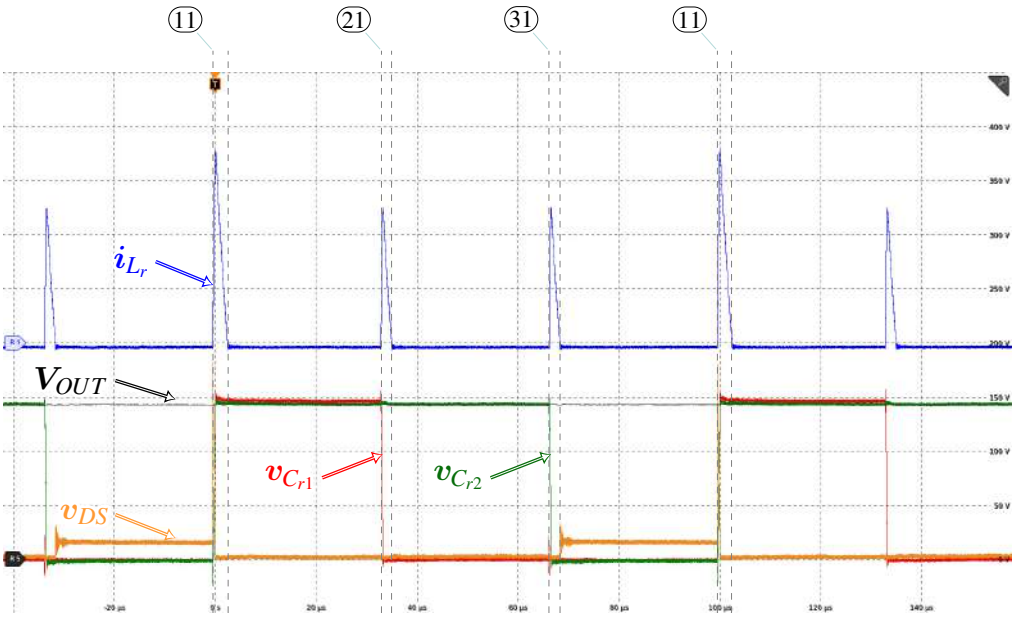
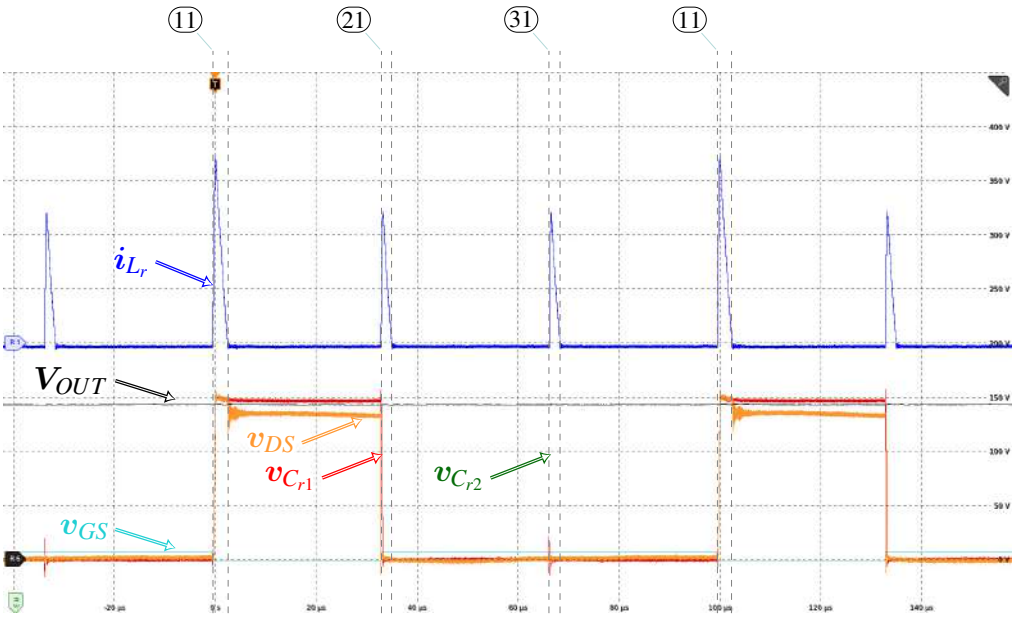


Figure 113 – Switch S_3 and D_4 Voltage Stresses Experimental Results within Operating Region I and Test Condition ①:
(a) Active Switch S_3 under Test Condition ①.
(b) Passive Switch D_4 under Test Condition ①.

(a)



(b)

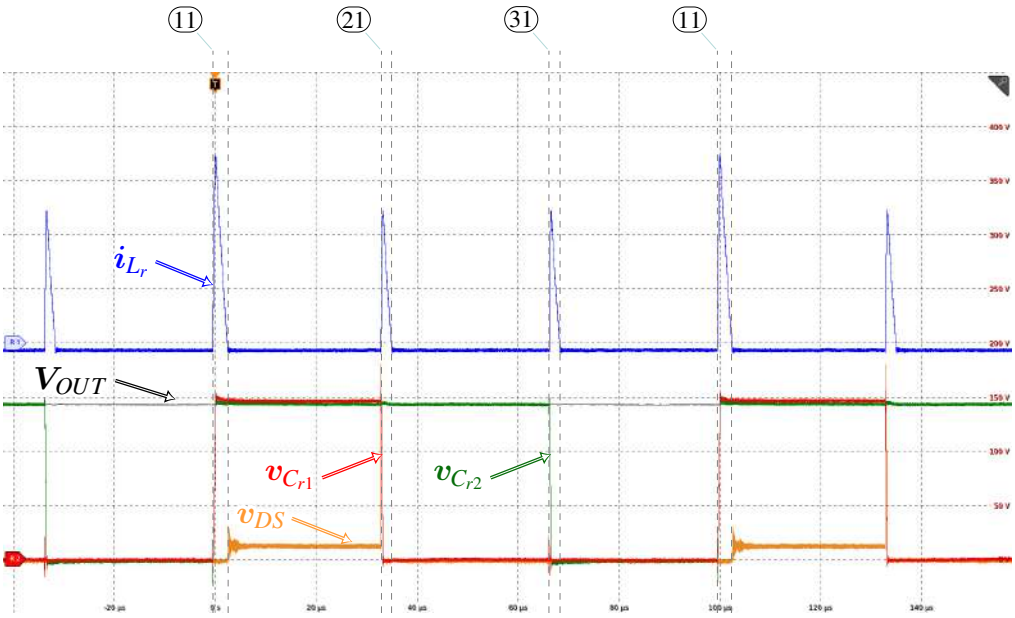
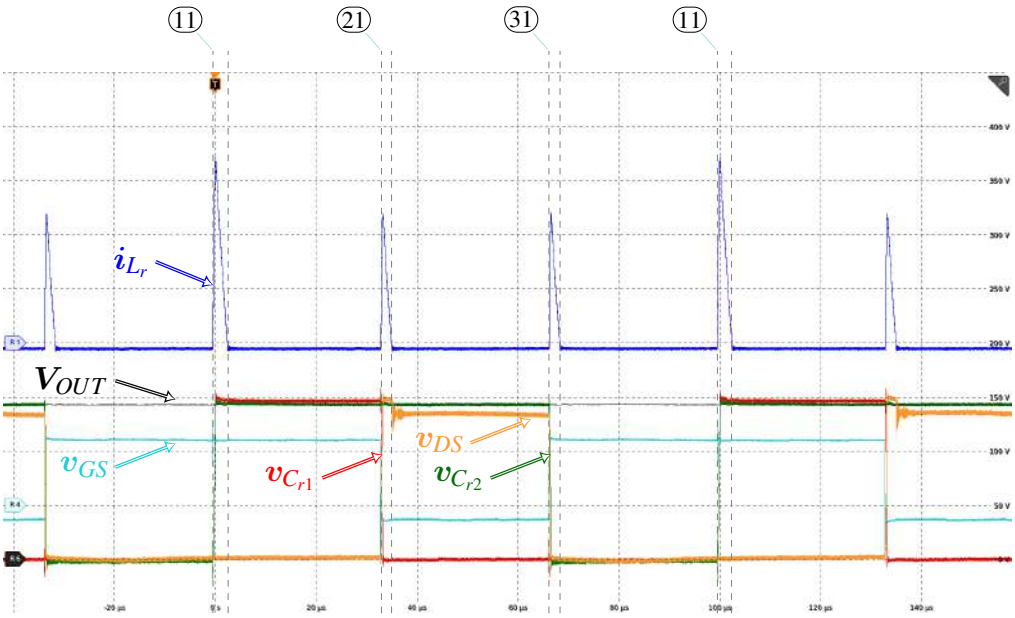


Figure 114 – Switch S_2 and D_5 Voltage Stresses Experimental Results within Operating Region I and Test Condition ①:
(a) Active Switch S_2 under Test Condition ①.
(b) Passive Switch D_5 under Test Condition ①.

(a)



(b)

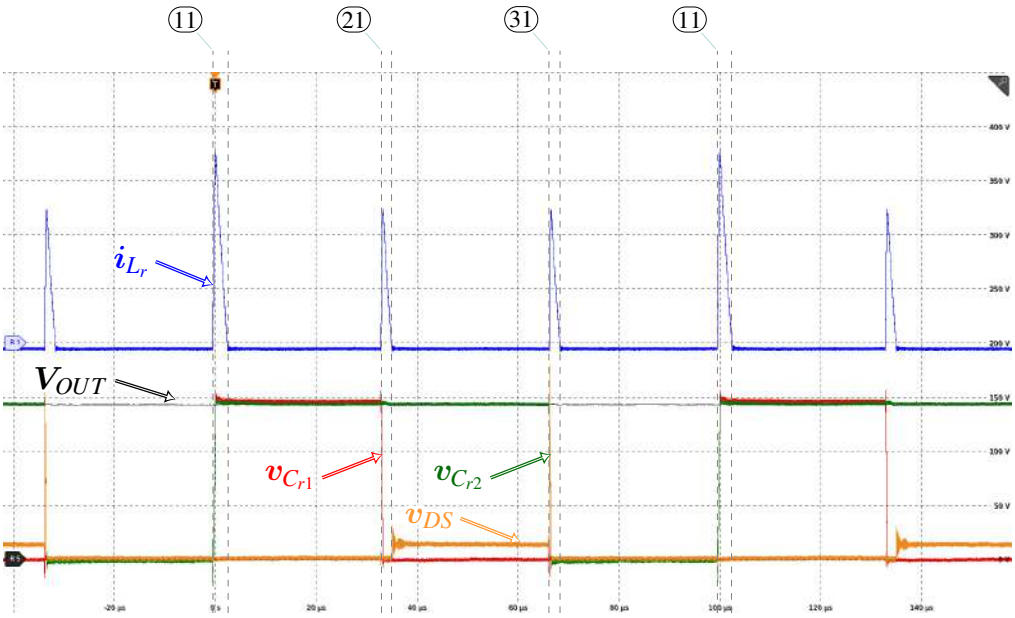
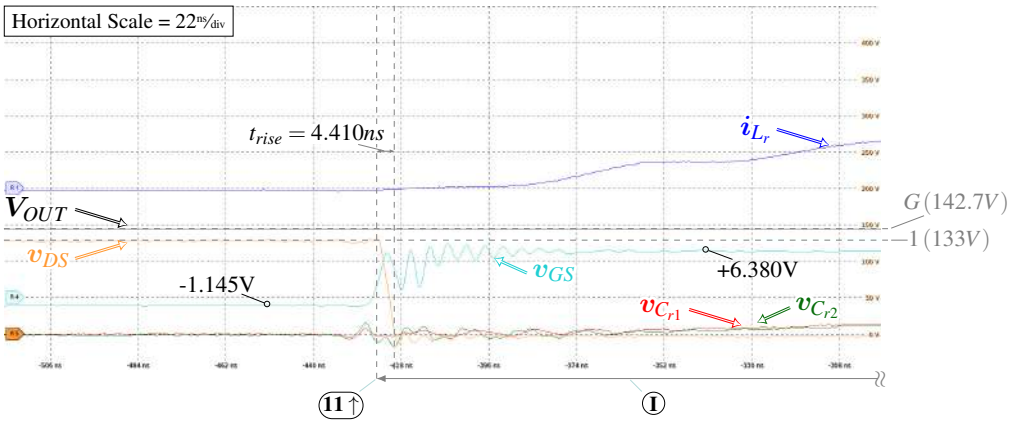
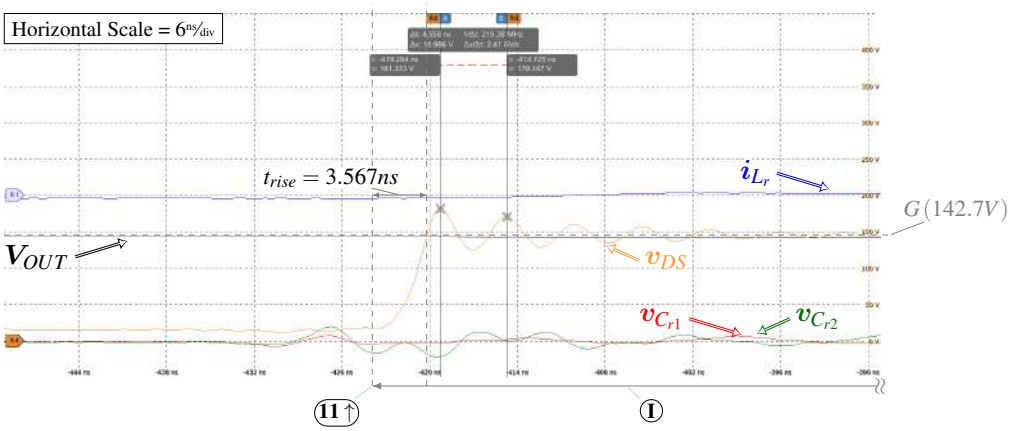


Figure 115 – Dynamic Voltage Behaviour upon Transition Event (11) under Test Condition (1) for:
(a) Active Switch S_1 turn-ON process.
(b) Passive Switch D_6 reverse-biasing process.

(a)



(b)



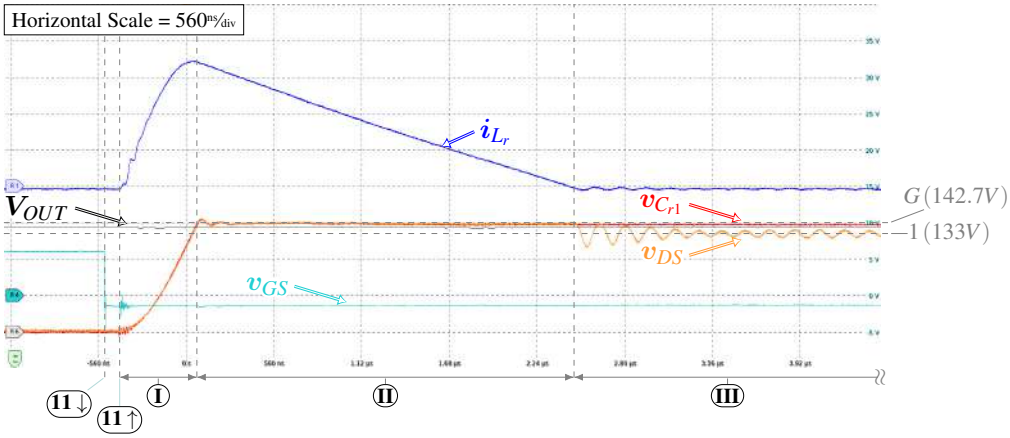
Transition State (21), the 4L-RFLCC is in Idle State, which makes the Active Switch S_3's voltage tend to V_{IN}.

Upon the Transition Event, the Active Switch S_3 hard-switches, and discharges its C_{out}'s energy within its 2DEG channel, as shown in Figure 118a leading to a loss mechanism. Simultaneously, the Passive Switch D_4, given its topology connection, hard-charges its C_{oss} up to the floating voltage $v_{C_{r_1}}$ with a rising time associated with the Active Switch S_3. As the resonant capacitor C_{r_1}'s initial condition is V_{OUT}, it charges from $V_{OUT} - V_{IN}$ to V_{OUT}, as shown in Figure 118b. This hard-charge is associated with an energy that is dissipated along the path, which includes the Active Switch S_3, Resonant Capacitor C_{r_1} and the PCB resistances. Additionally, it is also underlined by a very high-frequency oscillation derived due to the total commutation loop stray inductance and the Passive Switch D_4's output capacitor's C_{oss}, upon a given steep charge/discharge current.

Similarly, prior to the Transition Event (21), and the Resonant Capacitors C_{r_1} and C_{r_2}'s voltage condition, the Passive Diode D_5's blocking voltage is 0V, as shown in Figure 119b. Due

Figure 116 – Dynamic Voltage Behaviour upon Transition Event ⑪ under Test Condition ①
for:
(a) Active Switch S_3 turn-OFF process.
(b) Passive Switch D_4 foward-biasing process.

(a)



(b)

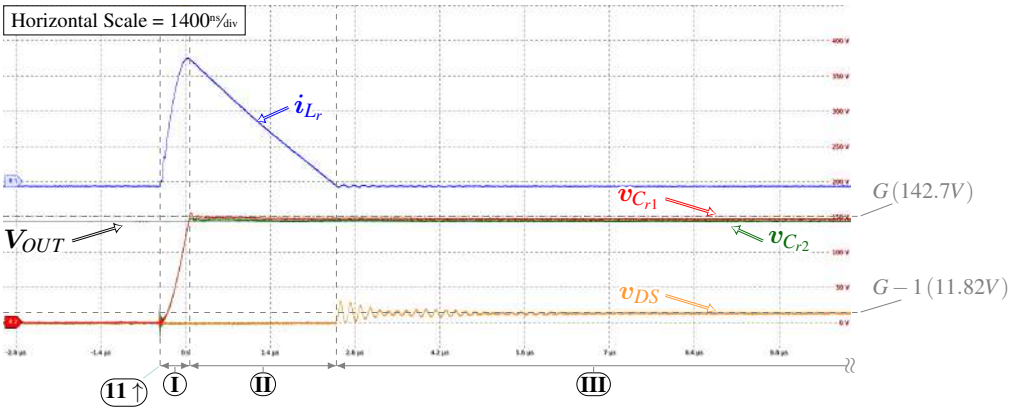


Figure 117 – Switch D_6 Dynamic voltage behaviour upon Transient Event ⑪ under Test Condition ①.

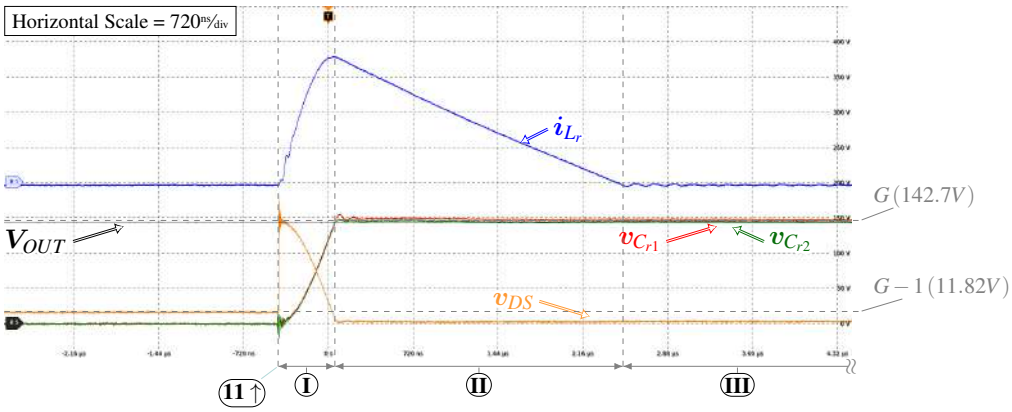
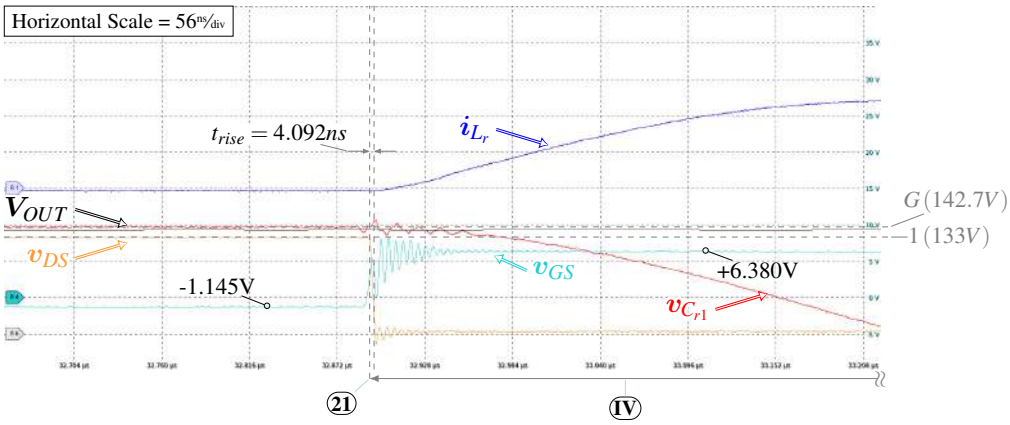
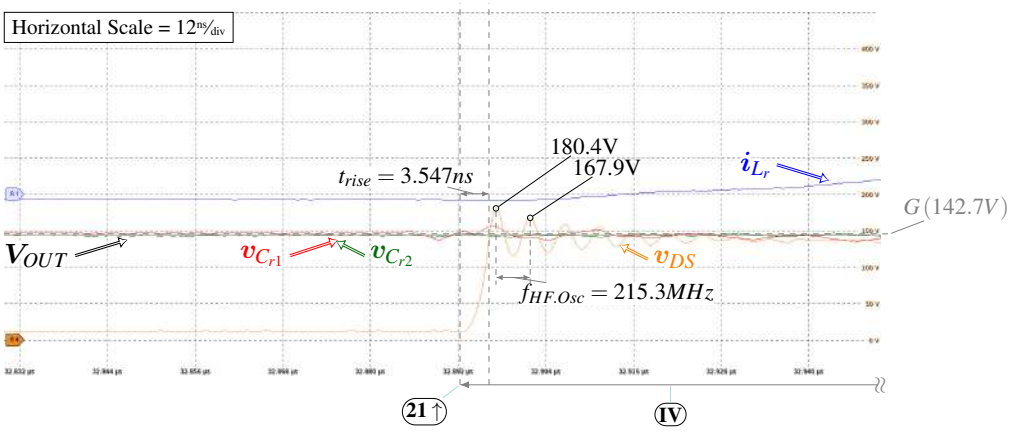


Figure 118 – Dynamic Voltage Behaviour upon Transition Event (21) under Test Condition (1) for:
(a) Active Switch S_3 turn-ON process.
(b) Passive Switch D_4 reverse-biasing process.

(a)



(b)



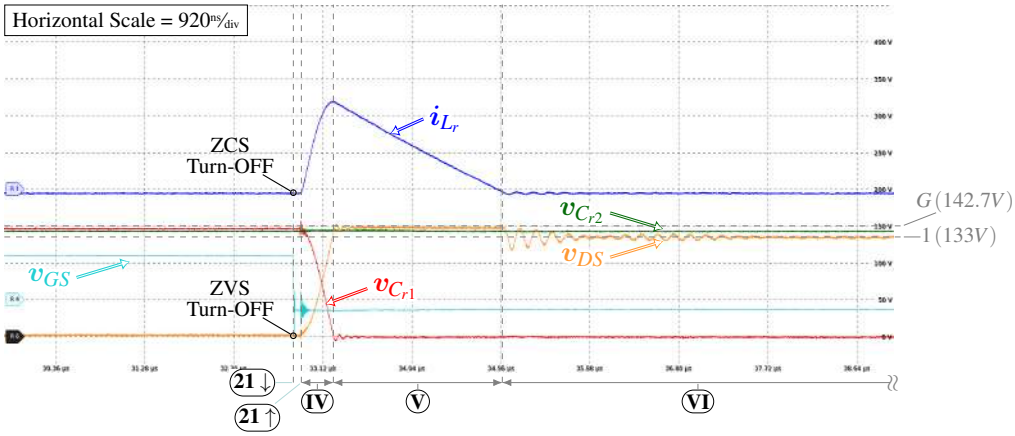
to that, upon the Transition Event (21↓), the Active Switch S_2 turns-OFF under ZVS and ZCS condition. Upon the Transition Event (21↑), the Passive Diode D_5 forward-biases and the Active Switch S_2's blocking voltage follows the differential voltage in between the Resonant Capacitor C_{r_1} and C_{r_2}, leading to a soft-charge in the Active Switch S_2's output capacitor C_{oss}, events highlighted in Figure 119a.

In a similar manner, as expressed by the Passive Switch D_6, the Passive Switch D_4's voltage decreases due to its topology connection, leading to a complete soft-discharge due to the 4L-RFLCC behaviour within the Operating Region I. Upon the complete soft-discharge, it coincides with its foward-biases mechanism, leading to a ZVS turn-ON condition upon transition to the Interval (V), as shown in Figure 120.

Following the PWM sequencing, the Active Switch S_2 and S_1 turn-ON and turn-OFF, respectively, at the Transition State (31). Similarly to the previous transition state, preceding the Transition State (31), the 4L-RFLCC is in Idle State, which makes the Active Switch S_2's voltage tend to V_{IN}.

Figure 119 – Dynamic Voltage Behaviour upon Transition Event 21 under Test Condition 1 for:
(a) Active Switch S_2 turn-OFF process.
(b) Passive Switch D_5 foward-biasing process.

(a)



(b)

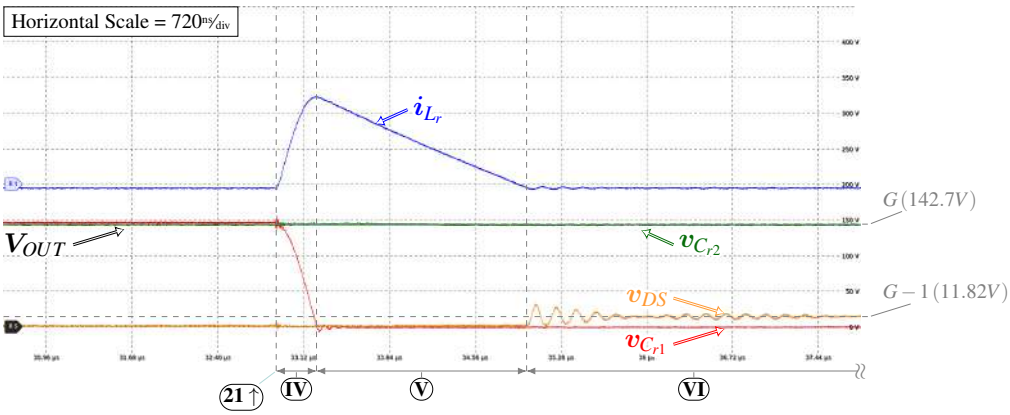


Figure 120 – Switch D_4 Dynamic voltage behaviour upon Transient Event 21 under Test Condition 1.

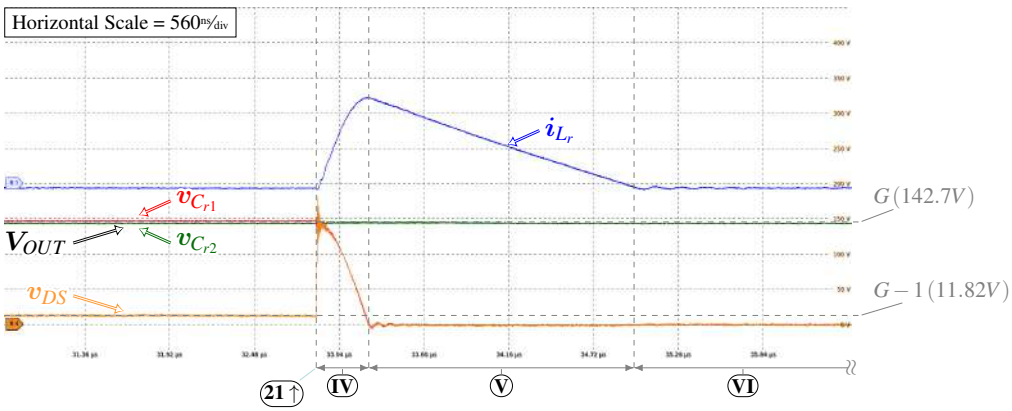
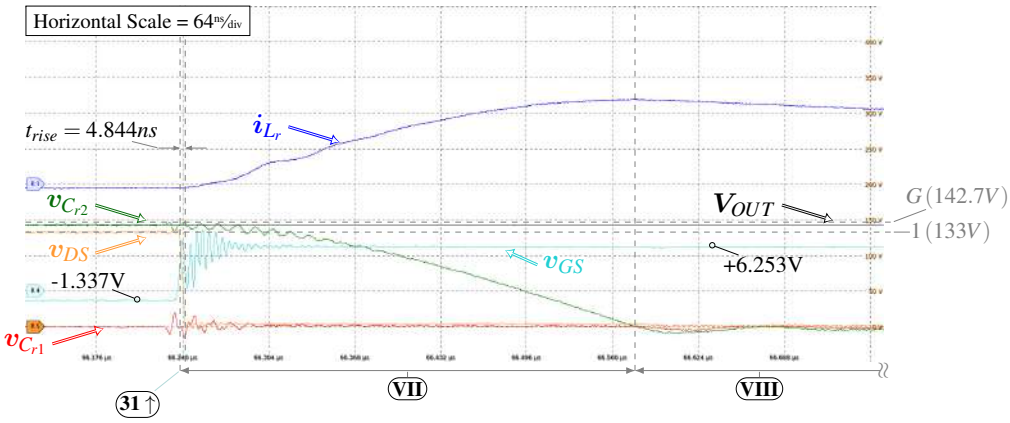
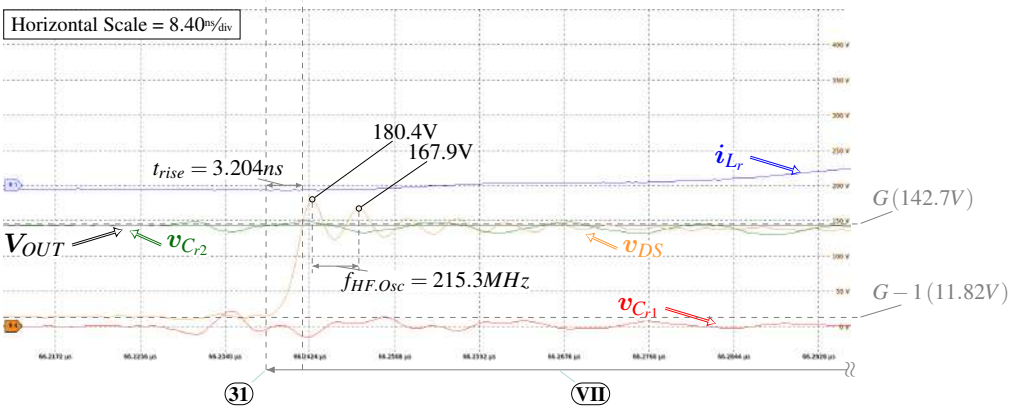


Figure 121 – Dynamic Voltage Behaviour upon Transition Event (31) under Test Condition (1) for:
(a) Active Switch S_3 turn-ON process.
(b) Passive Switch D_5 reverse-biasing process.

(a)



(b)

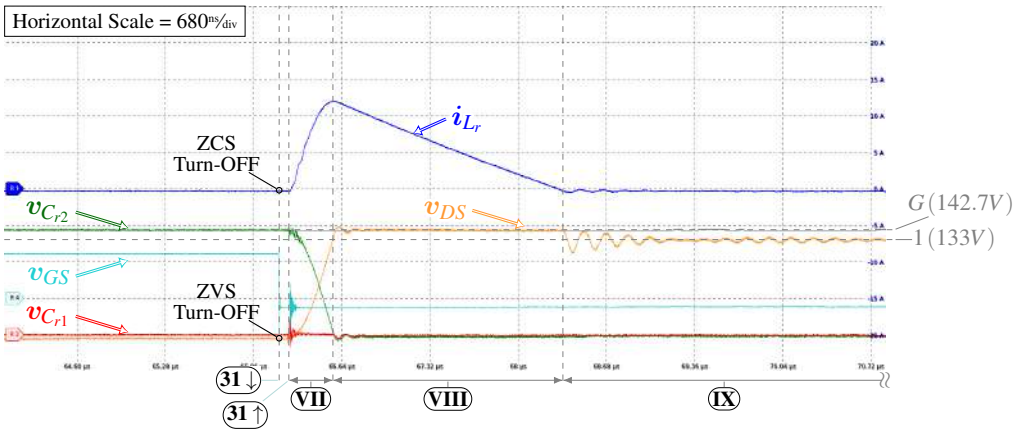


Upon the Transition Event, the Active Switch S_2 hard-switches, and discharges its C_{out}'s energy within its 2DEG channel, as shown in Figure 121a leading to a loss mechanism. Simultaneously, the Passive Switch D_5, given its topology connection, hard-charges its C_{out} up to the differential voltage in between $v_{C_{r_2}}$ and $v_{C_{r_1}}$ with a rising time associated with the Active Switch S_2. As the resonant capacitor C_{r_2} and C_{r_1}'s initial condition is V_{OUT} and $0V$, respectively, it charges from $V_{OUT} - V_{IN}$ to V_{OUT}, as shown in Figure 121b. This hard-charge is associated with an energy that is dissipated along the path, which includes the Active Switch S_2, Resonant Capacitors C_{r_1} and C_{r_2} and the PCB resistances. Additionally, it is also underlined by a very high-frequency oscillation derived due to the total commutation loop stray inductance and the Passive Switch D_5's output capacitor's C_o, upon a given steep charge/discharge current.

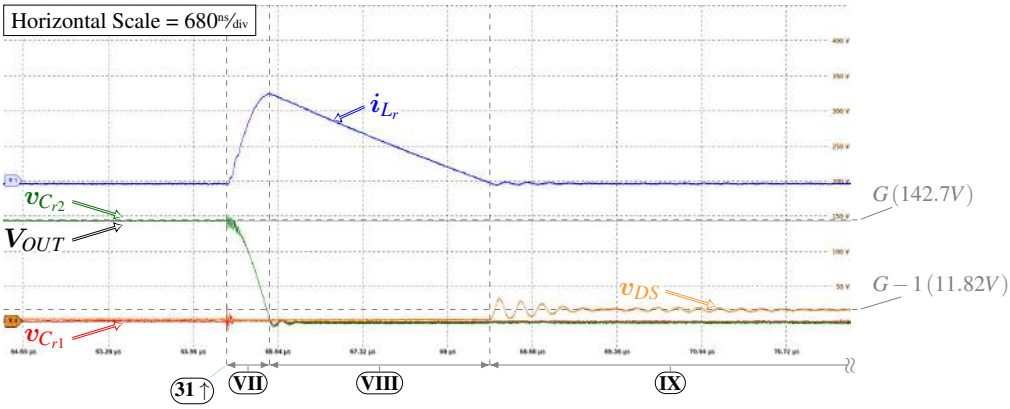
Identically to the Transition State (21), prior to the Transition State (31), and due to the Output Capacitor C_o and Resonant Capacitor C_{r_2}'s voltage condition, the Passive Diode D_6's blocking voltage is 0V, as shown in Figure 122b. Due to that, upon the Transition Event (31 ↓), the Active Switch S_1 turns-OFF under ZVS and ZCS condition. Upon the Transition Event (31 ↑), the Passive Diode D_6 forward-biases and the Active Switch S_1's blocking voltage follows the

Figure 122 – Dynamic Voltage Behaviour upon Transition Event (31) under Test Condition (1) for:
(a) Active Switch S_1 turn-OFF process.
(b) Passive Switch D_6 foward-biasing process.

(a)



(b)



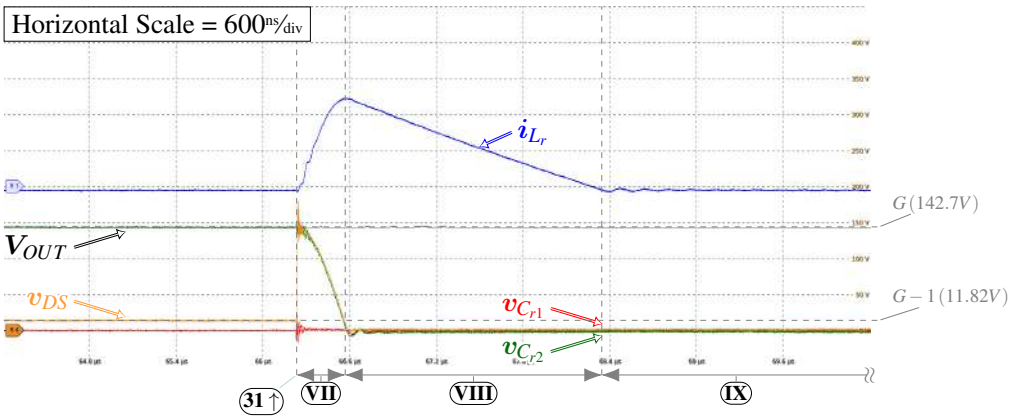
differential voltage in between the Resonant Capacitor C_{r_2} and Output Capacitor C_{OUT}, leading to a soft-charge in the Active Switch S_1's output capacitor C_{oss}, events highlighted in Figure 122a.

In a similar manner, as expressed by the Passive Switches D_4 and D_6, the Passive Switch D_5's voltage decreases due to its topology connection, leading to a complete soft-discharge due to the 4L-RFLCC behaviour within the Operating Region I. Upon the complete soft-discharge, it coincides with its foward-biases mechanism, leading to a ZVS turn-ON condition upon transition to the Interval (VIII), as shown in Figure 123.

6.0.2.2 Region II

According to Test Condition (4), the Figure 124 show the outermost flying capacitor commutation loop network S_1's and D_6's voltage stresses under CW PWM Sequence, whereas Figure 125 show the innermost flying capacitor commutation loop network S_3's and D_4's voltage stresses and Figure 126 show the flying capacitor commutation loop network S_2's and D_5's

Figure 123 – Switch D_5 Dynamic voltage behaviour upon Transient Event (31) under Test Condition (1).



voltage stresses.

Within each Transition Event, the switching transition behaves similar to the behavior displayed in Section 6.0.2.1, where each flying capacitor commutation loop cell's device's pair is exposed to the differential voltage in between adjacent cells. Additionally, upon the idle states, the large-signal voltage conditions change, as seen in the previous sections. Therefore, modifying the amplitude of the step-excitation into the resonant tank derived from the connection in between the resonant inductor L_r and the disabled Active Switch $S_1 - S_3$ with a distinguishable difference in the intensity of the high-frequency oscillation, as shown in Figures 124 - 126.

Differently from the expected theoretical behavior, upon the Transition Event (11), while the Active Switch S_3 turns-OFF under ZVS condition thanks to the introduced dead-time in between (11 ↓) and (11 ↑), there exist a forward-biasing delay time due to the transition time when the Passive Switch D_4 soft turns-ON as a result of the soft-charging of the Active Switch S_3's output capacitance, as shown in Figure 127.

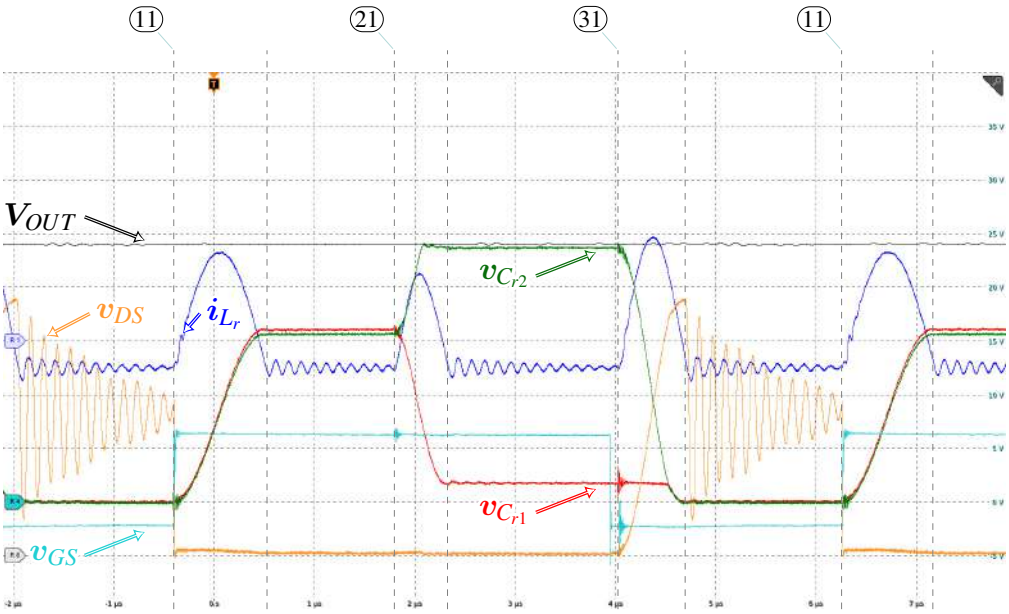
The soft-charging mechanism derives a new resonance with a much higher frequency, compared to the fundamental resonant frequency, composed by the resonant inductor L_r and the Active Switch S_3's and Passive Switch D_4's output capacitances.

Upon the synchronous soft charge/discharge, at the instant (11+), the resonant current discontinues from the Active Switch S_3, leading to an oscillation in the resonant inductor's current i_{L_r} while the resonant capacitors start to charge as per the expected equivalent circuit within Interval (I).

Upon the transition to the first Idle State, Interval (II), the Active Switch S_3 remains in the OFF-state whereas the Passive Switch D_5 remains forward-biased due to the resonant capacitors' voltage condition. Given the Active Switch S_1's state, the Passive Switch D_6 remains reverse-biased and blocking the differential voltage in between the Resonant Capacitors' C_{r_2} and Resonant Capacitors' C_{r_1}. On the other hand, due to the discontinuity, the Passive Switch D_4 reverse-biases, under ZCS condition, and resonates synchronously with the Active Switch S_3 in order to maintain the voltage balance according to Kirchhoff's law, as shown in Figure

Figure 124 – Switch S_1 and D_6 Voltage Stresses Experimental Results within Operating Region II and Test Condition ④:
(a) Active Switch S_1 under Test Condition ④.
(b) Passive Switch D_6 under Test Condition ④.

(a)



(b)

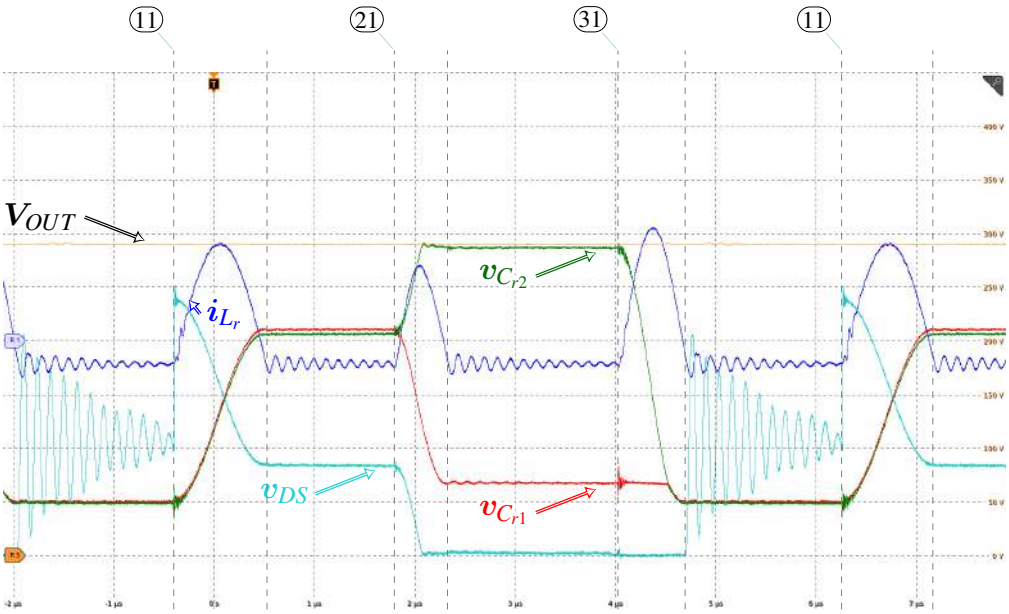
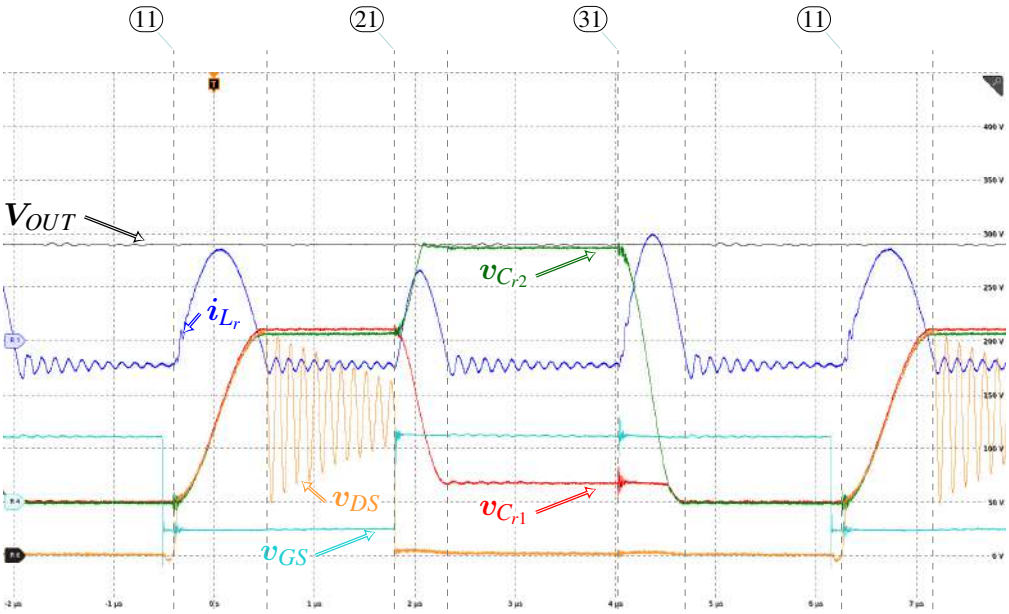


Figure 125 – Switch S_3 and D_4 Voltage Stresses Experimental Results within Operating Region II and Test Condition ④:
(a) Active Switch S_3 under Test Condition ④.
(b) Passive Switch D_4 under Test Condition ④.

(a)



(b)

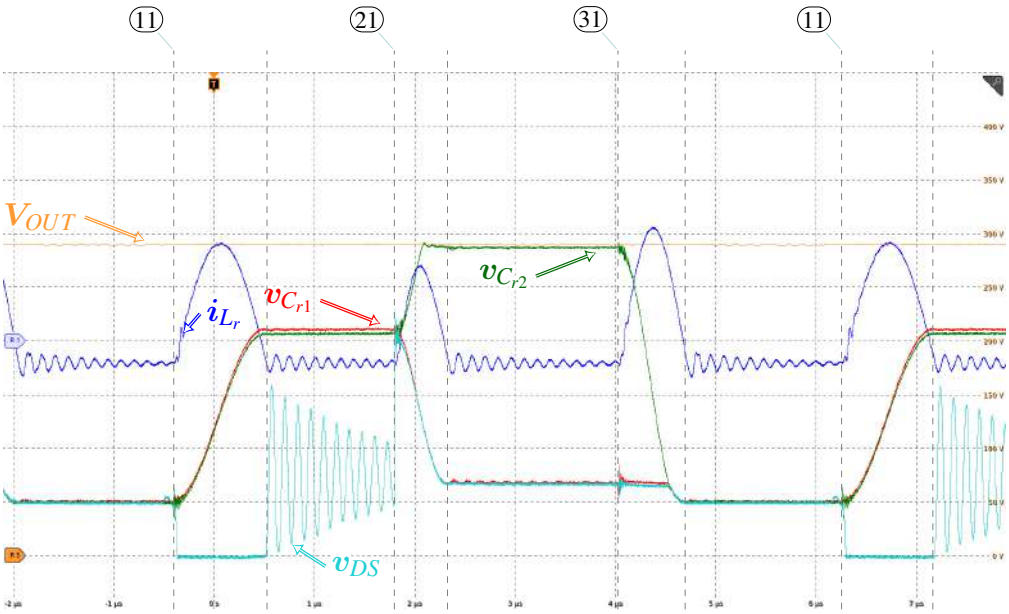
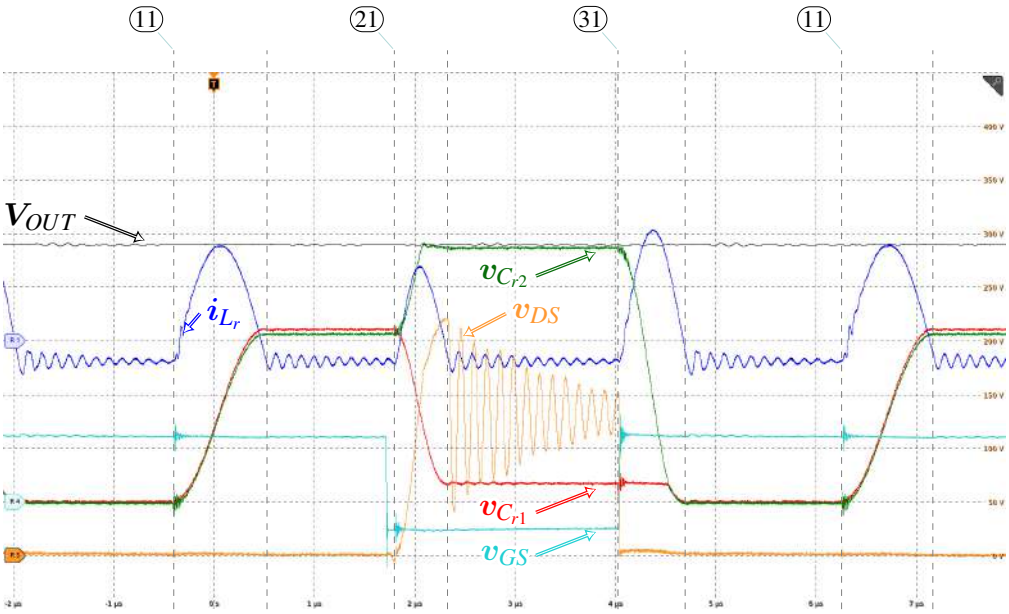


Figure 126 – Switch S_2 and D_5 Voltage Stresses Experimental Results within Operating Region II and Test Condition ④:
(a) Active Switch S_2 under Test Condition ④.
(b) Passive Switch D_5 under Test Condition ④.

(a)



(b)

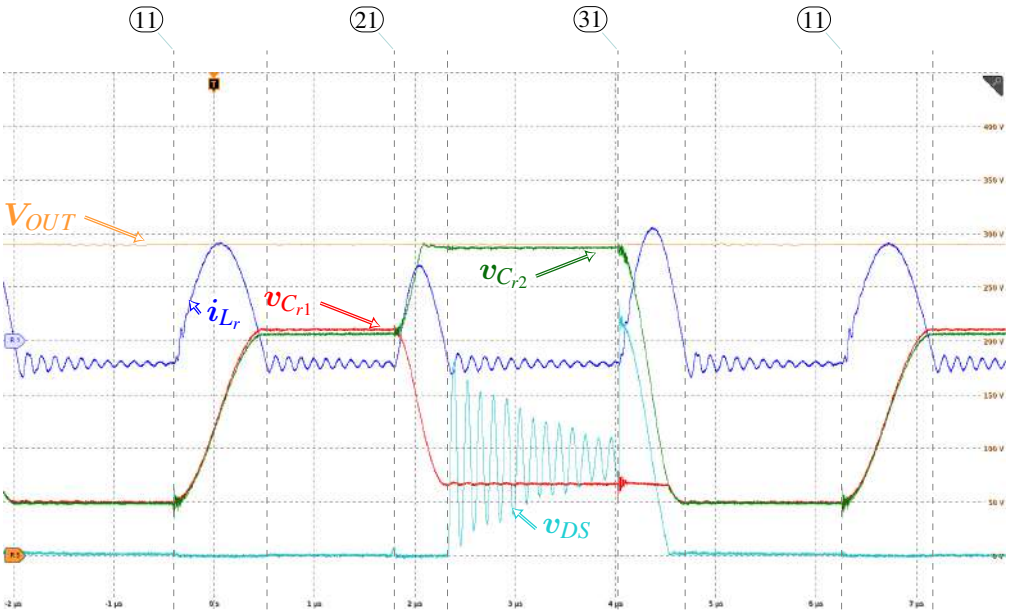
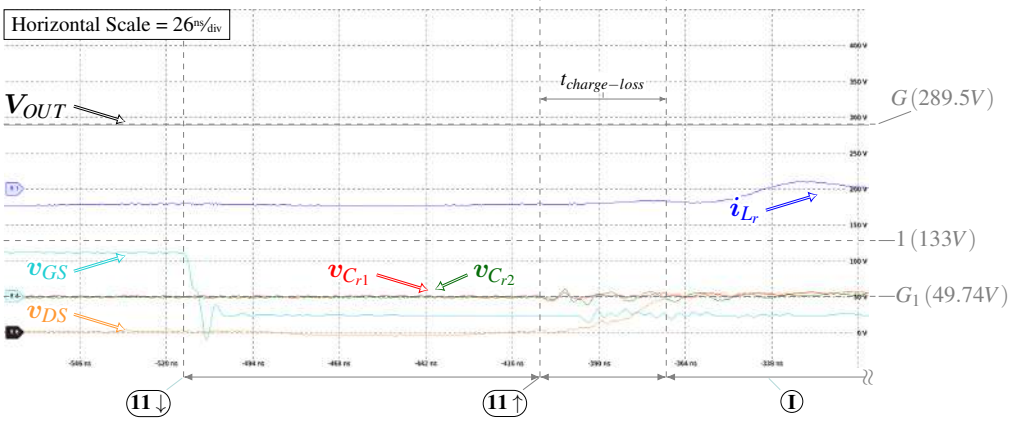
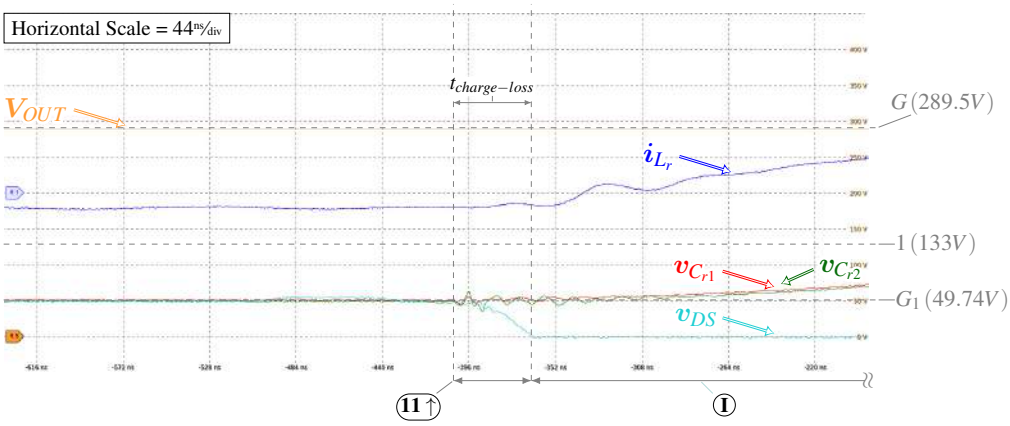


Figure 127 – Dynamic Voltage Stresses Experimental Results within Operating Region II and Test Condition ④ upon a Transition Event (11↑) for:
(a) Active Switch S_3 .
(b) Passive Switch D_4 .

(a)



(b)



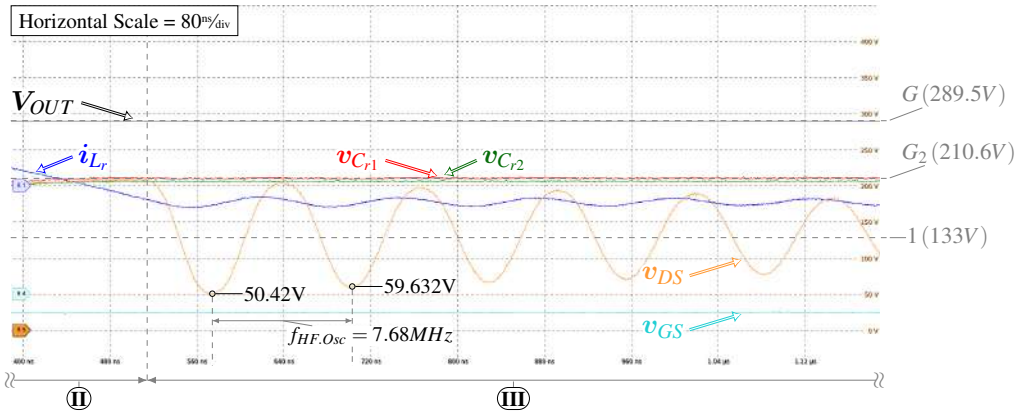
128. The undampness demonstrates the low-ohmic damping factor in the equivalent RLC circuit. The Idle State's time duration becomes shorter due to the higher switching frequency in the Test Condition ④, leading to the Transition Event (21) while resonant behavior is still in progress.

Upon the transition to the second Idle State, Interval Ⓥ, the Active Switch S_2 remains in the OFF-state whereas the Passive Switch D_6 remains forward-biased due to the resonant capacitor C_{r_2}'s voltage condition. Given the Active Switch S_3's state, the Passive Switch D_4 remains reverse-biased and blocking the voltage across the Resonant Capacitor C_{r_1}. On the other hand, similarly to the first Idle State, the Passive Switch D_5 reverse-biases, under ZCS condition, and resonates synchronously with the Active Switch S_2, as shown in Figure 129.

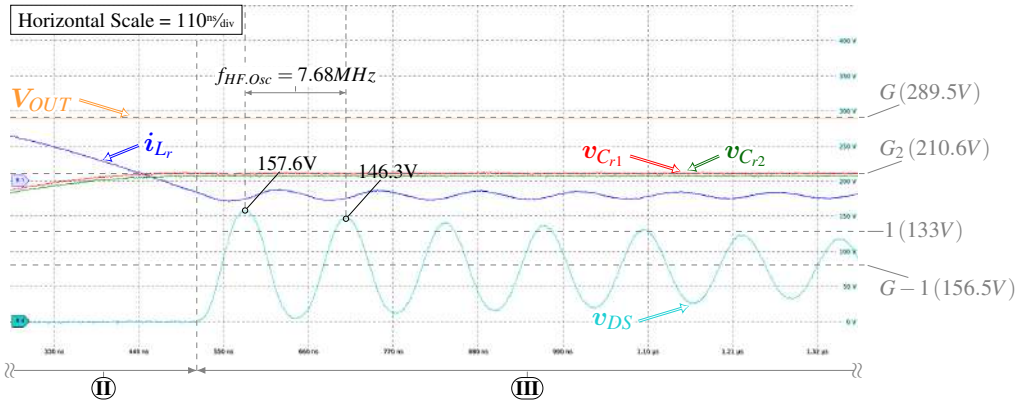
Upon the transition to the third Idle State, Interval (VIII), the Active Switch S_1 remains in the OFF-state whereas the Passive Switch D_5 remains forward-biased due to the resonant capacitors' voltage condition. Given the Active Switch S_3's state, the Passive Switch D_4 remains reverse-biased and blocking the voltage across the Resonant Capacitor C_{r_1}, similarly as in the second Idle State. On the other hand, the Passive Switch D_6 reverse-biases, under ZCS condition, and resonates synchronously with the Active Switch S_1, as shown in Figure 130.

Figure 128 – Dynamic Voltage Stresses Experimental Results within Operating Region II and Test Condition ④ upon a transition to the first Idle State for:
(a) Active Switch S_3 .
(b) Passive Switch D_4 .

(a)



(b)



6.0.2.3 Region III

According to Test Condition ⑥, the Figure 131 show the outermost flying capacitor commutation loop network S_1's and D_6's voltage stresses under CW PWM Sequence, whereas Figure 132 show the innermost flying capacitor commutation loop network S_3's and D_4's voltage stresses and Figure 133 show the flying capacitor commutation loop network S_2's and D_5's voltage stresses.

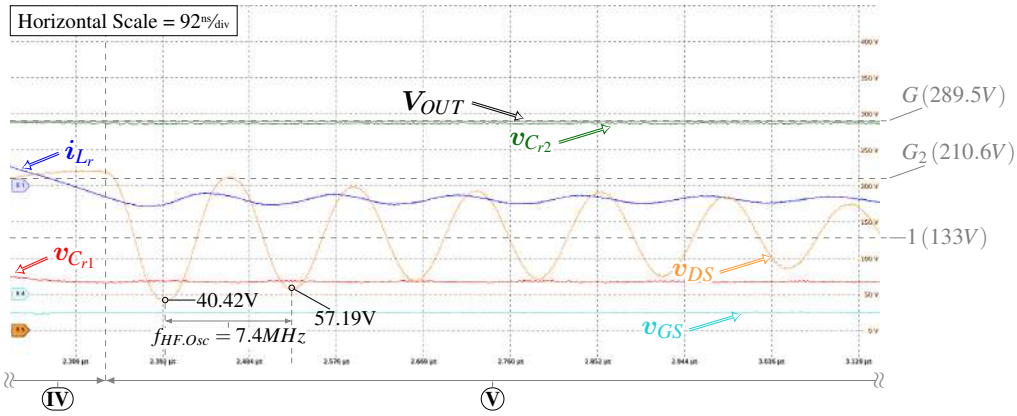
Compared to the Operating Region Ⓘ and Ⓘⓘ, shown in Section 6.0.2.1 and 6.0.2.2, the high-frequency oscillation upon a transition to the Idle States become conditionally more intensified given the initial condition of the Active Switches' drain-to-source voltage upon the turn-ON transition event. This is expected given the large-signal variation based on the 4L-RFLCC's operating condition as validated and shown in Figure 107.

Figure 134a and 134b show the high-frequency oscillation for the Active Switch S_1 and S_3, respectively, in which they correspond to a higher and lower high-frequency oscillation, respectively, due to their initial condition.

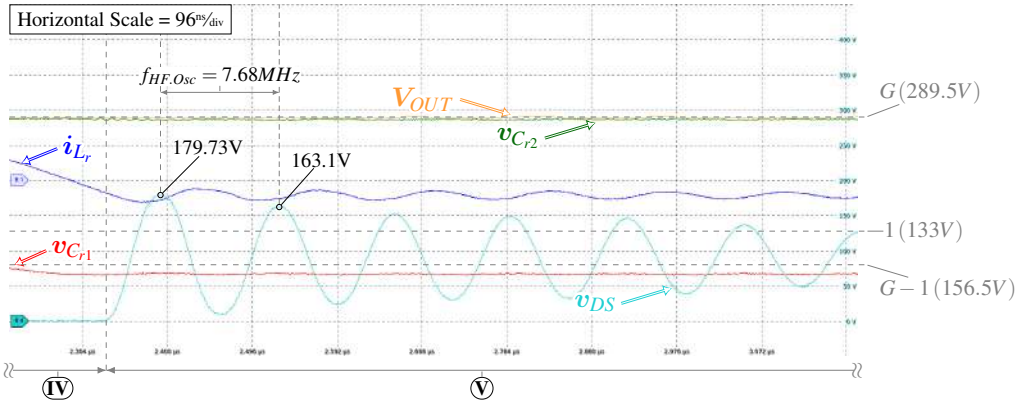
The operating characteristic, and the resonant capacitors' state-trajectory, within the Oper-

Figure 129 – Dynamic Voltage Stresses Experimental Results within Operating Region II and Test Condition ④ upon a transition to the second Idle State for:
(a) Active Switch S_2 .
(b) Passive Switch D_5 .

(a)



(b)



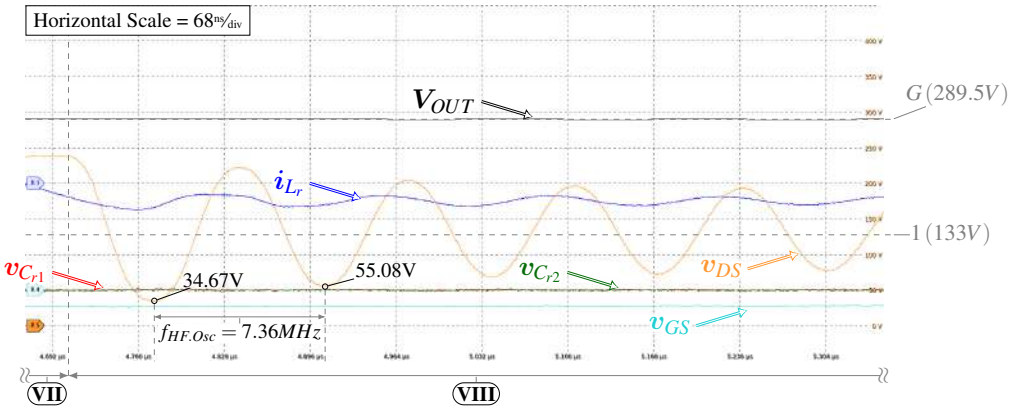
ating Region (III) leads to a non-zero differential voltage within a Flying Capacitor Commutation Cell, which is different from the existing attribute exhibited in the Operating Region (I) and (II). Due to that, within the Transient Events (**11** ↑) and (**31** ↑), it is expected the Switch Pairs $S_3 - D_4$ and $S_1 - D_6$ to encounter a lossy switching transition, respectively.

Within the Operating Region III, the introduced dead-time in between (**x1** ↓) and (**x1** ↑) leads to a more pronounced resonant transient in the two simultaneous OFF-state's Switch Pair. Figure 135 and 136 represents the aforementioned phenomenon for the Switch Pairs $S_1 - D_6$ and $S_3 - D_4$ upon the Transient Events (**31** ↓) and (**11** ↓), respectively.

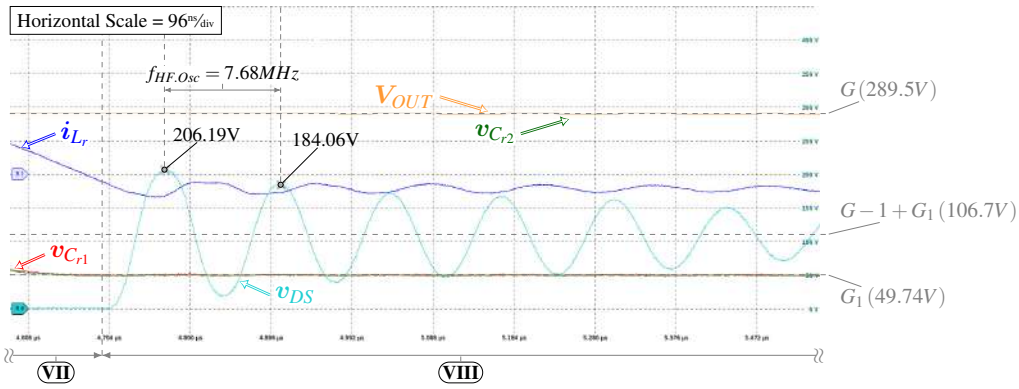
As observed in Figure 133a, the Switch S_2 exhibits a high-frequency oscillatory behavior due to the DCM, during Interval (V). At (**31** ↓), the Switch S_2 remains in OFF-state while the Switch S_1 is turned-OFF, as observed in Figure 135a. As a consequence, the high-frequency oscillation is interrupted and exhibits a shift in its damped oscillatory trajectory due to the Switch Pair $S_1 - D_6$ introduction to the oscillatory trajectory. Within (**31** ↓) and (**31** ↑), the Switch S_1 oscillates according to a voltage divider derived from S_1 and S_2's output capacitance in a series connection. Since S_2 is initially oscillating at a higher voltage level, its output capacitance is

Figure 130 – Dynamic Voltage Stresses Experimental Results within Operating Region II and Test Condition ④ upon a transition to the third Idle State for:
(a) Active Switch S_1 .
(b) Passive Switch D_6 .

(a)



(b)



low, whereas the Switch S_1's output capacitance is considerably higher once it starts oscillating. Therefore, it is expected that Switch S_1 oscillations at a much lower voltage. Simultaneously, the Diode D_6 is also oscillating to maintain the equilibrium within the Flying Capacitor Commutation Cell, as shown in Figure 136b.

Given the oscillatory behavior, upon the Transient Event (**31** ↑), the Switch Pair's output capacitances are charged and discharged with a lower ΔV, which contributes to reduce the charge and discharge losses associated with the devices.

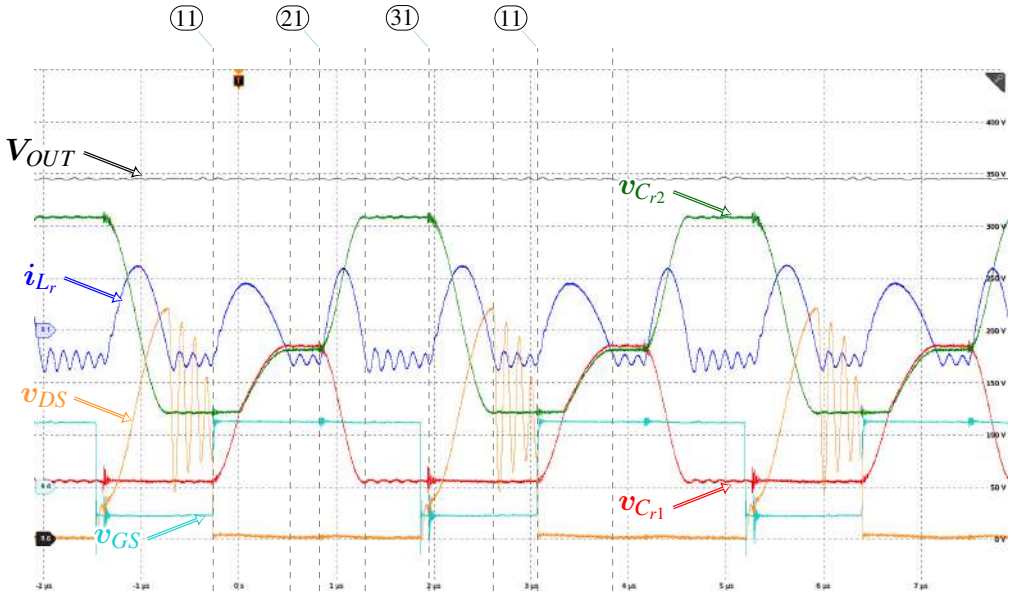
Similarly, the Switch Pair $S_3 - D_4$ undegoes the same behavior as a result of the simultaneous OFF-state from Switch S_1 and S_3, upon the (**11** ↓), as shown in Figure 135b and Figure 136a.

6.0.2.4 Region IV

According to Test Condition (**12**), the Figure 137 show the outermost flying capacitor commutation cell network S_1's and D_6's voltage stresses under CW PWM Sequence, whereas Figure 138 show the innermost flying capacitor commutation cell network S_3's and D_4's voltage

Figure 131 – Switch S_1 and D_6 Voltage Stresses Experimental Results within Operating Region III and Test Condition ⑥:
(a) Active Switch S_1 under Test Condition ⑥.
(b) Passive Switch D_6 under Test Condition ⑥.

(a)



(b)

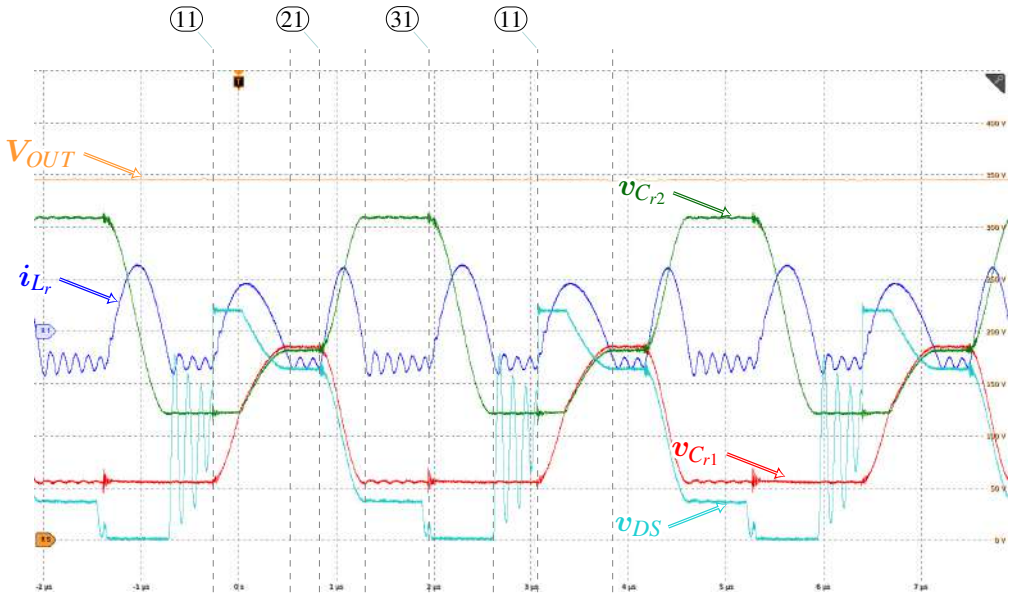
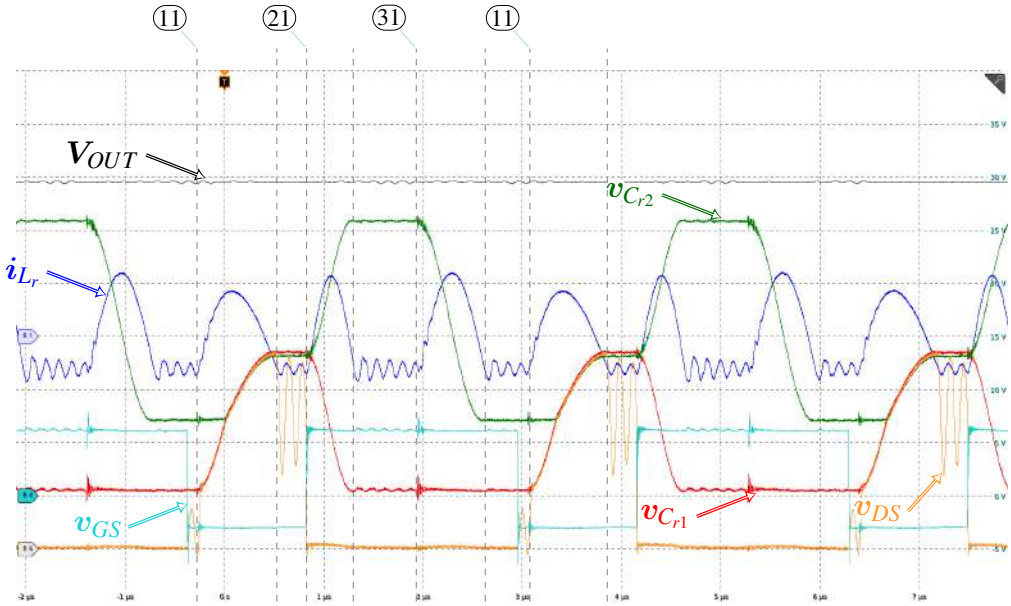


Figure 132 – Switch S_3 and D_4 Voltage Stresses Experimental Results within Operating Region III and Test Condition ⑥:
(a) Active Switch S_3 under Test Condition ⑥.
(b) Passive Switch D_4 under Test Condition ⑥.

(a)



(b)

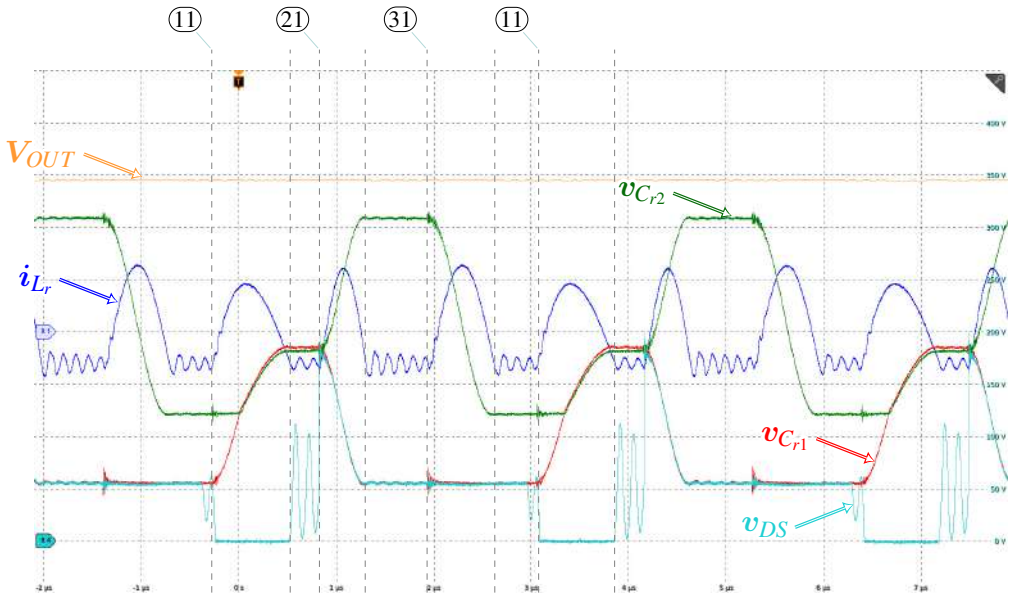
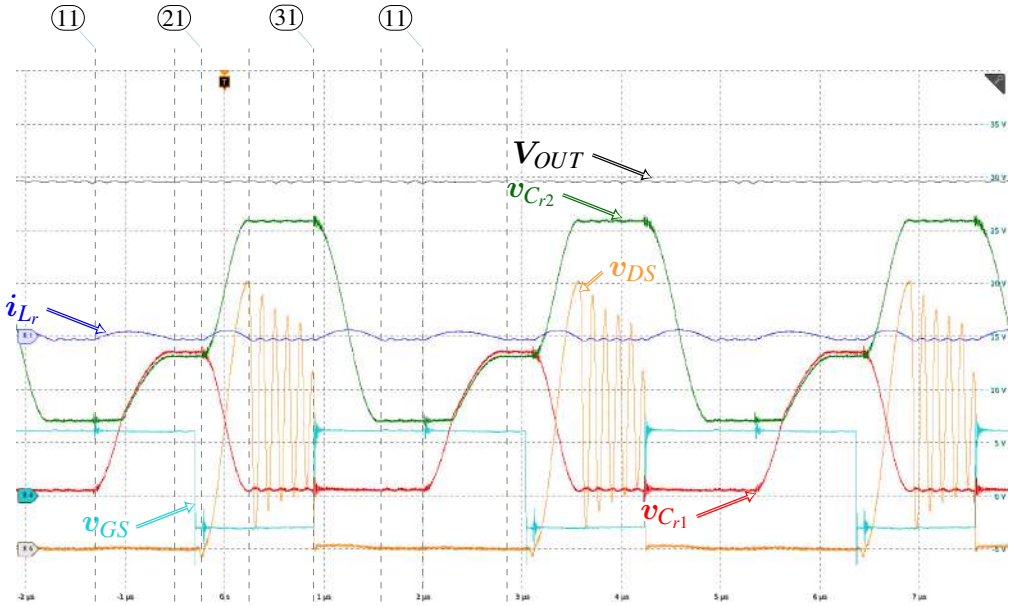


Figure 133 – Switch S_2 and D_5 Voltage Stresses Experimental Results within Operating Region III and Test Condition ⑥:
(a) Active Switch S_2 under Test Condition ⑥.
(b) Passive Switch D_5 under Test Condition ⑥.

(a)



(b)

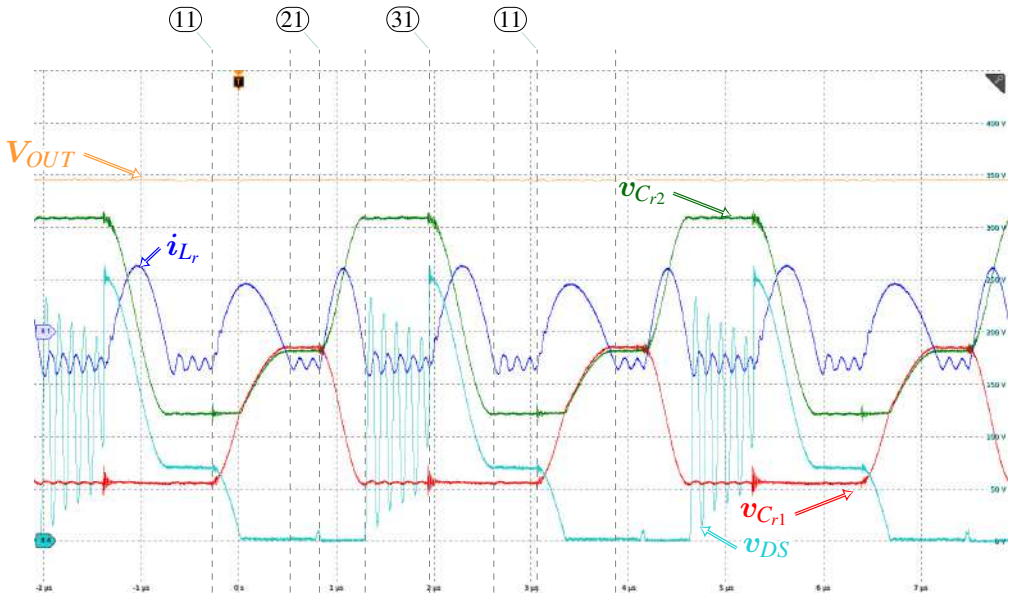
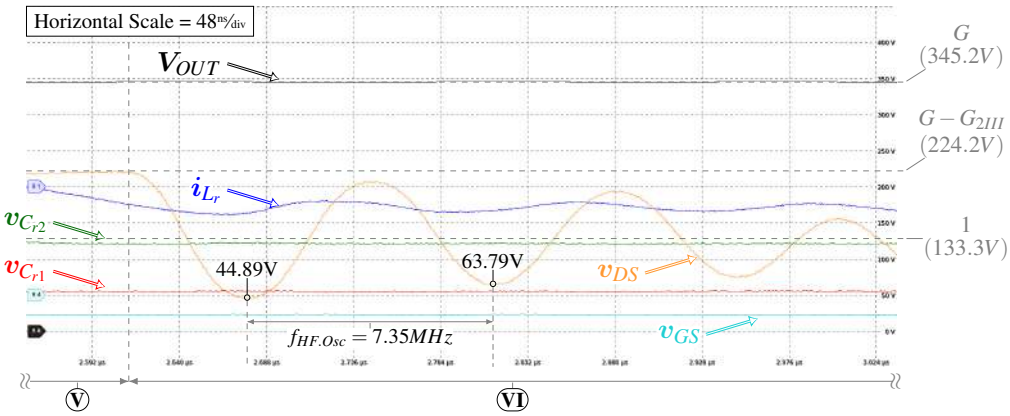
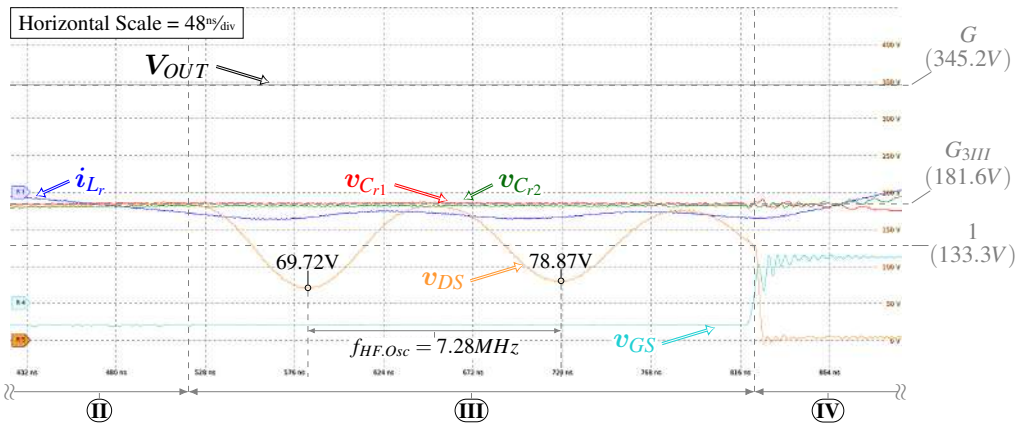


Figure 134 – Dynamic Voltage Stresses Experimental Results within Operating Region III for:
(a) Active Switch S_1 under Test Condition ⑥ upon transition to the Third Idle State with Transition State ㉛.
(b) Active Switch S_3 under Test Condition ⑥ upon transition to the First Idle State with Transition State ⑪.

(a)



(b)



stresses and Figure 139 show the flying capacitor commutation cell network S_2's and D_5's voltage stresses.

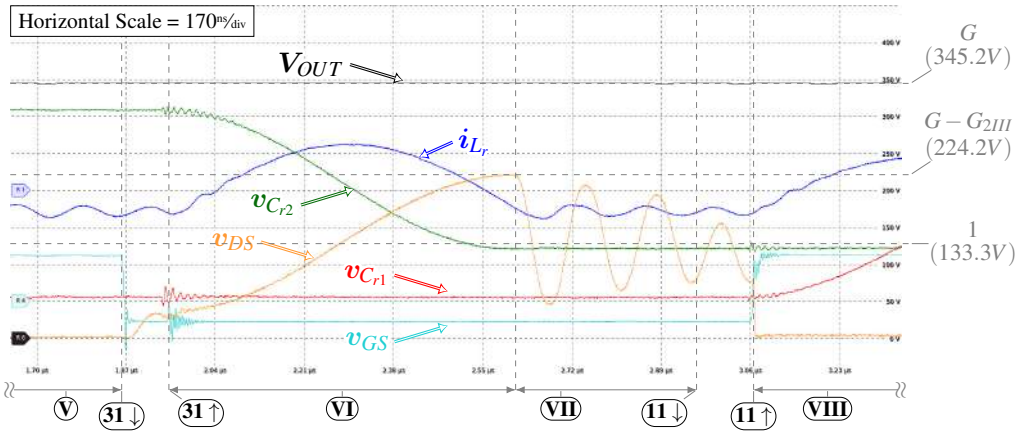
Within Operating Region Ⅳ, and specifically for Test Condition ⑫, the FLCC is fully utilized as the resonant sinusoidal current waveform synchronizes with the switching transitions, securing ZCS transition. Due to that, the high-frequency oscillation is nearly omitted and the dead-time effect is more pronounced.

Similarly as shown in the Test Condition ⑥, the Switch Pair $S_2 - D_5$ does not exhibit the dead-time effect due to its differential voltage at the Switching Transient ㉑, as observed in Figure 139. Additionally, due to the operating characteristic, the Passive Switch D_5 forward-biases under ZVS condition at ㉑↑.

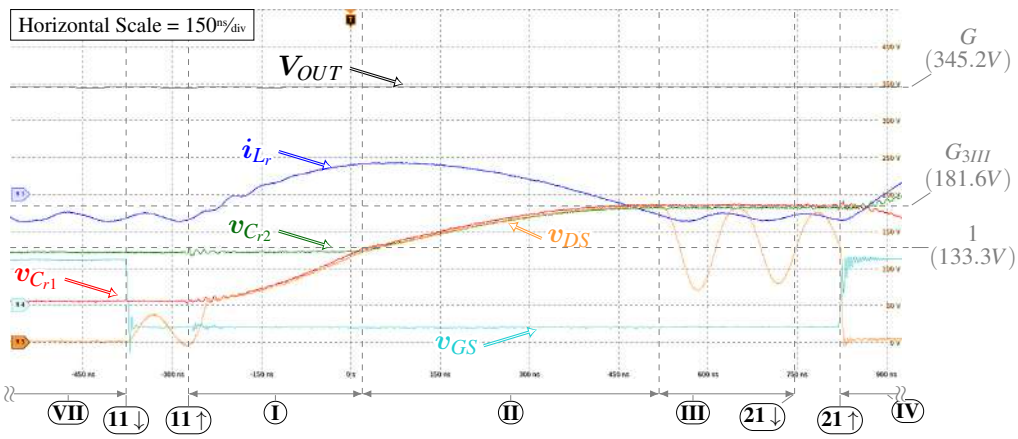
The Switch Pair $S_1 - D_6$, on the other hand, does exhibit a pronounced dead-time effect, as shown in Figure 137, at the Transition Event ⑪. At the instant ⑪↓, Switch S_1 remains in the OFF-state while Switch S_3 is turned-OFF, momentarily shifting the high-frequency resonant oscillation due to the engagement of the Switch Pair $S_3 - D_4$, similarly as exhibited in Test

Figure 135 – Dead-time Dynamic Voltage Sharing Experimental Results within Operating Region III for:
(a) Active Switch S_1.
(b) Active Switch S_3.

(a)



(b)

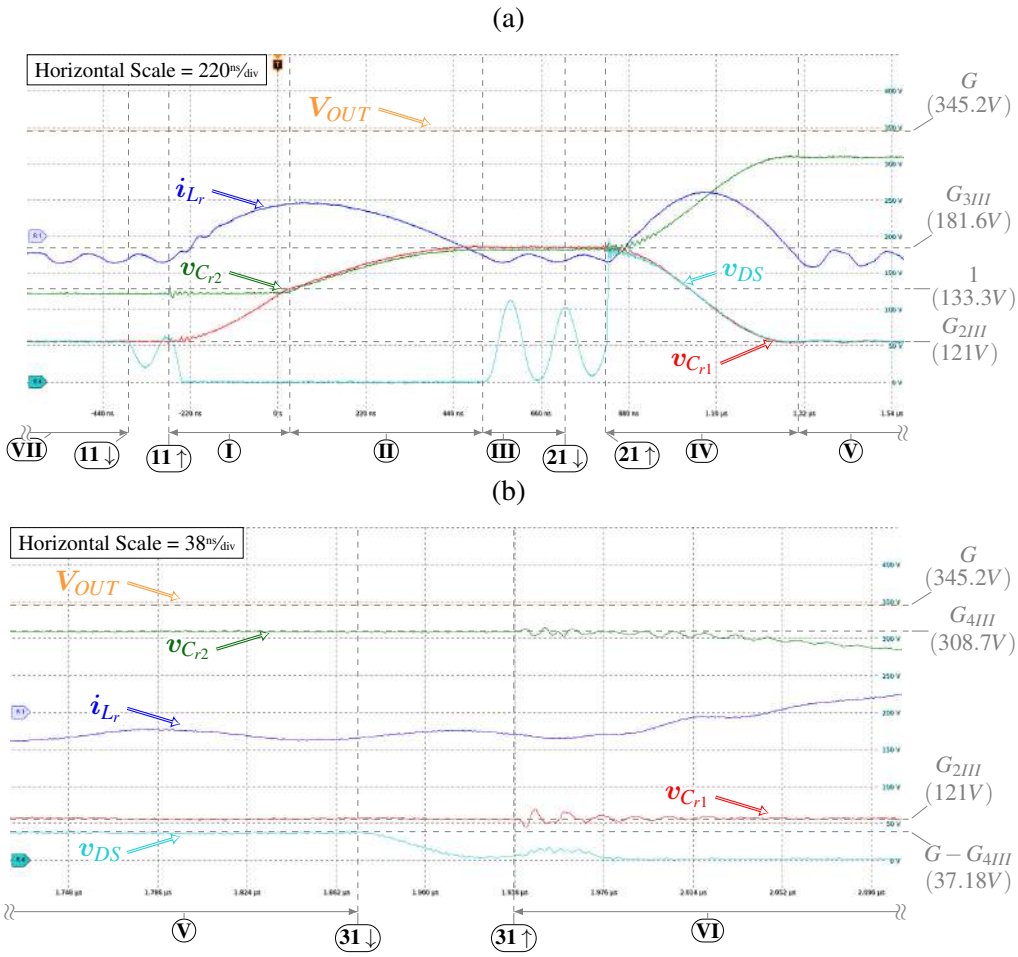


Condition ⑥. Firstly, due to the dead-time introduction, the Switch S_3 anticipates its turn-OFF; Despite of the expected non-ZCS condition, given the resonant tank properties, the Switch S_3 still experiences a ZCS condition. This characteristic is validated due to the instantaneous voltage oscillation in the Diode D_4. The high-frequency oscillation, within the dead-time period, is much more pronounced and surpass the Resonant Capacitor's C_{r_1}'s voltage condition, leading to an unintended Diode D_4 forward biasing event, as shown in Figure 140.

Secondly, the Switch Pair $S_1 - D_6$'s voltage resonates before the Transition Event (**11** ↑), as observed in Figure 141, owing to the ZCS transition being anticipated as a result of the dead-time introduction, prompting a quasi-ZVS condition. As a consequence, reducing the output capacitance's charge and discharge losses, at Transition Event (**11** ↑). This attribute suggests that quasi-ZVS condition is achievable depending on the operating condition even under DCM.

Upon the Transition Event (**11** ↑), the Switch S_1 turns-ON. As a consequence of the step-up excitation and the initial condition for the Switch Pair's voltage, a resonance is derived based on the Switch Pair $S_3 - D_4$ and the resonant inductor L_r, as shown in Figure 142, where

Figure 136 – Dead-time Dynamic Voltage Sharing Experimental Results within Operating Region III for:
(a) Passive Switch D_4.
(b) Passive Switch D_6.



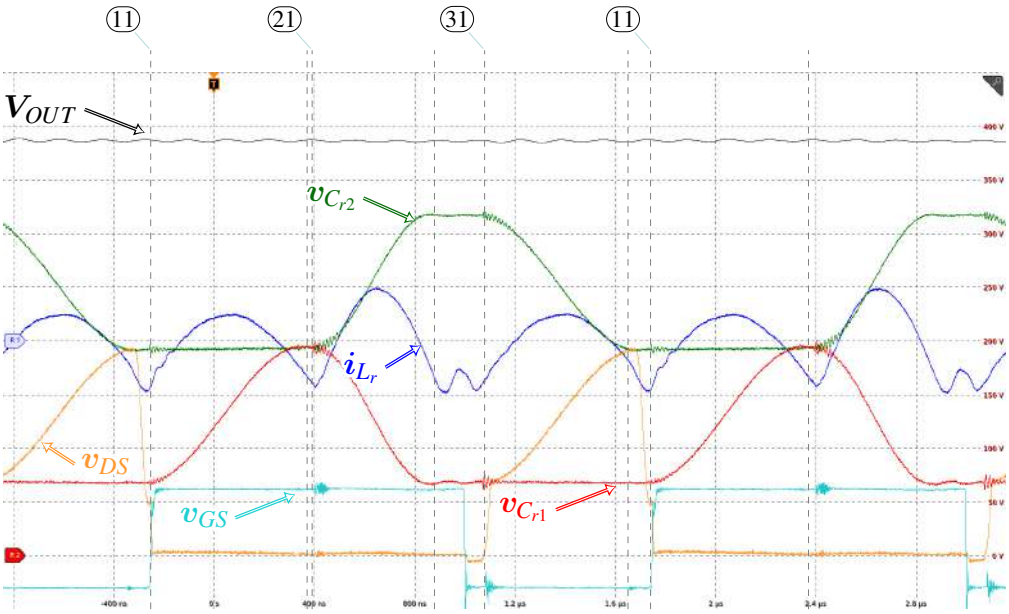
the Active Switch S_3 and Passive Switch D_4's voltage symmetrically increase and decrease, respectively, until the Passive Switch D_4 forward-biases, under ZVS condition. At this moment, the L_r resonant inductor's current is diverged to the Passive Switch D_4, where the nominal resonance ω_0 is derived given the equivalent circuit during Interval (I).

An identical behavior takes place upon Transition Event (31↑), where the Switch Pair $S_1 - D_6$ undergo a symmetrical output capacitance charge and discharge until the Passive Switch D_6 forward-biases under ZVS condition, as depicted in Figure 143 . This process also features a capacitive charge loss within the interval (V).

Differently from the Interval (I), the resonant frequency is higher than ω_0, resulting in an Idle State where the Switch Pair $S_2 - D_5$ exhibits a high-frequency oscillation prior to the Transition State (31↑). The oscillation trajectory is also subjected to a quasi-ZVS condition depending on the triggering point for the aforementioned state. Specifically to the Test Condition (12), the Active Switch S_2 turns-ON close to the second valley, as shown in Figure 144a leading to a reduced turn-ON switching loss.

Figure 137 – Voltage Stresses Experimental Results within Operating Region IV and Test Condition ⑫ for:
(a) Active Switch S_1 under Test Condition ⑫.
(b) Passive Switch D_6 under Test Condition ⑫.

(a)



(b)

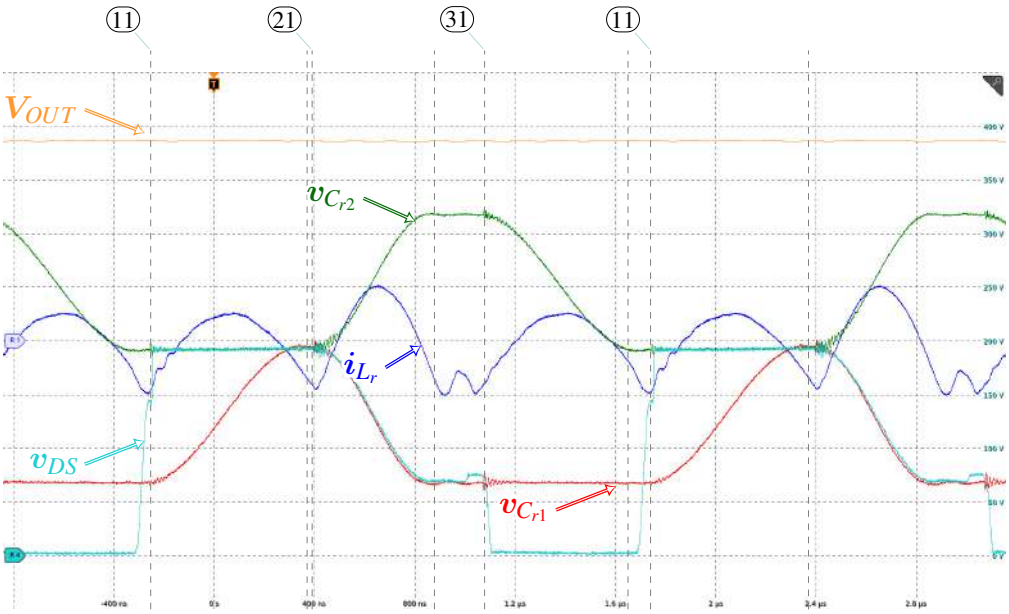
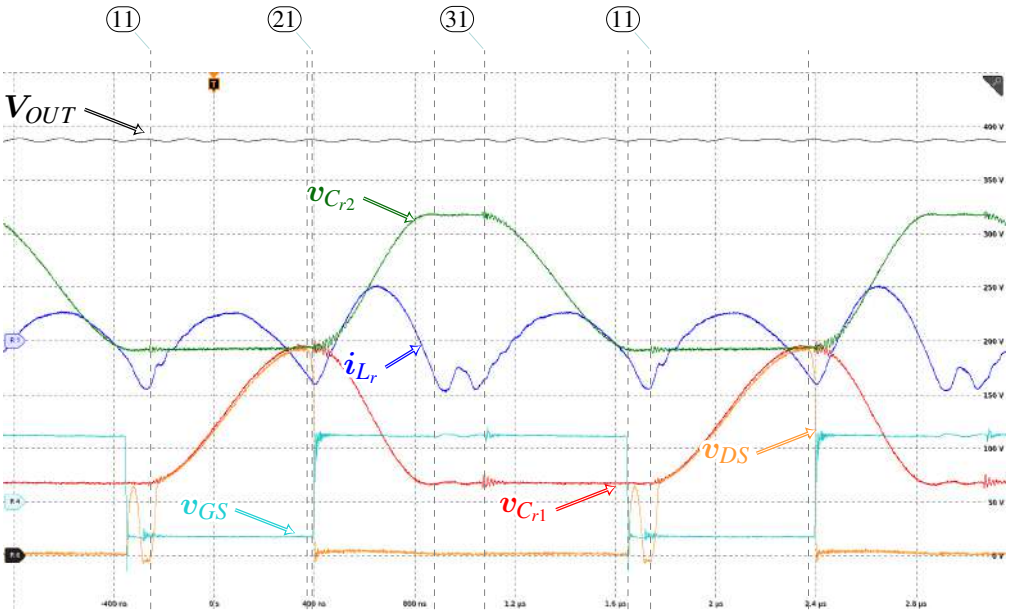


Figure 138 – Voltage Stresses Experimental Results within Operating Region IV and Test Condition ⑫ for:
(a) Active Switch S_3 under Test Condition ⑫.
(b) Passive Switch D_4 under Test Condition ⑫.

(a)



(b)

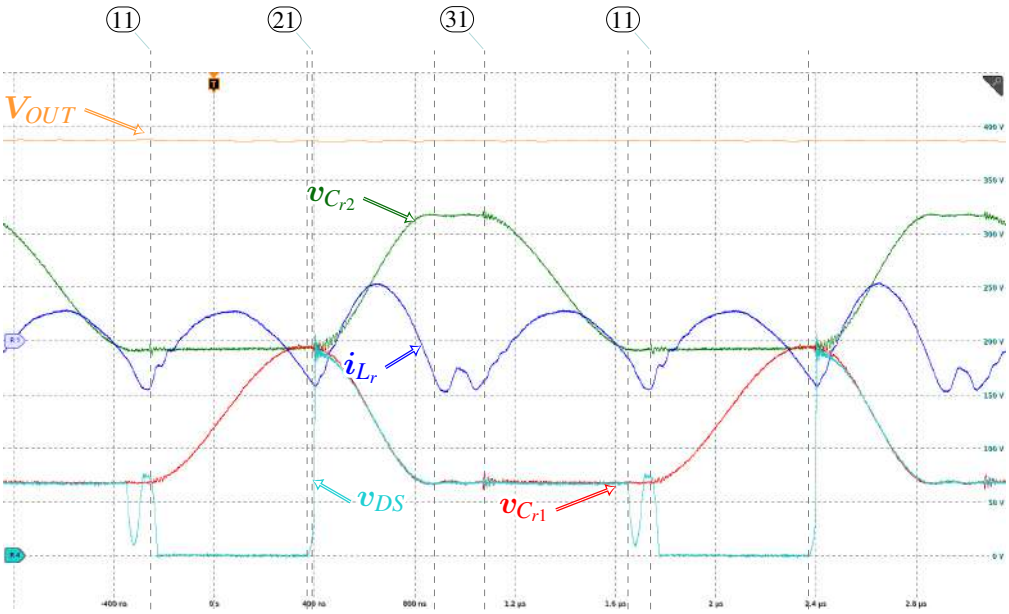
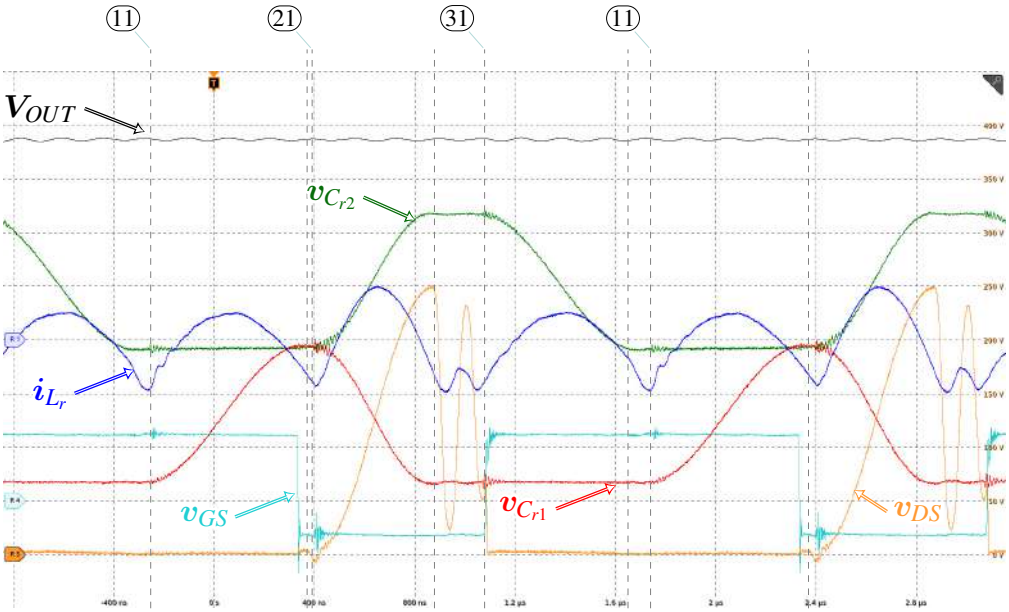


Figure 139 – Voltage Stresses Experimental Results within Operating Region IV and Test Condition ⑫ for:
(a) Active Switch S_2 under Test Condition ⑫.
(b) Passive Switch D_5 under Test Condition ⑫.

(a)



(b)

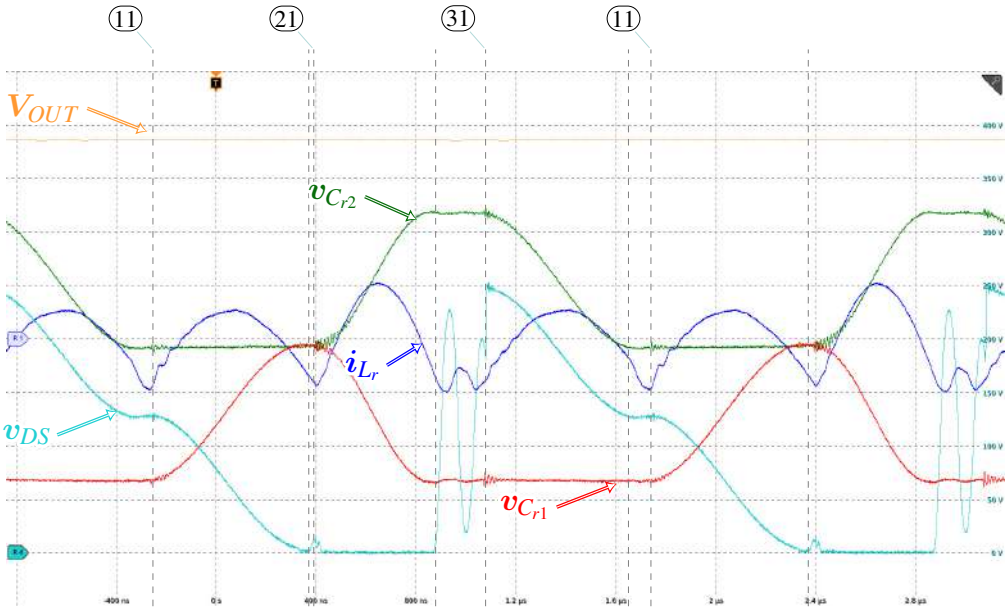
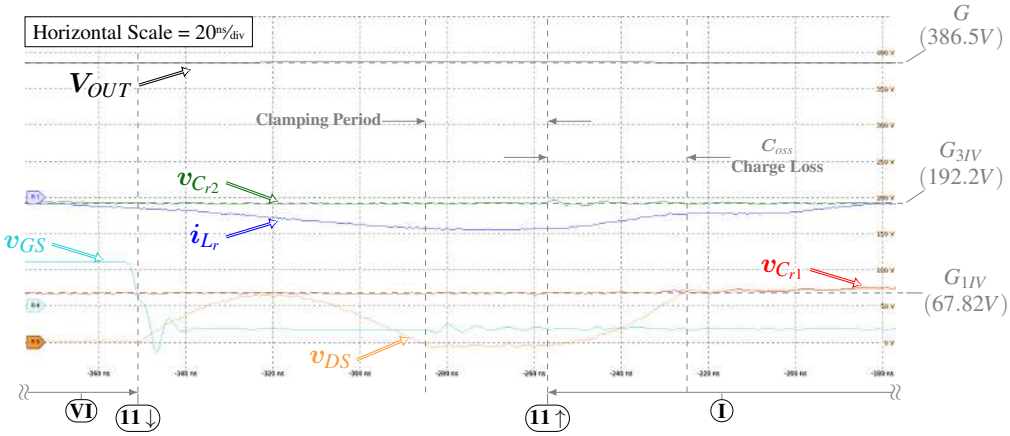


Figure 140 – Dead-time Dynamic Voltage Sharing and Unintended Diode D_4 bias Experimental Results within Operating Region IV for:
(a) Active Switch S_3.
(b) Passive Switch D_4.

(a)



(b)

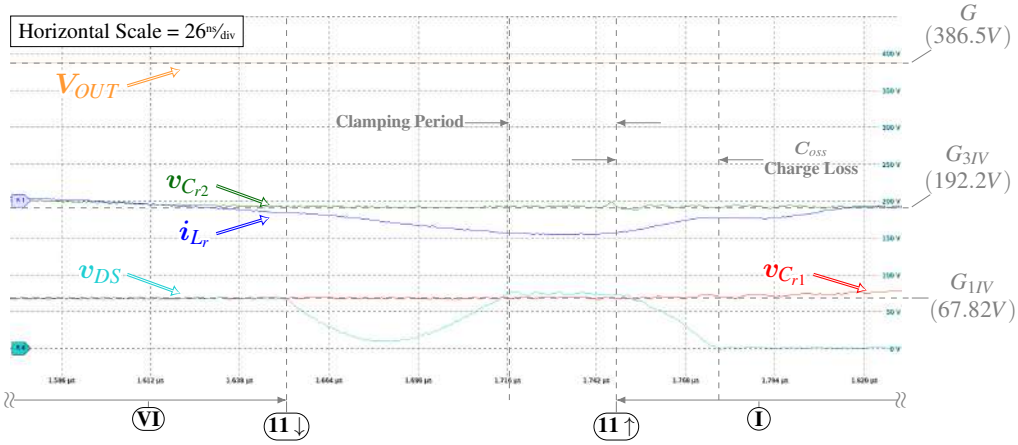
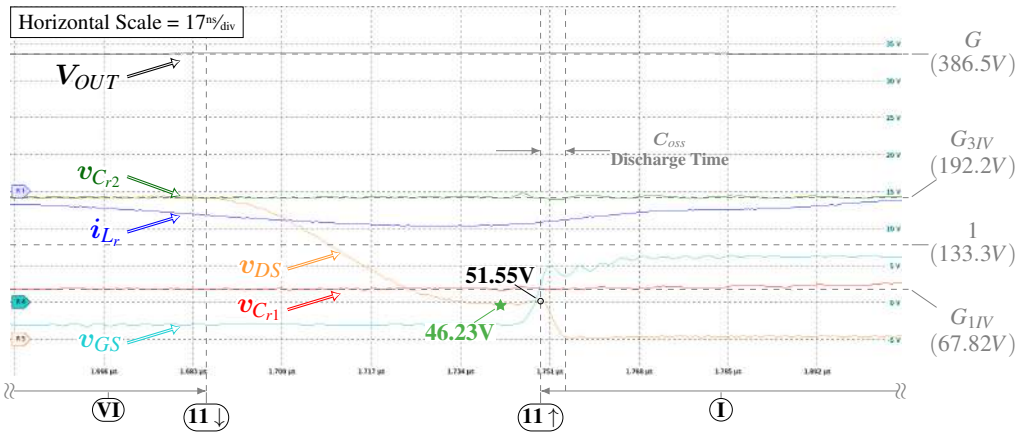


Figure 141 – Experimental Results within Operating Region IV, highlighting a Quasi-ZVS behavior, for:
(a) Active Switch S_1.
(b) Passive Switch D_6.

(a)



(b)

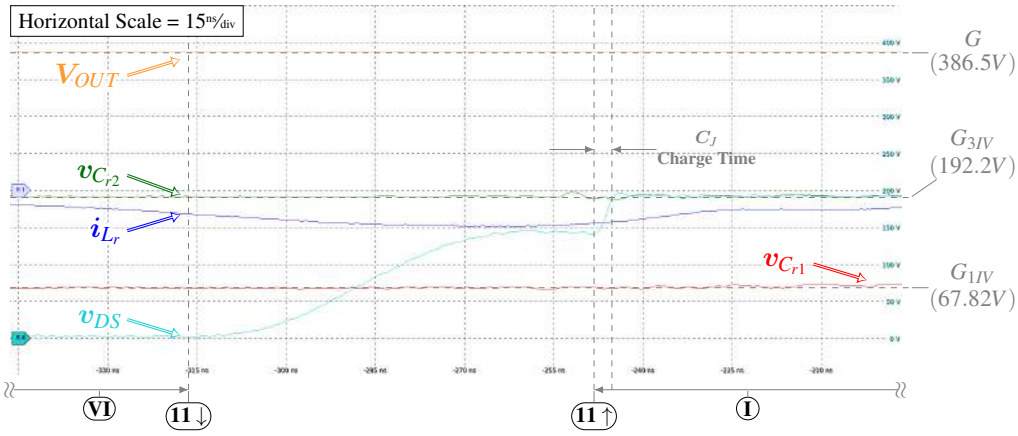


Figure 142 – 4L-RFLCC Non-ideal Equivalent Circuit during the Symmetrical Switch Pair $S_3 - D_4$'s Output Capacitance's charge and discharge, upon Transition State (11↑), originating a capacitive charge loss within Interval (I).

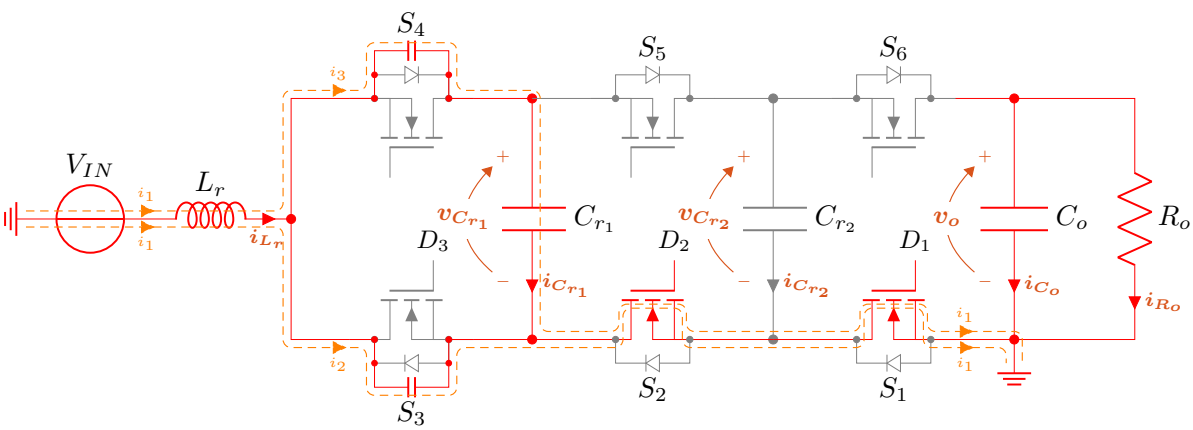


Figure 143 – 4LRFLCC Non-ideal Equivalent Circuit during the Symmetrical Switch Pair $S_1 - D_6$'s Output Capacitance's charge and discharge, upon Transition State (31 ↑), originating a capacitive charge loss within Interval (V).

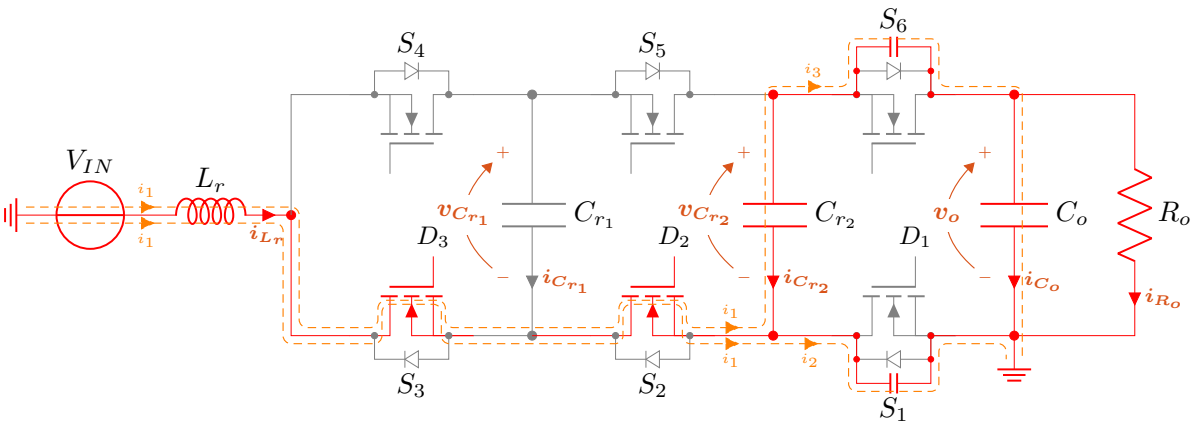
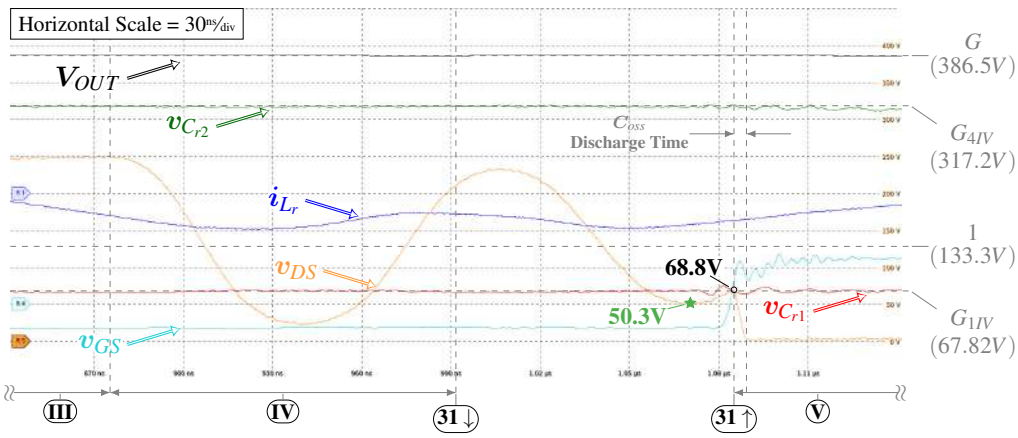
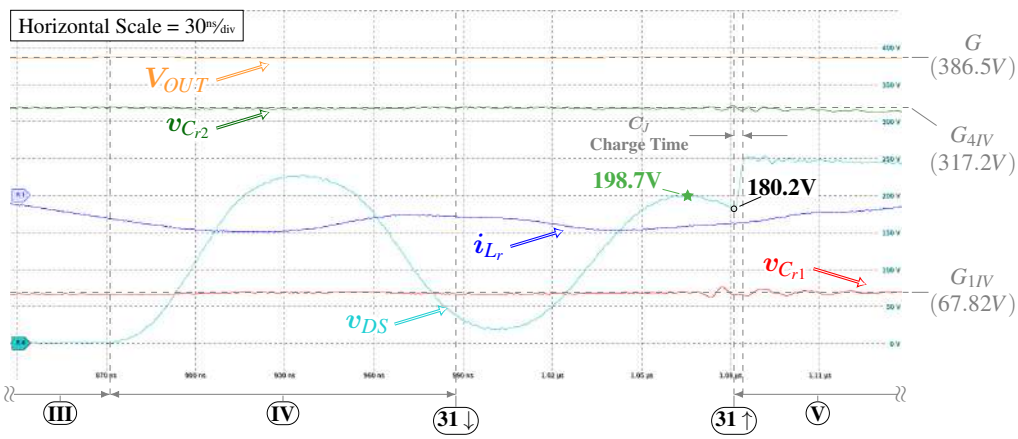


Figure 144 – Experimental Results within Operating Region IV, highlighting a Quasi-ZVS behavior, for:
(a) Active Switch S_2.
(b) Passive Switch D_5.

(a)



(b)



6.0.3 Efficiency Map

The proposed 4L-RFLCC efficiency has been acquired utilizing the same experimental points as shown in Figure 78.

Figure 145 shows the efficiency map as a function of Λ. Since Λ exhibits a duality effect as r_o and μ_o have the same effect, both being correlated to the output load and operating switching frequency, respectively. As seen in the previous Section, the expected current stresses reduces as Λ increases. Therefore, the conduction stress per resonant cycle would be lower. However, it does not translate into a higher conduction losses due to the operating μ_o condition. As a consequence, the highest conduction losses operating condition is a function of μ_o and r_o, not necessarily in the extreme cases. On the other hand, the theoretical switching losses depend on $\Delta V_{C_{r_n}}$ at the Transition State. Due to the DCM's high-frequency oscillation characteristic, the experimental switching losses are not obvious and depend on the dead-time and μ_o condition.

Figure 145 – 500W GaN-based 4L-RFLCC Efficienc Map as a function of Λ with different representations for the R_{OUT} condition.

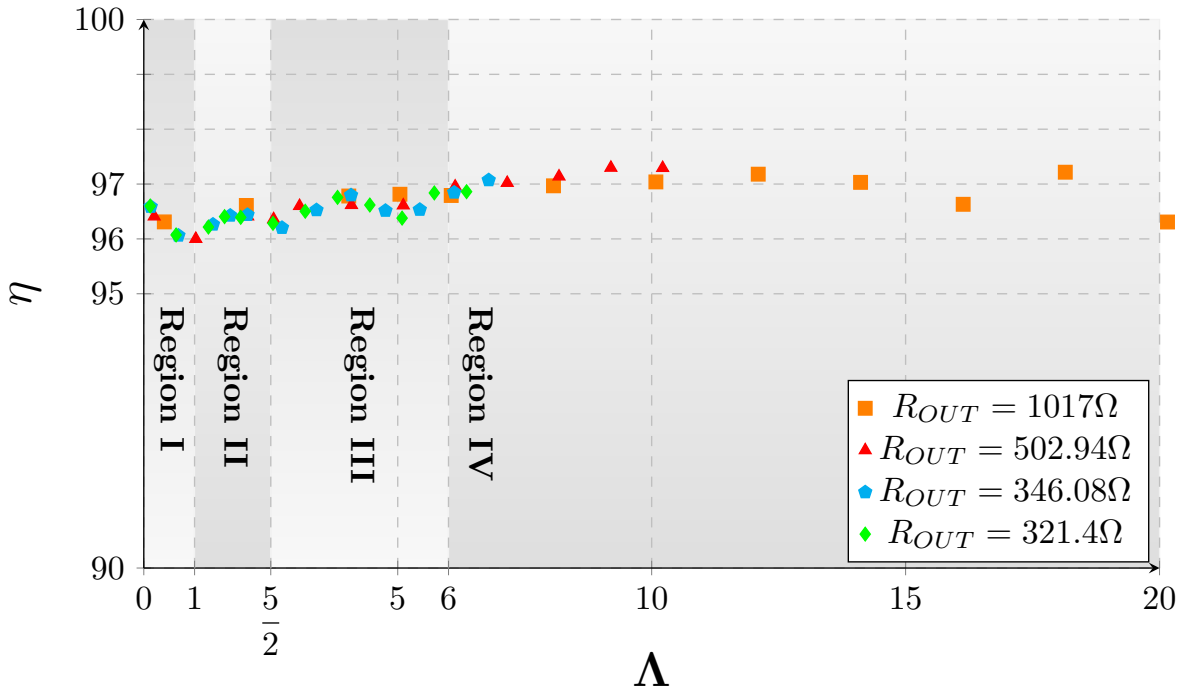
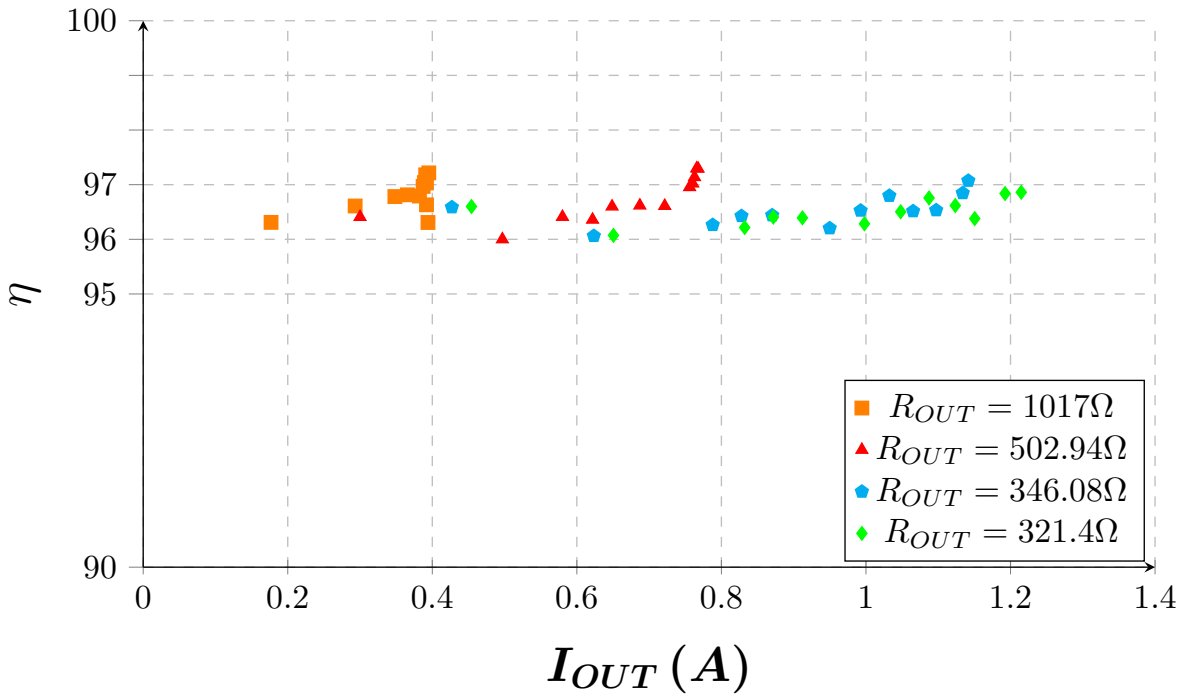


Figure 145 exhibits one characteristic that is worthy-noting. There exist overlapping experimental points, corresponding to similar Λ, that exhibits the same efficiency, suggesting that despite of the higher conduction losses, the switching losses are reduced due to the DCM's valley quasi soft-switching feature.

Alternatively, Figure 146 exhibits the efficiency map as a function of I_{OUT}. Despite of the same intrisic different conditions amongst overlapping points, the efficiency map is also parameterized as a function of R_{OUT}.

The key characteristic is the flat attribute in the efficiency trend which is a good asset for power electronics applications. Another observation is the slight efficiency increase when

Figure 146 – 500W GaN-based 4L-RFLCC Efficienc Map as a function of I_{OUT} with different representations for the R_{OUT} condition.



the converter operates within Operating Region IV, reinforcing the theory about the reduced conduction stresses as well as the quasi soft-switching characteristic.

The peak efficiency was 97.297% under $R_{OUT} = 525\Omega$ and $f_{SW} = 500kHz$ operating condition, followed very close by many different operating points. The efficiency at the highest load condition was 96.86% under $R_{OUT} = 321.4\Omega$ and $f_{SW} = 500kHz$

7 CONCLUSIONS

This work has focused on expanding the assessment of Resonant Flying-capacitor Converter for step-up conversion applications, in which has been theoretically described and validated experimentally, leading to great correlation with exception of a charge-loss which can be associated with the ZCS characteristic. Throughout this work it has been observed there exist a great majority of research focus on low-voltage applications due to the increased demand for telecom, where higher current demands are applicable, as a non-regulated intermediate stage to step-down the voltage with high efficiency and power density. One of the great advantages of such topology is the reduced stresses in the devices and the ability to increase the operating switching frequency given the soft-switching capability, compared to the non-resonant counter-parts.

The 4L-RFLCC introduces several benefits, compared to the 3L-RFLCC, despite of the differences in the maximum conversion ratio. Firstly, the 4L-RFLCC exhibits a considerable reduction in the resonant characteristic impedance, when comparing the same Input Voltage V_{IN} and same Output Power P_{OUT}. Therefore, the resonant tank can be further shrank. Operating Region I has shown to be the most comparable to the 3L-RFLCC as the static gain is in the same range. As a result of the topology modification, the normalized peak current increases but the absolute value decreases due to the reduction in the characteristic impedance. Furthermore, it introduces additional topological steps in order to transfer energy to the Output; leading to a better utilization of the passive and active components. However, in general, the components' utilization are not ideal because of the ladder characteristic, exhibiting some exceptions when the converter is not operating in Region III and IV, where it tends to be most applicable.

Due to the quasi load-independent characteristic, within the Region IV, the RFLCC brings several advantages, compared to other conventional resonant converters, which are associated with the reduced current stresses as well as the possibility to operate under ZVS condition when operating above resonance. The main drawback of operating below the resonance is the non-ZVS condition, which leads to a minimum switching losses that can limit the utilization of such condition for very-high switching frequency applications. Also, it could be associated with EMI issues despite of the great effort in the ZCS conditions being fulfilled. The Large-signal characteristics, within Region IV, have brought several interest as the current and voltage stresses reduce by increasing the operating condition Λ and, despite of the Discontinuous Conduction Mode, it retains the characteristic of decreasing the current stresses, similar to the current stress reduction, under Continuous Conduction Mode, presented by recent works. Thus; suggesting that a comparable efficiency optimization is possible, when comparing to the ZCS condition. As a consequence, the DCM RFLCC become an interesting alternative.

From a different perspective, given the allocation of the resonant tank's characteristic impedance, depending on the optimization object, the RFLCC can also operate as a regulated converter stage; Thus, bringing additional benefits while retaining the soft-switching capability. However, due to its complexity, the Static Gain & Large-Signal Analysis are not as simple

to derive as compared to the Region IV's characteristics due to its full-resonance mode. The complexity presented a not intuitive approach to describe the 4L-RFLCC characteristic, which by utilizing geometrical representations can simplify the process, instead. Additionally, due to the light load characteristic, the 4L-RFLCC loses its ability to regulate the voltage to a lower level, except if duty-cycle control is explored.

By operating the converter under Region I to III, the 4L-RFLCC revealed the possibility to operate under ZCS and ZVS simultaneously due to the C_r voltage coupling as well as C_r coupling to the Output. The ability of the C_r to operate with the same voltage level led to a null differential voltage across the Flying-Capacitor Commutation Cell (FCCC) while retaining the ZCS condition. Despite of this benefit, the current stresses, under these conditions, have shown to be higher, compared to Region IV.

Finally, the experimental results have shown a great correlation with the expected results with an exception due to a unintended charge-loss, which have been associated with the non-ZVS condition as well as the conduction losses in the system. The unintended charge-loss was observed to deviate the operation of the resonant tank, due to the charge/discharge of the Switches Output Capacitance C_{out}. It introduced a effective charge-transfer coefficient loss, when compared to the total charge-transfer within the full resonant cycle. On the other hand, the Discontinuous Conduction Mode has demonstrated a potential utilization of "quasi-resonance" while operating the 4L-RFLCC; Thus, leading to ZCS as well as quasi-ZVS under a wide operating range. As a result, the right allocation of the resonant tank, with the Switches' Output Capacitance can be predominant to achieve such characteristic, specially by intentionally operating the RFLCC under a non-synchronized frequency.

Therefore, based on the literature review, and the topics explored during this work, the following items are considered as contributions:

1. Literature review of the State of the Art within Multi-level Resonant Flying Capacitor and its applications, including gate driving techniques and layout techniques
2. The Static Gain and Large-Signal Description of the 4L-RFLCC
3. The Current and Voltage Stresses analysis, under different operating conditions, for the proposed 4L-RFLCC
4. The introduction of the proposed Design Methodology in a Step-up converter, operating at a higher voltage level condition
5. The exploration of GaN and SiC devices to achieve MHz resonant frequencies
6. The design and validation of the GaN-based 500kHz 4L-RFLCC

whereas topics for future work are considered:

1. Expand the Static Gain and Large-Signal Analysis for operations above resonance under low Λ conditions
2. Expanding the description to n-levels by generalizing the n-RFLCC based on its Static-Gain and Large-Signal characteristics as well as the potential different conduction modes, including below and above resonance
3. Explore the same topology to operate bidirectionally based on High-side Active Devices
4. Explore the optimization objects around the Region IV associated with the characteristic impedance Z_r as well as the quasi-resonant behavior
5. Explore the topology to operate with different control strategies, such as Duty-Cycle Control and Phase-Shift Control as an attempt to reduce the light-load dependency in the voltage regulation characteristic as well as to extend the conversion ratio by "over-modulating"
6. Explore different PCB layout techniques to address the compromise in between Stray Capacitance and Stray Inductance for ZCS operation
7. Compare the performance level in between resonant mode and TCM operation
8. Explore the EMC content while operating the converter abovementioned

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