

Control Strategy for Current Harmonic Programmed AC Active Electronic Power Loads

Joselito A. Heerdt, *Member, IEEE*, Daniel Ferreira Coutinho, *Senior Member, IEEE*, Samir Ahmad Mussa, *Member, IEEE*, and Marcelo Lobo Heldwein, *Senior Member, IEEE*

Abstract—Alternating current (ac) active electronic loads (AELs) based on pulsewidth modulation (PWM) converters, capable of emulating nonlinear loads, require effective current control techniques and power stages. These two aspects of an AEL are interdependent mainly due to the presence of electromagnetic compatibility filters to reduce electromagnetic emissions. However, the filter components affect the dynamics of the system. In this context, this paper proposes a digitally implemented control strategy comprising the state feedback, robust observer, phase-locked loop, and linear current controller to cope with ac AEL applications. The control-oriented modeling and the control system design are presented. Experimental results obtained from a 10-kW three-phase three-level PWM converter prototype illustrate and demonstrate the feasibility of the proposed AEL control strategy.

Index Terms—Alternating current (ac) active load, current control techniques, state feedback, state observers, three-level converters.

NOMENCLATURE

i_a	Equipment under test (EUT) current.
i_A	Filter inductor current.
v_a	Mains or EUT voltage.
v_A	Converter switched voltage.
$v_{C,a}$	Voltage at the filter terminals.
$v_{C,A}$	Voltage across the damping capacitor.
E	DC-link voltage.
L_a	EUT output inductance.
L_A	Converter filter inductance.
L_{aA}	Inductance in case $L_a = 0$.
C_a	Filter capacitor.
C_A	Damping network capacitor.
R_A	Damping network resistor.
S_j	Switch j .
s_j	Switching function of switch S_j .
D_j	Diode j .

$p, n, 0$	DC-link terminals.
j^*	Reference value of j .
j_{pk}	Peak value of j .
f_o	EUT fundamental frequency.
h	Harmonic order (integer).
t	Time.
T_{sw}	Switching period.
f_{sw}	Switching frequency.
f_s	Sampling frequency.
f_o	EUT voltage fundamental frequency.
$\vec{x}$	System state vector.
$\vec{y}$	System output vector.
$\vec{u}$	System input vector.
$\vec{w}$	Disturbance vector.
$\mathbf{A}$	System state matrix.
$\mathbf{B}$	System input matrix.
$\mathbf{C}$	System output matrix.
$\mathbf{D}$	System feedforward matrix.
$\mathbf{I}$	Identity matrix.
$\vec{K}$	State feedback vector.
k_1, k_2, k_3	State feedback gains.
p_1, p_2, p_3	Desired pole location.
$\vec{j}_s, \mathbf{J}_s$	Simplified system vectors and matrices.
$\vec{j}_o, \mathbf{J}_o$	Luenberger observer vectors and matrices.
$\hat{j}$	Estimated value of j .
$\mathbf{M}$	Luenberger observer gain matrix.
$C(s)$	Current controller.
k_c	Current controller gain.
k_{sf}	State feedback common gain.
d	Duty cycle.
k	Sampling number.

I. INTRODUCTION

BURN-IN routines, equipment operation test during research and development phases, and maintenance procedure are among the test procedures that take advantage from active electronic loads (AELs). Regarding alternating current (ac) AELs, the equipment that potentially profit from testing with ac AEL are the following: distribution transformers, power system protection equipment, transmission lines, ac regulators, generators, energy measurement devices, uninterruptible power supplies (UPSs), and others. Such testing procedures promote energy savings [1]. An example is presented in [2], where an economic analysis shows that an electronic load that regenerates energy to the grid can have its payback time in less than five months.

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J. A. Heerdt is with the Electrical Power Processing Research Group (nPPE), Department of Electrical Engineering (DEE), Santa Catarina State University (UDESC), 89223-100 Joinville-SC, Brazil (e-mail: jaheerdt@joinville.udesc.br).

D. F. Coutinho is with the Department of Automation and Systems (DAS), Federal University of Santa Catarina (UFSC), 88040-970 Florianópolis-SC, Brazil (e-mail: daniel.coutinho@ufsc.br).

S. A. Mussa and M. L. Heldwein are with the Department of Electronics and Electrical Engineering (EEL), Federal University of Santa Catarina (UFSC), 88040-970 Florianópolis-SC, Brazil (e-mail: samir@inep.ufsc.br; heldwein@inep.ufsc.br).

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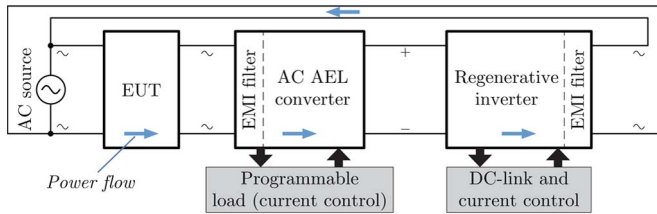


Fig. 1. Simplified single-phase equivalent block diagram of an ac AEL composed of an AEL converter and a regenerative inverter that feeds power back to the ac source.

Nonlinear loads connected to distribution networks generate harmonic currents that do not add to their active power due to the frequency mismatch with the grid voltage. However, their circulation through feeders produces Joule losses and electromagnetic (EM) emissions. This creates harmful effects. In this context, each equipment that is subject to distorted currents is required to withstand the additional requirements produced by such currents. Therefore, test setups including the injection of high amplitude harmonic currents into energy supply equipment are able to provide close to real application conditions. These setups could use dedicated nonlinear in addition to linear loads or use ac AELs with programmable harmonic currents to emulate field applications.

AC AELs as illustrated in Fig. 1 can be implemented through different technologies and with various objectives (see Appendix A). The basic blocks of an ac AEL are a power source, an electronic converter that drains power from the EUT, and a regenerative inverter that feeds power back to the power source to increase test efficiency.

There are several works related to the emulation of ac loads through electronic power converters. For instance, an AEL based on a three-phase diode rectifier fed by a three-phase ac-side transformer was proposed in [3] to generate distorted test currents. However, no explicit control was used, and the load characteristics could not be programmed. An approach based on a linear amplifier was proposed in [4], which presents high control bandwidth but poor efficiency. This poses limitations for the testing of high-power equipment. A hybrid amplifier approach, i.e., the connection of a linear amplifier with a switched circuit, is proposed for AELs in [5] to increase the current control bandwidth with higher efficiency. A proportional-integral (PI)-type current controller was considered in [6] to generate current distortion in a three-phase switched inverter-based ac AEL. This approach leads to even higher efficiency. On the other hand, switch mode AELs generate high frequency (HF) emissions and are more complex from the control perspective.

The active ac load based on switch mode power converters option leads to several benefits and must be considered. Potential benefits are as follows [2]: low energy consumption and reduction of peak power demand due to mains energy reinjection, installation cost reduction due to lower cooling requirements when compared with linear amplifier-based AELs, and smaller test equipment footprint because resistive loads are not employed. In addition, an active ac load is easily scalable, is highly flexible regarding changing current test profiles, and provides dynamic testing capability, i.e., the reference currents can be programmed. A dynamic electronic load simulator (DELS) for

ac power supplies was briefly described in [7] without detailing the used current controller. Wang *et al.* [8] propose the use of a resonant plus P-type current controller to reduce reference tracking errors. However, they do not include an *LCL* filter configuration, which dramatically increases the current control challenge. A repetitive controller is employed in [9] for a similar power circuit as in [8] also for an *L* type of filter. A single inductor (*L* filter) is again used in [10] to couple EUT and a pulsewidth modulation (PWM) inverter-based electronic ac load. This configuration injects relevant HF current contents in the EUT or requires very large inductors, which are both non-desirable. Thus, electromagnetic compatibility (EMC) filters should be employed in order to prevent HF current components from circulating in the tested device. Typical filters would lead to *LC* or *LCL* configurations [11]–[15].

An *LCL* filter is a reasonable approach regarding overall filter volume, weight, and cost, but it adds resonances to the circuit that should be handled by the inverter control system. Furthermore, the tested device output impedance changes the control plant as well. Thus, a robust control system should be designed. De Sousa *et al.* [16] propose an ac AEL that is employed to test power distribution transformers. The topology uses an input *LCL* filter followed by a standard three-phase inverter. It is shown that the resonant behavior of practical *LCL* filters with low damping is quite challenging for controlling the inverter. The solution given in [16] proposes a damping resistor in series with the filter capacitor. However, this reduces the capacitor filtering effect regarding HF current components, leading to the oversizing of the filter components and/or poor EMC filtering performance. Chang *et al.* [17] propose an *LCL* single-phase PWM inverter-based DELS that is employed for operational and burn-in tests for ac and dc power supplies emulating linear *RLC*-type loads. The current controller employs a full-order system state feedback, and a 2-kHz control bandwidth was obtained with 50-kHz switching frequency.

This paper proposes a control strategy suitable for a switch mode ac AEL. The ac AEL is based on a modern power electronics three-level converter, and the proposed control strategy is shown to be able to cope with the added challenges of an *LCL* filter with high grid interfacing inductance values. The final objective is to reproduce a given current harmonic profile. The application focus is placed on the testing of distribution transformers that are subject to heavy harmonic pollution, namely, the testing of K-rated transformers and harmonic mitigating transformers, among others. The proposed control design approach for this system employs the state-space description, which is the basis for a state feedback strategy aiming to mitigate the influence of the *LCL* filter on the controlled plant. The eigenvalues of the system are chosen to provide active damping, and a control law for the closed-loop system leads to a control bandwidth of approximately 11 kHz with 66-kHz switching frequency. The EUT current, i.e., the grid interface transformer current, is not directly measured. Therefore, the *LCL* filter can be segregated and shielded from all electronic components in the converter layout. However, the current to be controlled is ideally the current on the EUT side, i.e., through the inductor located at the grid side. Another option would be to sense both currents as in [17], but this adds

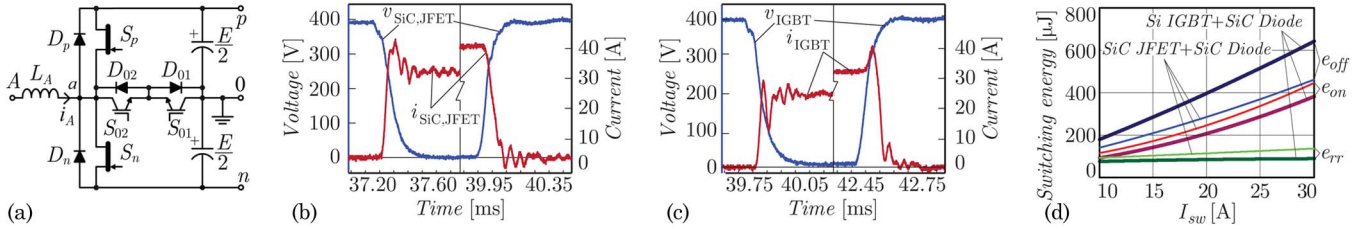


Fig. 2. (a) One of the phases (phase A) of a four-wire three-level bidirectional TCC converter. (b) Switching test voltage and current at the 1.2-kV SiC JFET $v_{SiC,JFET}$. (c) Switching test voltage and current at the 600-V Si insulated-gate bipolar transistor (IGBT) v_{IGBT} . (d) Measured switching losses.

cost and tends to worsen the filter performance regarding the EM emissions. In the proposed control system, a Luenberger observer (cf. Section IV-B) provides information regarding the EUT current that is indirectly estimated and controlled. The observer gains are chosen based on a robust H_∞ formulation that minimizes the influence to external disturbance errors. A comprehensive control design example illustrates the proposed design procedure.

Even though the current control of the LCL -based converter has been widely analyzed in the literature [11], [12], [14], [18]–[23], the challenge with an ac AEL is fundamentally different since high-performance EUT current control must be achieved. In addition, this requires the knowledge of the EUT-side filter currents, which is not the case in most of the proposed LCL control schemes.

This paper is structured as follows. The ac AEL three-level power converter prototype is described in Section II, and its control-oriented model is detailed in Section III. The proposed control strategy is explained in Section IV. Finally, experimental results are given in Section V, and Section VI ends this paper. A classification for AEL systems is presented in Appendix A. Finally, a guideline for the dc-link voltage choice of an ac AEL is proposed in Appendix B.

II. AC AEL POWER CONVERTER DESCRIPTION

The switching cells of traditional bidirectional three-level voltage source converters, such as the neutral point clamped (NPC) [24], [25] and the flying capacitor [26]–[28], are typically employed as three-level inverters. These topologies are commonly rated for very high power (hundreds of kilowatts up to megawatts), and the use of such structures as bidirectional converters in the lower kilowatt range is not widespread in industrial applications. However, ac AELs present a potential application for such converters since the size of the ac-side filter can be reduced for a given switching frequency (f_{sw}) due to the lower values of the voltage steps at the converter ac-side terminals. Fig. 2(a) shows a three-level transistor-clamped converter (TCC) topology that presents the same external characteristics of the NPC. However, two of the switches per phase are subject to the full dc-link voltage [29], [30]. This topology presents the potential for reducing the total losses when compared to the NPC for low voltage (< 1 kV) applications [31], [32]. Thus, it is employed as the basis for the modeled three-phase ac AEL. As other three-level topologies, the converter at hand might lead to unbalances at the partial dc-link voltages. In the proposed implementation, the balance should be provided by a downstream converter connected to the mains in order to regenerate energy

during EUT testing. A four-wire connection to an EUT is considered in the following. Thus, all circuit and control diagrams consider noncoupled single-phase variables. The four-wire connection is based on the model of an EUT that is a hypothetical distribution transformer with Y windings. This is a typical case for three-phase transformers feeding single-phase nonlinear loads, where the triplen harmonics add up in the neutral cable.

The built three-phase converter laboratory prototype is shown in Fig. 3. Switches $S_{01} - D_{01}$ and $S_{02} - D_{02}$ employ 600-V Si IGBTs (IRF IRG4PC50W) and Si Stealth diodes (Fairchild ISL9R3060G2). The full dc-link voltage is chosen at 800 V. Thus, 1.2-kV normally off SiC JFETs (SemiSouth SJEP120R063) and SiC diodes (SemiSouth SDP30S120) are used for $S_p - D_p$ and $S_n - D_n$. Relatively low switching losses [31] are obtained as shown in Fig. 2(b)–(d). The main circuit specifications are as follows: rated power (for purely sinusoidal balanced currents) $P_{rated} = 10$ kW, line-to-line rms voltage $V_{l-l} = 380$ V, and dc-link voltages $E/2 = 400$ V (see Appendix B). The computed semiconductor losses for the converter operating at rated conditions as a unit power factor rectifier are as follows: switching losses $P_{sw} \cong 60$ W and conduction losses $P_{cond} \cong 87$ W.

The converter modulation is an in-phase disposition (IPD) scheme. The appropriate steps between the transitions of the switching signals, i.e., a logic sequence that prevents short circuit at any instant, are employed as presented in [31].

Filtering is required between the EUT and the converter to limit EM emissions from the AEL. The use of step-up power converters requires that inductors are used to implement a current source characteristic at the ac side of the converter. However, if only an L -type filter was used, the volume and weight of such filter would be very large. In addition, large inductance values limit the achievable control bandwidth. Thus, a second-order LC filter leads to much reduced passive component dimensions and weight. It leads to reduced inductance that potentially increases converter dynamics. On the other hand, the added capacitance leads to a resonance that can be minimized with passive or active (lossless) damping. In addition, common-mode emission filtering must also be included in the filter. Thus, the filter configuration in Fig. 3(a) is used. This can be seen as an LC filter since the common-mode inductor L_{CM} leakage inductance is typically small. However, this paper considers an LCL filter configuration (see Fig. 4) due to the presence of a nonnegligible output inductance for the EUT. The EMC filter design is not within the scope of this paper since it requires information on the complete test setup. References on the design of EMC filters for high-switching-frequency three-level converters are given in [33]–[35]. The filter parameters are

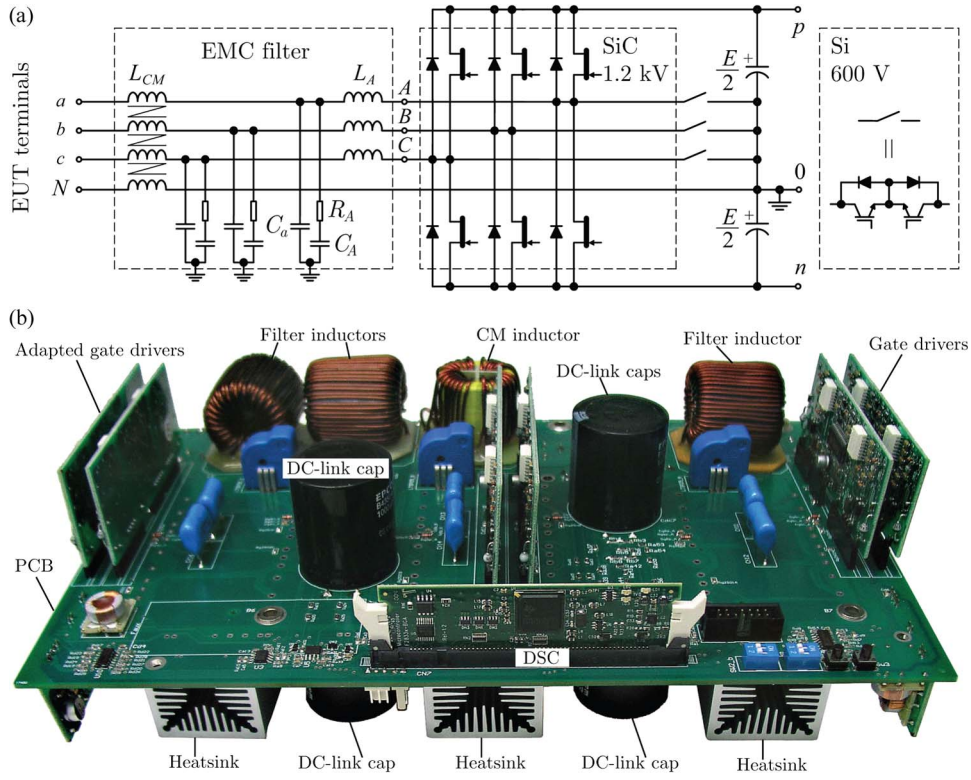


Fig. 3. Built three-phase TCC converter laboratory prototype. Dimensions: ($\cong 300 \times 185 \times 105$) mm.

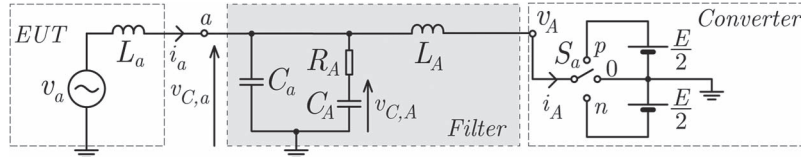


Fig. 4. Phase “a” equivalent circuit used for the control-oriented modeling of the three-phase ac AEL. Only four-wire EUTs are considered, and the neutral is connected to terminal 0.

$L_A = 420 \mu\text{H}$, $C_a = 1 \mu\text{F}$, $R_A = 33 \Omega$, and $C_A = 1 \mu\text{F}$. The EUT output inductance is assumed for designing reasons to be unknown but bounded to a given interval

$$L_a \in [L_a^{\min}, L_a^{\max}], \quad L_a^{\min} = 380 \mu\text{H}, \quad L_a^{\max} = 570 \mu\text{H} \quad (1)$$

with $\bar{L}_a = 456 \mu\text{H}$ being its nominal level. This leads to a strong resonance close to 10 kHz.

III. CONTROL-ORIENTED MODEL

The converter model is obtained through the equivalent circuit depicted in Fig. 4 following the procedure described in [36]. The EUT is considered with a voltage source characteristic followed by inductor L_a that models the leakage inductance of a transformer under test and includes the leakage inductance of the common-mode inductor L_{CM} in Fig. 3. The EMC filter presents the interface inductor L_A , the filter capacitor C_a , and a damping network $R_A - C_A$ that is used to provide minimum passive damping [37]. The dc-link voltages are considered to be regulated by a downstream converter that also balances the partial voltages to $E/2$.

The converter switching functions describing the state of the switch S_a are $s_a = +1$ if S_a is connected to the p terminal, $s_a = -1$ if it is connected to n , and $s_a = 0$ if it is connected

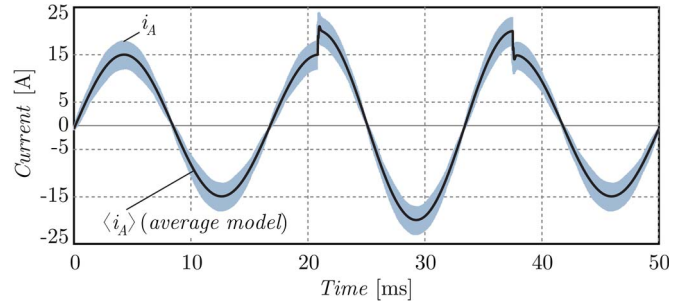


Fig. 5. Comparative analysis between the switched model (i_A) current and the state-space average ($\langle i_A \rangle$) current for a simulated single-phase converter in current control with a simple PI controller in closed-loop operation. Circuit parameters: $L_a = 500 \mu\text{H}$, $L_A = 420 \mu\text{H}$, $C_a = 1 \mu\text{F}$, $R_A = 33 \Omega$, $C_A = 1 \mu\text{F}$, $E = 400 \text{ V}$, $f_{sw} = 40 \text{ kHz}$, $v_a = V_{pk} \sin(\omega t)$, $V_{pk} = \sqrt{2}110 \text{ V}$, $\omega = 2\pi f_o$, and $f_o = 60 \text{ Hz}$. A reference step from 15 to 20 A and back is applied during the time interval from 20.83 to 37.5 ms.

to 0. The local average value of voltage v_A , i.e., that obtained by state-space averaging, is defined with $\langle v_A \rangle = d_a(E/2)$, where $d_a = \{-1, +1\}$ is the duty cycle of switch S_a .

The following state-space description is obtained by considering the local average values of the circuit voltages and currents:

$$\begin{aligned} \dot{\vec{x}} &= \mathbf{A}\vec{x} + \mathbf{B}\vec{u} \\ \dot{\vec{y}} &= \mathbf{C}\vec{x} + \mathbf{D}\vec{u} \end{aligned} \quad (2)$$

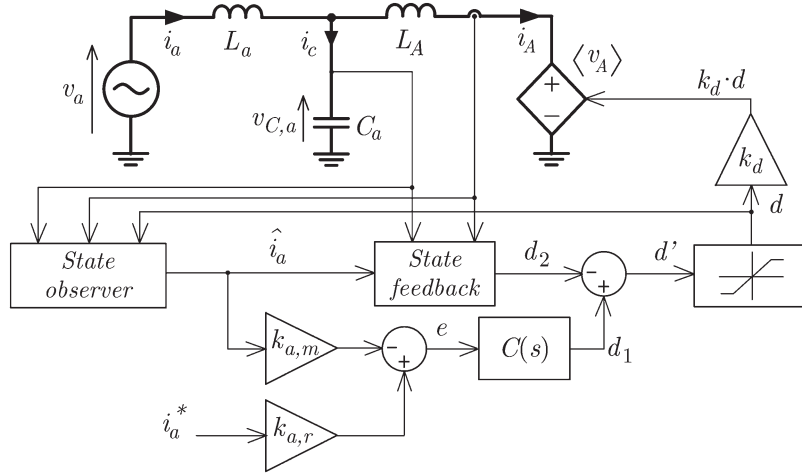


Fig. 6. AC AEL current control block diagram.

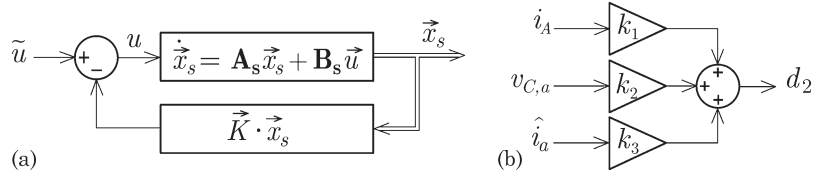


Fig. 7. AC AEL state feedback block diagram.

where

$$\vec{x} = [i_a \ i_A \ v_{C,a} \ v_{C,A}]^T \quad (3)$$

$$\vec{u} = [v_a \ d_a]^T \quad (4)$$

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & -1/L_a & 0 \\ 0 & 0 & 1/L_A & 0 \\ 1/C_a & -1/C_a & -1/(R_A C_a) & 1/(R_A C_a) \\ 0 & 0 & 1/(R_A C_A) & -1/(R_A C_A) \end{bmatrix} \quad (5)$$

$$\mathbf{B} = \begin{bmatrix} 1/L_a & 0 \\ 0 & -E/(2L_A) \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad \mathbf{C} = [1 \ 0 \ 0 \ 0] \quad (6)$$

Fig. 5 shows simulation results that validate the described average model by comparing the obtained grid-side current with that of a switched circuit model.

IV. CONTROL STRATEGY

The proposed control strategy block diagram for the modeled ac AEL is shown in Fig. 6. The converter current i_A and the filter capacitor voltage $v_{C,a}$ are the measured variables. A state observer based on the converter duty cycle d and the two measured variables estimates the EUT-side current $\hat{i}_a$. The state observer is used in order to not add extra current sensors to the power circuit. EUT-side current sensors might deteriorate EMI filter performance due to noise coupling from the control electronics and add cost to the system. The filter damping branch $R_A - C_A$ is neglected since it helps to reduce the dynamic requirements at the resonant peak and only adds complexity for the system analysis. The LCL filter resonance is actively damped through the use of a state feedback. Finally, the EUT current error e is compensated through a current controller $C(s)$ (cf. Section IV-C). The main control blocks are explained in the following.

A. Active Damping Through State Feedback

State feedback is a pole placement technique that reallocates the original poles of the controlled system in a way that the closed-loop system presents a desired dynamic behavior. The states i_a , $v_{C,a}$, and i_A are here used. A linear combination of these states generates signal d_2 in Fig. 6. This technique does not change the number of poles nor the position of the original zeros of the system.

The model described in (2)–(6) is reduced by eliminating the damping components R_A and C_A . Thus, the simplified system used for the control design is

$$\dot{\vec{x}}_s = \mathbf{A}_s \vec{x}_s + \mathbf{B}_s \vec{u} \quad (7)$$

where

$$\vec{x}_s = [i_a \ i_A \ v_{C,a}]^T \quad (8)$$

$$\mathbf{A}_s = \begin{bmatrix} 0 & 0 & -1/L_a \\ 0 & 0 & 1/L_A \\ 1/C_a & -1/C_a & 0 \end{bmatrix} \quad (9)$$

$$\mathbf{B}_s = \begin{bmatrix} 1/L_a & 0 \\ 0 & -E/(2L_A) \end{bmatrix}^T \quad (10)$$

The state feedback implementation is seen in Fig. 7, where $\vec{K} = [k_1 \ k_2 \ k_3]^T$. From Fig. 7(a), it follows that

$$\dot{\vec{x}}_s = [\mathbf{A}_s - \mathbf{B}_s \vec{K}] \vec{x}_s + \mathbf{B}_s \vec{u}. \quad (11)$$

Hence, the closed-loop characteristic equation is as follows:

$$\det[s\mathbf{I} - (\mathbf{A}_s - \mathbf{B}_s \vec{K})] = 0. \quad (12)$$

Assuming that the desired characteristic equation is defined by three real poles p_1 , p_2 , and p_3 , the following is obtained:

$$s^3 - (p_1 + p_2 + p_3)s^2 + (p_3(p_1 + p_2) + p_1 p_2)s - p_1 p_2 p_3 = 0. \quad (13)$$

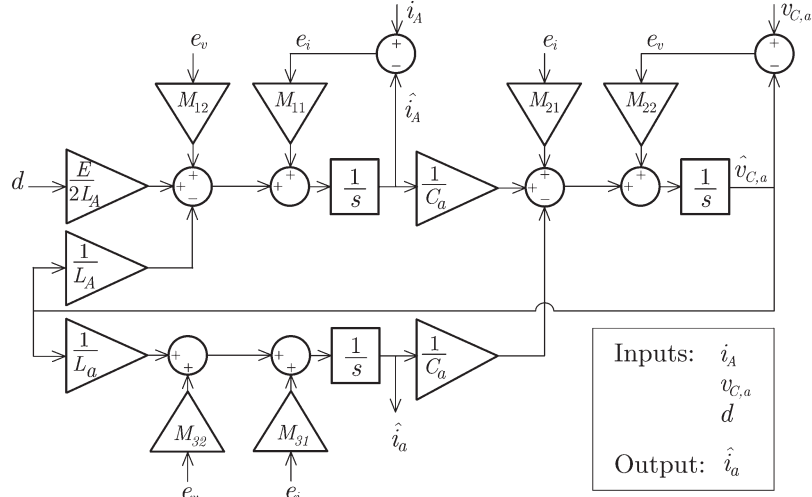


Fig. 8. AC AEL Luenberger state observer block diagram.

Solving the system including (12) and (13) gives

$$k_1 = -\frac{2L_A}{E} \cdot (p_1 + p_2 + p_3) \quad (14)$$

$$k_2 = \frac{2L_A C_a}{E} \left[(p_1 p_2 + p_2 p_3 + p_3 p_1) - \frac{L_a + L_A}{C_a L_a L_A} \right] \quad (15)$$

$$k_3 = -k_1 - 2 \frac{(p_1 p_2 p_3) L_a L_A C_a}{E}. \quad (16)$$

B. State Observer

The EUT-side current i_a is estimated by means of a Luenberger state observer [38]. The observer gain is designed based on the robust H_∞ formulation as proposed in [39] and [40]. Precisely, the gain of the correction term (i.e., the error between the measurements and their estimate) is designed in order to minimize the effects of external disturbances as well as the errors due to model inaccuracy on the estate estimation.

In light of the uncertainty on the value of L_a , we recast the system dynamics in terms of a disturbance vector $\vec{w}$ comprising exogenous signals and modeling errors

$$\begin{aligned} \dot{\vec{x}}_s &= \bar{\mathbf{A}}_s \vec{x}_s + \mathbf{B}_{s1} d_a + \mathbf{B}_{s2} \vec{w} \\ \vec{y} &= \mathbf{C}_s \vec{x}_s \end{aligned} \quad (17)$$

where $\bar{\mathbf{A}}_s$ is the matrix $\mathbf{A}_s$ evaluated at $L_a = \bar{L}_a$ and

$$\mathbf{B}_{s1} = \begin{bmatrix} 0 \\ -\frac{E}{2L_A} \\ 0 \end{bmatrix}, \quad \mathbf{B}_{s2} = \begin{bmatrix} \frac{1}{L_a} & \delta L_a \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad \vec{w} = \begin{bmatrix} v_a \\ v_{C,a} \end{bmatrix} \quad (18)$$

with δL_a representing a bounded uncertainty which models the error between $1/L_a$ and $1/\bar{L}_a$.

Then, the Luenberger observer is defined as follows:

$$\dot{\vec{\xi}} = \bar{\mathbf{A}}_s \vec{\xi} + \mathbf{B}_{s1} d_a + \mathbf{M}(\vec{y} - \vec{y}_\xi) \quad (19)$$

$$\vec{y}_\xi = \mathbf{C}_s \vec{\xi} \quad (20)$$

$$\vec{\eta} = \mathbf{C}_\eta \vec{\xi} \quad (21)$$

$$\vec{\xi} = [\xi_1 \ \xi_2 \ \xi_3]^T \quad (22)$$

where $\vec{\eta}$ is the signal to be estimated and $\mathbf{M}$ is a constant matrix to be determined.

Let $\vec{e} := \vec{x}_s - \vec{\xi}$ and $\vec{\eta}_e := \mathbf{C}_\eta \vec{x}_s - \vec{\eta}$ be the estimation error vector and the observation error, respectively. Thus, the estimation error dynamics can be cast by means of

$$\dot{\vec{e}} = (\mathbf{A}_s - \mathbf{M} \mathbf{C}_s) \vec{e} + \mathbf{B}_{s2} \vec{w} \quad (23)$$

$$\vec{\eta}_e = \mathbf{C}_\eta \vec{e}. \quad (24)$$

The observer gain matrix $\mathbf{M}$ is designed aiming to mitigate the effects of external disturbances and modeling errors on the estimation $\hat{i}_a$ of i_a by minimizing the following cost function:

$$\min_{\mathbf{M}} \left\{ \sup \frac{\|\vec{\eta}_e\|_2}{\|\vec{w}\|_2} \right\} \quad (25)$$

for all L_a belonging to the interval $[L_a^{\min}, L_a^{\max}]$.

The results proposed in [39] and [40] are applied for the gain determination. The optimization problem in these references is recast in terms of linear matrix inequality constraints [41], which are numerically solved with appropriate software [42]. This approach leads to

$$\mathbf{M} = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \\ M_{31} & M_{32} \end{bmatrix} = 10^6 \cdot \begin{bmatrix} 1.9525 & -0.2007 \\ -0.3356 & 0.1028 \\ 1.9665 & -0.2049 \end{bmatrix}. \quad (26)$$

Then, the complete observer structure as illustrated in Fig. 8 can be written as follows:

$$\begin{bmatrix} \frac{d\hat{i}_A}{dt} \\ \frac{d\hat{v}_{C,a}}{dt} \\ \frac{d\hat{i}_a}{dt} \end{bmatrix} = \mathbf{A}^\circ \cdot \begin{bmatrix} \hat{i}_A \\ \hat{v}_{C,a} \\ \hat{i}_a \end{bmatrix} + \mathbf{B}^\circ \cdot \begin{bmatrix} d \\ i_A \\ v_{C,a} \end{bmatrix} \quad (27)$$

where

$$\mathbf{A}^\circ = \begin{bmatrix} -M_{11} & \frac{-1}{L_A} - M_{12} & 0 \\ \frac{1}{C_a} - M_{21} & -M_{22} & \frac{-1}{C_a} \\ -M_{31} & \frac{1}{L_a} - M_{32} & 0 \end{bmatrix} \quad (28)$$

$$\mathbf{B}^\circ = \begin{bmatrix} \frac{E}{2L_A} & M_{11} & M_{12} \\ 0 & M_{21} & M_{22} \\ 0 & M_{31} & M_{32} \end{bmatrix} \quad (29)$$

and the estimation error vector is $\vec{e} = [e_{i_A} \ e_{v_{C,a}} \ e_{i_a}]^T$.

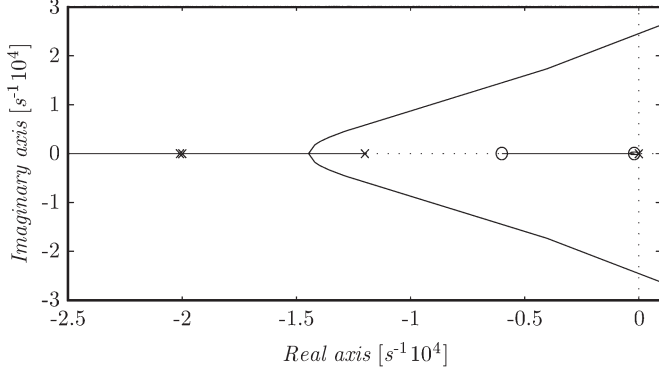


Fig. 9. Root locus of the controlled system including the plant, the current controller, and the state feedback. Circuit parameters: $L_a = 500 \mu\text{H}$, $L_A = 420 \mu\text{H}$, $C_a = 1 \mu\text{F}$, $R_A = 33 \Omega$, $C_A = 1 \mu\text{F}$, and $E = 400 \text{ V}$.

C. Current Controller

Two integrators are employed in order to provide improved current reference following capability for the circuit to perform its ac AEL function. Two zeros, one at -200 rad/s and the other at $-6 \cdot 10^3 \text{ rad/s}$, are included in order to position the poles of the system as presented in Fig. 9. The root locus presented in Fig. 9 considers the state feedback and a current controller $C(s)$ defined as

$$C(s) = k_c \frac{s^2 + 6.2 \cdot 10^3 s + 1.2 \cdot 10^6}{s^2}. \quad (30)$$

Poles are at the origin, $-20 \cdot 10^3 \text{ rad/s}$ and $-12 \cdot 10^3 \text{ rad/s}$. The placement considered an upper bound at one-tenth of the switching frequency to guarantee a reliable performance.

D. Digital Control Issues and Implementation

The previous analysis and design parameters were performed considering continuous implementations of all system blocks. However, it is well known that the digital implementation of the control and modulation blocks might bring further challenges to the control performance and stability. The main influences of digital implementations are related to analog-to-digital (AD) conversion, computation time, and sampling frequency. The main effects are typically modeled through transport delays. An example is the simulated dynamic response seen in Fig. 5, which is obtained with the proposed control strategy without considering the digital implementation issues and a switching frequency of $f_{sw} = 40 \text{ kHz}$. Such dynamic response is not possible when the AD delay and a double update mode modulation scheme are used. Increasing the sampling frequency allows to improve this situation. For instance, a sampling frequency of 160 kHz allows to increase the precision of the proposed observer and improve the dynamic response close to the continuous time one. However, a large sampling frequency increases the noise levels mainly at the current measurement due to the approximation of sampling instants to switching instants. Furthermore, the delay associated to the updating of the duty cycle is not reduced. Thus, the straightforward way to obtain the expected dynamic behavior is to increase the switching frequency. Computer simulation studies to evaluate the effects of the digital implementation were carried out. The

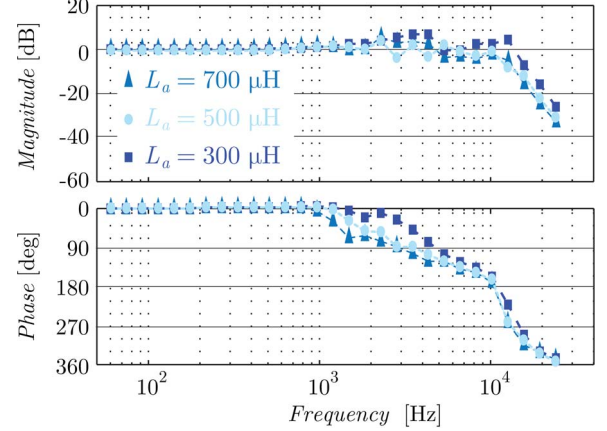


Fig. 10. Closed-loop Bode diagram of the controlled system resulting from computer simulations including the power circuit and the main digital control blocks, i.e., delays, quantization, sample and hold, PWM with double update mode, and the complete control structure. Circuit parameters: $L_a = 300, 500, 700 \mu\text{H}$; $L_A = 420 \mu\text{H}$; $C_a = 1 \mu\text{F}$; $R_A = 33 \Omega$; $C_A = 1 \mu\text{F}$; and $E = 400 \text{ V}$. It is important to notice that, according to Appendix B, the peak current reference for higher harmonic frequencies is decreased. For the case at hand, the current peak reference was linearly decreased from 15 A at 60 Hz down to 1 A at 30 kHz .

simulation model includes the following: quantizers and zero-order-hold blocks to emulate the effect of the AD converter in the current and voltage sensors, an IPD modulation scheme employing the double update PWM mode to guarantee noise-free samples, limiters to model saturation effects in the control loops, and the discrete implementation of all presented control blocks. An analysis of the AEL switching frequency on the performance of the current reproduction was done based on the simulation results, and a switching frequency of $f_{sw} = 66 \text{ kHz}$ was chosen, leading to a sampling frequency of $f_s = 132 \text{ kHz}$.

The control laws are discretized based on the chosen switching frequency with the help of Matlab and are described in the following discretized models.

The current controller is defined with

$$d_1(k) = k_c [2917e(k) - 5700e(k-1) + 2783e(k-2)] + 2d_1(k-1) - d_1(k-2) \quad (31)$$

where $k_c = 1.5 \cdot 10^{-5}$ is the current controller gain and k refers to the sampling number.

The employed state feedback discrete model expression is

$$d_2(k) = k_{sf} [54.705 \cdot 10^{-3} i_A(k) + -3.673 \cdot 10^{-3} v_{C,a}(k) - 52.172 \cdot 10^{-3} i_a(k)] \quad (32)$$

where $k_{sf} = 0.6$ is the state feedback gain.

Finally, the future states of the observer are

$$\begin{aligned} \hat{i}_A(k+1) &= A_{11}^o \hat{i}_A(k) + A_{12}^o \hat{v}_{C,a}(k) + A_{13}^o \hat{i}_a(k) \\ &\quad + B_{11}^o d(k) + B_{12}^o i_A(k) + B_{13}^o v_{C,a}(k) \\ \hat{v}_{C,a}(k+1) &= A_{21}^o \hat{i}_A(k) + A_{22}^o \hat{v}_{C,a}(k) + A_{23}^o \hat{i}_a(k) \\ &\quad + B_{21}^o d(k) + B_{22}^o i_A(k) + B_{23}^o v_{C,a}(k) \\ \hat{i}_a(k+1) &= A_{31}^o \hat{i}_A(k) + A_{32}^o \hat{v}_{C,a}(k) + A_{33}^o \hat{i}_a(k) \\ &\quad + B_{31}^o d(k) + B_{32}^o i_A(k) + B_{33}^o v_{C,a}(k). \end{aligned} \quad (33)$$

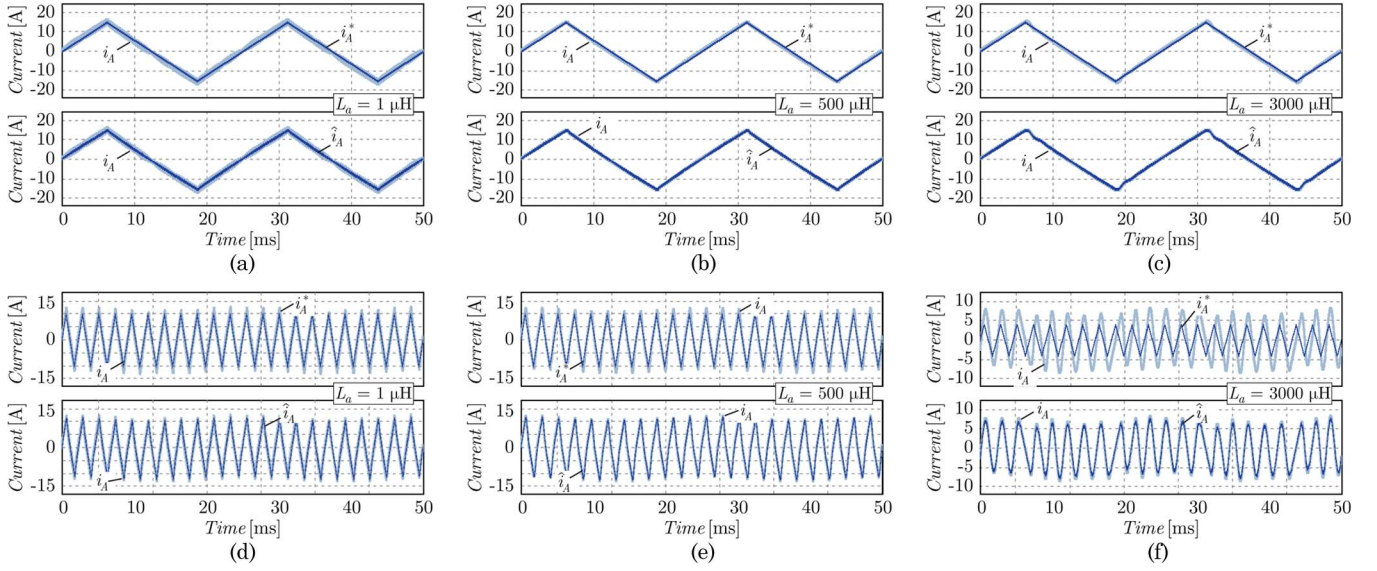


Fig. 11. Simulation results for triangular current references with 60 and 660 Hz, i.e., (a), (b), and (c) with $f_o = 60$ Hz and (d), (e), and (f) with $f_o = 660$ Hz for three different EUT inductances: (a) and (d) $L_a = 1 \mu\text{H}$, (b) and (e) $L_a = 500 \mu\text{H}$, and (c) and (f) $L_a = 3000 \mu\text{H}$. Simulations of the controlled system including the power circuit and the main digital control blocks, i.e., delays, quantization, sample and hold, PWM with double update mode, and the complete digital control blocks. Circuit parameters: $L_A = 420 \mu\text{H}$, $C_a = 1 \mu\text{F}$, $R_A = 33 \Omega$, $C_A = 1 \mu\text{F}$, and $E = 400$ V.

The frequency response regarding the tracking of the current reference is shown in Fig. 10 for three values of EUT inductance $L_a = 500 \mu\text{H} \pm 40\%$. The presented closed-loop Bode diagram considers computer simulations with the controlled system including the power circuit and the main digital control blocks, i.e., AD-conversion delays, quantization, sample and hold, PWM with double update mode, state feedback, observer, and current controller. The closed-loop system bandwidth measured at -3 dB approaches 11 kHz. However, it is important for the ac AEL that the phase delay is small for its harmonic reference following function. Thus, the practical frequency range is closer to 2 kHz, depending on the EUT inductance. Lower EUT inductances lead to a larger bandwidth.

The robustness and accuracy of the designed state observer is shown in Fig. 11. Six operation conditions are presented, namely, triangular current references with 60 and 660 Hz, i.e., $h = 1$ and $h = 11$ for three different EUT inductances $L_a = 1, 500, 3000 \mu\text{H}$. The triangular reference signal presents a rich harmonic spectrum and thus is used for this analysis. The peak current reference is varied accordingly for accounting for the saturation effects presented in Appendix B. The control performance is acceptable for the cases where $h = 1$ and also for $h = 11$ and $L_a = 1, 500 \mu\text{H}$. The control performance is poor with $L_a = 3000 \mu\text{H}$ and $h = 11$. However, the EUT current estimation is adequate even for this case.

The floating-point digital signal controller (DSC) TMS320F-28335 (150 MIPS) available from Texas Instruments is used to implement the control algorithm in the laboratory prototype.

V. EXPERIMENTAL RESULTS

The final specifications of the test setup are given in Table I.

A q-PLL-type phase-locked loop [44] was employed at the converter terminals to derive the synchronization signal to the voltage $v_{C,a}$. This can also be made at the supply terminals.

TABLE I
EXPERIMENTAL PARAMETERS

Parameter	Specification
v_a	Programmable power supply available from Supplier [43]
L_a (EUT)	20 A Si-steel wound inductor with $404 \mu\text{H}$
L_A	Ferrite inductor with $420 \mu\text{H}$
C_a, C_A	Film capacitors with $1 \mu\text{F}$
R_A	Wound resistor with 33Ω
E	Two series connected dc power supplies with $E \cong 400$ V
f_{sw} / f_s	66 kHz / 132 kHz

The PLL was designed with a 12-Hz bandwidth and 55° phase margin.

The dc-link terminals $p, n, 0$ were connected to two well-regulated dc sources. Furthermore, the dc-link capacitors were designed to provide voltage ripple lower than 4% under rated single-phase power, i.e., one-third of the rated three-phase power. This is to minimize the influence of EUT unbalances in the quality of the synthesized waveforms. Considering four-wire setups guarantees that the phases are decoupled. Thus, only single-phase results are presented in the following.

Current reference step experimental responses are seen in Fig. 12 for sinusoidal supply voltage and sinusoidal current reference in phase with the supply voltage. Fig. 12(a) shows a 4–8-A peak current step, while Fig. 12(b) shows the opposite step. Fast dynamics are observed, where overshoots are approximately 30%. These results were obtained with an EUT inductor of $404 \mu\text{H}$.

Fig. 13(a) shows the ac AEL operating as a power generator, i.e., inverter operation. Voltage v_a was deliberately programmed to supply approximately 5% fifth harmonic, leading to a voltage total harmonic distortion (THD) around 4.8% measured up to the 40th harmonic according to Fig. 13(b). The AEL current reference was a pure sinusoidal reference in phase with the mains fundamental voltage. The current THD was approximately 1.94%, while the maximum current harmonic (5th) was below 1% [cf. Fig. 13(c)]. A similar situation was

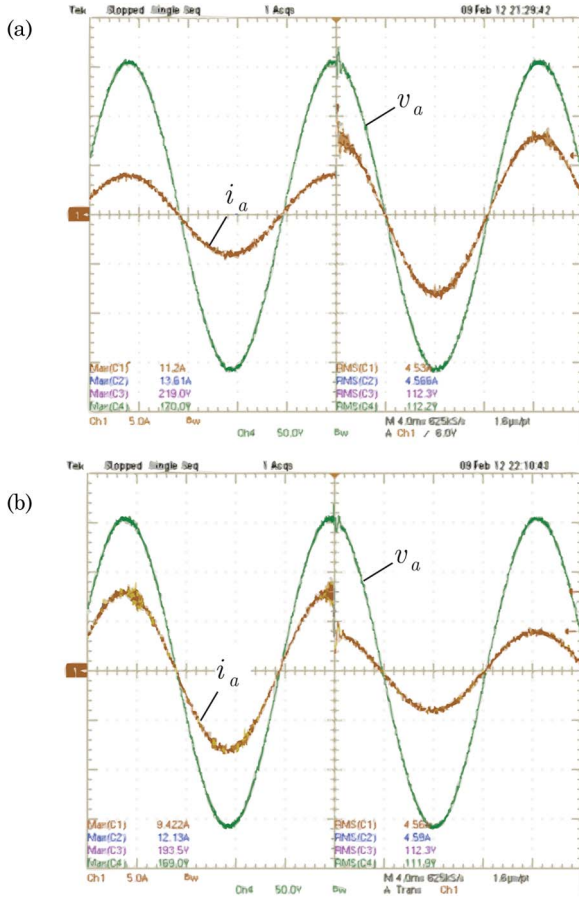


Fig. 12. Experimental waveforms showing the dynamic response of the AEL to peak current reference steps. The EUT current i_a is shown with the ac supply voltage v_a for reference currents steps from (a) 4 to 8 A and from (b) 8 to 4 A. Scales: Current i_a —5 A/div; voltage v_a —50 V/div.

tested with the AEL operating as a rectifier draining pure sinusoidal current from the EUT. The measured waveforms are presented in Fig. 14(a). The ac supply voltage v_a distortion emulates highly distorted mains that are typical on electrical installations with a large number of single-phase diode rectifiers. The supply voltage spectrum seen in Fig. 14(b) shows the 5% fifth harmonic, while the EUT current i_a shows all individual current harmonics below 1% and the current THD at approximately 1.57%. The AEL filter inductor current i_A and the filter capacitor voltage $v_{C,a}$ present HF ripple as expected. These results show that the proposed control scheme is able to reject disturbances from the grid side. UPS, rectifier, and general inverter testing applications can profit from this feature.

The current waveform generation capability of the proposed ac AEL is exemplified in the experimental results presented in Fig. 15. The synthesized current waveforms are drained from the programmable ac power supply feeding purely sinusoidal voltages (v_a) with an rms value of approximately 110 V.

Fig. 15(a) shows the ac AEL draining a triangular shaped current. The programmed current spectrum amplitudes are shown in Fig. 15(b) with the corresponding amplitudes of the harmonics of the actual current. The relation (gain) of the generated harmonics with the programmed ones is seen in Fig. 15(c). The 23th harmonic presents a +3-dB gain over its

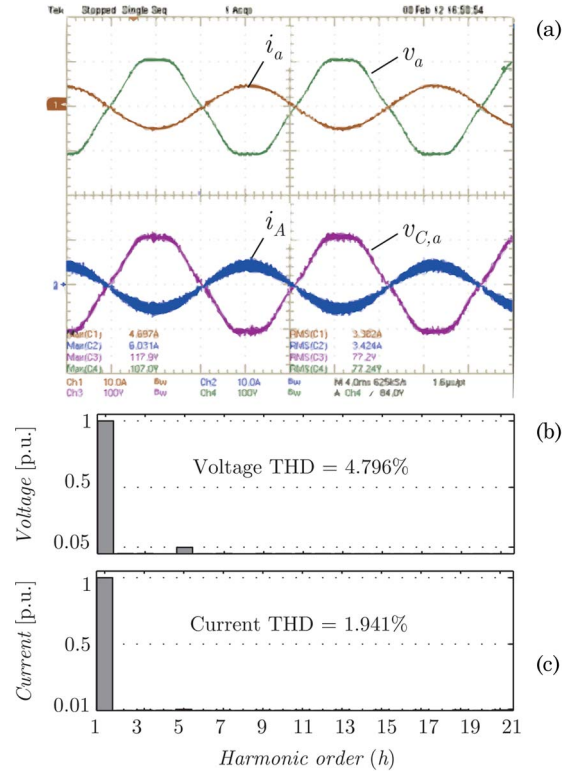


Fig. 13. Inverter operation. (a) Experimental waveforms: EUT current i_a , supply voltage v_a , converter current i_A , and filter capacitor voltage $v_{C,a}$. (b) AC supply voltage v_a spectrum and THD. (c) EUT current i_a spectrum and THD. Scales: Current i_a —5 A/div; voltage v_a —50 V/div.

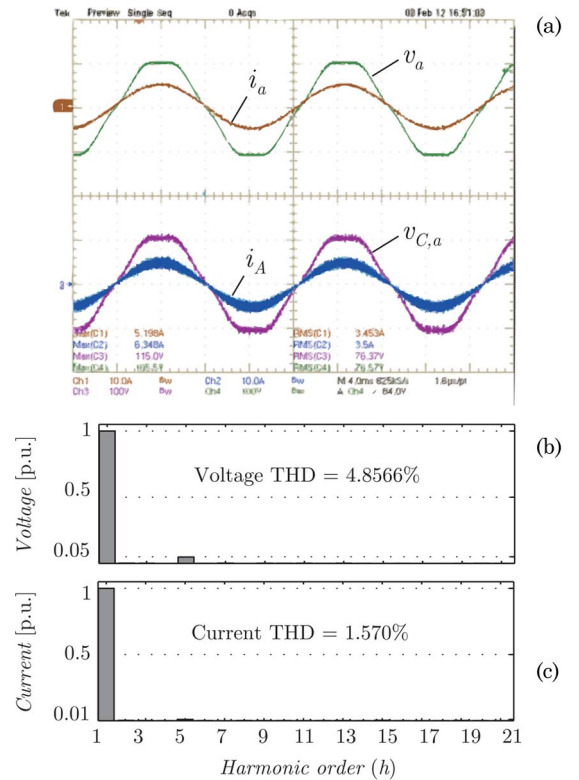


Fig. 14. Rectifier operation. (a) Experimental waveforms: EUT current i_a , supply voltage v_a , converter current i_A , and filter capacitor voltage $v_{C,a}$. (b) AC supply voltage v_a spectrum and THD. (c) EUT current i_a spectrum and THD. Scales: Current i_a —5 A/div; voltage v_a —50 V/div.

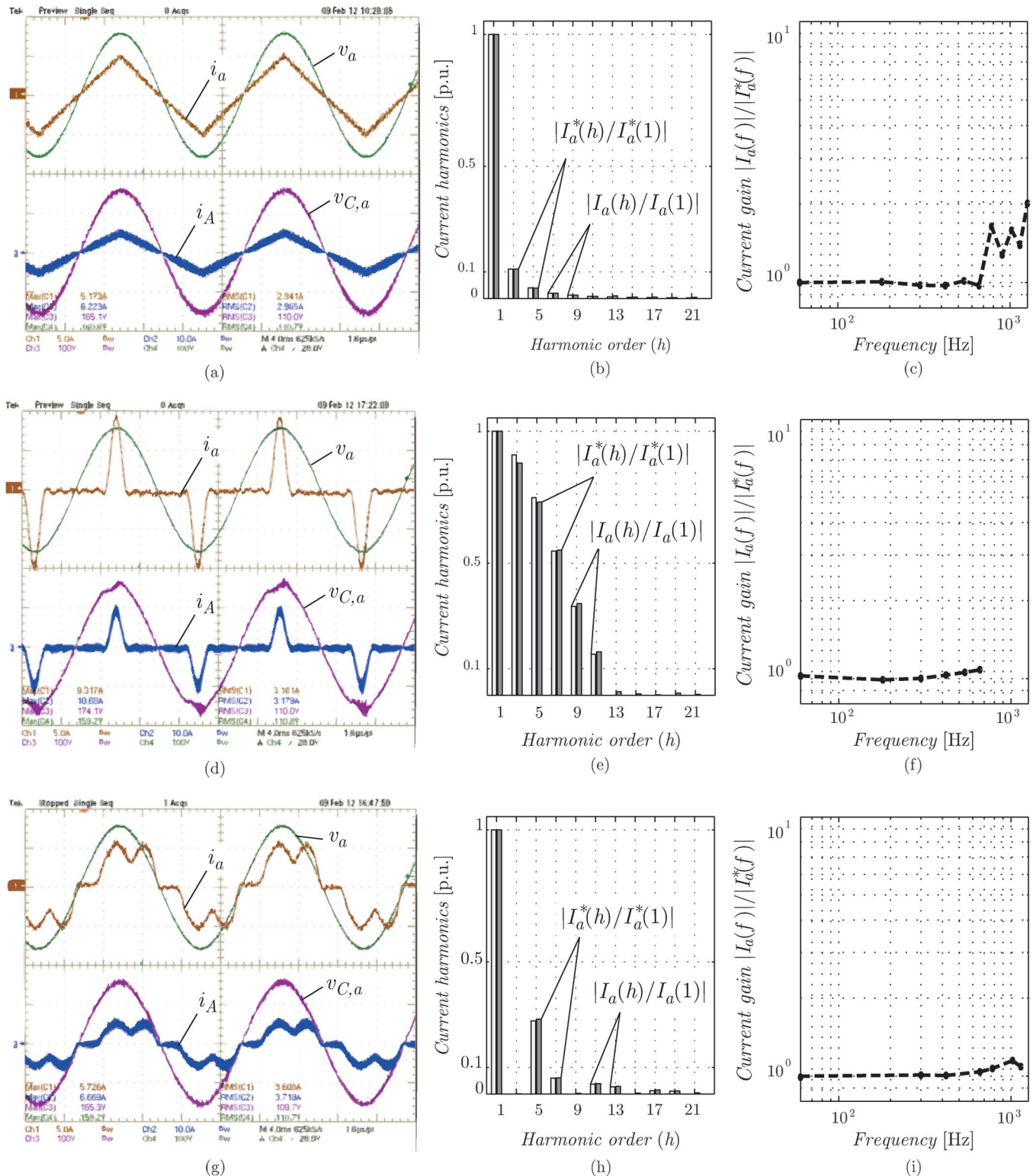


Fig. 15. Current spectrum programmed ac AEL operation. (a) Time waveforms for the EUT current i_a , ac supply voltage v_a , filter capacitor voltage $v_{C,a}$, and AEL inductor current i_A for a current reference comprising the harmonics of a triangular wave. (b) Programmed reference and measured current harmonic amplitudes for a current reference comprising the harmonics of a triangular wave. (c) Current spectrum gain for a current reference comprising the harmonics of a triangular wave. (d) Time waveforms for i_a , v_a , $v_{C,a}$, and i_A for a current reference emulating a typical single-phase rectifier. (e) Reference and measured current harmonic amplitudes for the emulation of a typical single-phase rectifier. (f) Current spectrum gain for the emulation of a typical single-phase rectifier. (g) Time waveforms for i_a , v_a , $v_{C,a}$, and i_A for a current reference emulating a typical three-phase rectifier. (h) Reference and measured current harmonic amplitudes for the emulation of a typical three-phase rectifier. (i) Current spectrum gain for the emulation of a typical three-phase rectifier. Scales: Current i_a —5 A/div; current i_A —5 A/div; voltage v_a —50 V/div; voltage $v_{C,a}$ —50 V/div.

reference. A very flat region is observed up to the 11th current harmonic.

Eleven harmonics were programmed to emulate a single-phase rectifier with a crest factor of $CF \cong 3$, as shown in Fig. 15(d) and (e). The computed gain of the harmonics is presented in Fig. 15(f).

Finally, the behavior of a typical three-phase diode bridge rectifier with smoothing inductors is emulated by the ac AEL. The achieved waveforms are seen in Fig. 15(g). The magnitude of the measured and programmed current harmonics is plotted in Fig. 15(h), and the gain curve points are in Fig. 15(i), where a flat region up to the 21th harmonic is observed.

The presented results show that the proposed AEL is able to perform the current harmonics control over a region that is of great interest for industrial equipment and thus enables high efficiency and flexible test systems. Based on the simulation and experimental results, a closed-loop response with a -3 -dB bandwidth of approximately 11 kHz is seen, which leads to a flat response up to approximately 1 kHz. This is contrasted against [17], which also uses a current controller based on a full-order system state feedback and presents a 2-kHz -3 -dB control bandwidth with 50-kHz switching frequency.

VI. CONCLUSION

This paper has discussed different aspects of the design of an ac active electronic with programmable current harmonics and dynamic transient capability. A novel control strategy and its design procedure were proposed for an ac AEL.

An appropriate power circuit for the application based on a three-level topology was used, which makes use of relatively high switching frequency and employs modern power semiconductor devices. Power circuit implementation issues were discussed, and a practical design guideline for the choice of the dc-link voltage of the AEL based on the harmonics to be generated is presented in Appendix B.

The EM compatibility filter is considered as it prevents HF emissions from the AEL to interfere with the EUT and the surrounding environment. However, such filter creates a resonance that poses a challenge for the current control of the AEL. The complete AEL circuit was modeled, and a control strategy that includes active damping through state feedback was proposed. The control system design considers a simplified model of the circuit and a state observer to estimate the EUT current. The challenges and limitations posed by the digital control implementation were discussed, and the importance of high switching frequency was highlighted.

Finally, simulation and experimental results from a laboratory prototype were presented. The experimental results include reference step tracking, mains voltage disturbance rejection, and current harmonics analysis that validate the proposed ac AEL control strategy. The results show that the tested system presents the capability to emulate different types of loads as required for the application at hand. The frequency response and the achieved frequency bandwidth are adequate to the testing of magnetic components. Other applications such as UPS circuits, inverters, generators, and hardware-in-the-loop applications, among others, can also profit from this type of technology.

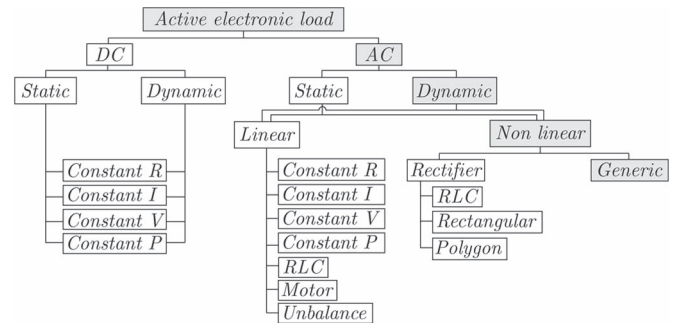


Fig. 16. Classification of AELs regarding load-type emulation.

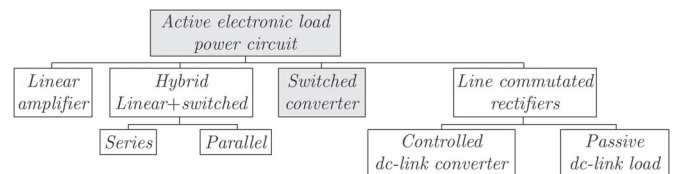


Fig. 17. Classification of AELs regarding AEL power circuit.

APPENDIX A AEL CLASSIFICATION

AELs are electronic power devices that emulate given characteristics of an electric power load within certain operational boundaries, i.e., the electrical and thermal limits defined in its specifications. Several expressions are used to name such devices, including AEL [45], [46], active power load, programmable load [47], load simulator [4], active load simulator [4], load emulator, energy recycler [10], [48], power recycler [49], power recycling unit, regenerative load [50], loss-free resistor [7], dynamic load, and DELS [17], among others.

AELs can be broadly divided into two major classes from the load-type perspective, namely, dc and ac. Further subdivisions are observed within these classes as illustrated in Fig. 16. It is observed that the first two main classifications depend on the dynamic characteristics that the AEL is able to emulate, i.e., if it can emulate the behavior of a load regarding its steady state (static AEL) [3] or both transient- and steady-state electrical responses (dynamic AEL) [16], [17], [50]. DC AELs emulate constant resistance, current, voltage, or power loads. The same types are observed within the linear load types that ac AEL emulates in addition to RLC circuits, electric motors, and unbalanced three-phase loads. However, the most difficult challenges for electronic load emulation are the ac nonlinear loads [50]. Nonlinear ac AELs are mainly divided into two subclasses, namely, rectifier-type loads and generic loads. Rectifier-type AELs can be further categorized depending on the shape of the ac currents as diode plus RLC loads and polygonal currents mainly with rectangular and trapezoidal shapes. Finally, the ones able to emulate programmable shapes for its ac currents are named generic ac AEL.

A second classification can be defined regarding the AEL power circuit as shown in Fig. 17. Four main types of AEL power circuits use linear amplifiers, switched converters, a hybrid of the two, or line-commutated rectifiers. Linear amplifiers [4] present as main advantages the high control bandwidth and the low level of EM emissions, but they have very low

conversion efficiency. These are widely used in dc AELs. Efficiency can be improved with the use of a hybrid series- or parallel-connected configuration [5] at the expense of higher EM emissions and lower control bandwidth. Most ac AELs employ switched converters due to their high conversion efficiency [4], [50]. Finally, line-commutated rectifiers [3] can be used to generate distorted currents from an ac supply equipment and, thus, model specific types of loads. Such rectifiers either use controlled converters in order to feed power back to the grid or passive circuits that consume energy as their dc-link load.

APPENDIX B

DC-LINK VOLTAGE LIMITATIONS TO THE GENERATION OF CURRENT HARMONICS

The generation of current harmonics is limited by the available voltage across the ac-side inductors. A case of this type of limitation is observed when the AEL is required to impose currents that do not present the first harmonic, i.e., a harmonic component at the mains fundamental frequency. Assume that the only filtering element between v_a and v_A is an ideal inductor with inductance L_{aA} , that $v_a = V_{pk} \sin(2\pi f_o t)$, and that a reference current is given by

$$i_a^* = I_{pk,(h)} \sin(2\pi f_o h t) \quad (34)$$

where f_o is the mains fundamental frequency and h is the reference current harmonic order. Thus, to impose the reference current, it follows that

$$v_A^* = \underbrace{V_{pk} \sin(2\pi f_o t)}_{V_{pk,a,reg}} - \underbrace{2\pi f_o h L_{aA} I_{pk,(h)} \sin(2\pi f_o h t)}_{V_{pk,A,harm}}. \quad (35)$$

The worst case for (35) is when the peak voltages $V_{pk,a,reg}$ and $V_{pk,A,harm}$ occur simultaneously. In this case, a minimum dc-link voltage E_{min} to impose i_a^* is given by the sum of the two voltage components. Thus

$$E_{min} = 2 \left(V_{pk} + 2\pi f_o h L_{aA} \hat{I}_{(h)} \right). \quad (36)$$

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Daniel Ferreira Coutinho (M'00–SM'12) received the B.S. degree in electrical engineering from the Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil, in 1989, and the M.S. and Ph.D. degrees in electrical engineering from the Universidade Federal de Santa Catarina (UFSC), Florianópolis, Brazil, in 1993 and 2003, respectively.

In 2001, he was a Visiting Scholar at the University of Newcastle Australia, Callaghan, Australia. From 1992 to 1997, he was a Lecturer with the Electronics Department, Federal Institute of Technology of Santa Catarina, Santa Catarina, Brazil. From 1998 to 2010, he was with the Faculty of Engineering, Pontifícia Universidade Católica do Rio Grande do Sul, Porto Alegre. In 2008, he spent a sabbatical year in the Service d'Automatique, University of Mons, Mons, Belgium. In 2010, he joined the Department of Automation and Systems, UFSC, where he is currently a Senior Lecturer. He is an Associate Editor of the *Institute of Mathematics and its Applications (IMA) Journal of Mathematical Control and Information*, and the *Journal of Control, Automation, and Electrical Systems* (formerly *Controle e Automação*, a scientific journal of the Brazilian Society for Automatic Control). His research interests include robust control and filtering, stability analysis and control of nonlinear systems, 2-D discrete-time systems, time-delay systems, singular systems, networked control systems, and switched systems, with applications in robotics, bioprocess control, and power electronics.



Samir Ahmad Mussa (M'06) was born in Jaguari-RS, Brazil, in 1964. He received the B.S. degree in electrical engineering from the Federal University of Santa Maria, Santa Maria, Brazil, in 1988 and also holds the second degree in mathematics/physics. The M.Eng. and Ph.D. degrees in electrical engineering were awarded by the Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 1994 and 2003, respectively.

He is currently an Adjunct Professor with the Power Electronics Institute (INEP), UFSC. His research interests include digital control applied to power electronics, power factor correction techniques, and DSP/field programmable gate array applications.

Dr. Mussa is currently a member of the Brazilian Power Electronics Society (SOBRAEP).



Joselito A. Heerdt (M'11) received the B.S. degree in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 1991 and the M.S. degree in electrical engineering from Santa Catarina State University (UDESC), Joinville, Brazil, in 2000.

From 1992 to 1998, he worked as an Electronic Engineer in the industry in Joinville, Brazil, and from 1998 to 2003, he worked as a Course Coordinator for the Industrial Automation course with Sociedade Educacional de Santa Catarina (SOCIESC). Since

2003, he has been a Professor with the Department of Electrical Engineering, UDESC, and in 2004, he founded the Supplier Indústria e Comércio de Eletroeletrônicos Ltda, an industrial power electronics supply company. His research interests include switching power converters, power quality, and renewable energy systems.

Mr. Heerdt is currently a member of the Brazilian Power Electronics Society (SOBRAEP).



Marcelo Lobo Heldwein (S'99–M'08–SM'13) received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 1997 and 1999, respectively, and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH Zurich), Zurich, Switzerland, in 2007.

From 1999 to 2003, he worked in the industry, including research at the Power Electronics Institute, Brazil, and Emerson Network Power, Brazil and Sweden. He was a Postdoctoral Fellow at the ETH Zurich and at the UFSC from 2007 to 2009. He is currently an Adjunct Professor with the Department of Electronics and Electrical Engineering, UFSC. His research interests include power electronics and electromagnetic compatibility.

Dr. Heldwein is a member of the Brazilian Power Electronic Society (SOBRAEP).