

Semiconductors Current Efforts and Losses Evaluation for Single-Phase Three-Level Regenerative PWM Rectifiers

Joselito A. Heerdt¹, Samir A. Mussa², and Marcelo L. Heldwein²,

¹Santa Catarina State University (UDESC)

Electrical Engineering Department — NPEE
Campus Universitário Prof. Avelino Marcante s/n
Joinville, BRAZIL, 89223-100
jaheerdt@joinville.udesc.br

²Federal University of Santa Catarina (UFSC)

Electrical Engineering Department — INEP
Campus Universitário Trindade, PO box 5119
Florianópolis, BRAZIL, 88040-970
samir; heldwein; @inep.ufsc.br

Abstract—Ac electronic loads are of interest in applications such as loss measurements in distribution transformers and small generators, UPS testing and other. In order to achieve high control bandwidth to inject current harmonics, it is important that EMC filters use small value passive components. Based on this requirement, three-level regenerative rectifiers are able to achieve better performance than two-level ones. Two candidate topologies for the implementation of a high performance 3.5 kW regenerative rectifier operating as ac electronic load are compared with respect to achievable efficiency numbers. Both topologies present the same external characteristics. The operation of the topologies is briefly reviewed in order to compute current efforts across the power devices. Based on which the losses for the converters are estimated along with their efficiency.

I. INTRODUCTION

As power quality and EMC standards become more stringent, several applications require three-phase bi-directional PWM rectifiers in order to effectively impose high quality currents at the ac-side. High power (kW) regenerative adjustable speed drives are one example. However, ac electronic loads are the subject of interest in this work. Conventional two-level boost topologies are typically employed in these applications. However, three-phase/-level boost-type PWM unidirectional rectifiers present performance advantages over two-level unidirectional rectifiers as shown in [1]–[10]. They excel where high quality input currents, high efficiency, volume and weight are required. Similarly, regenerative applications also profit from three-level topologies [11]. Three-level operation allows the voltage steps to be lower than those found in two-level topologies leading to reduced spectral contents. Smaller input filters are able to attenuate conducted emissions accordingly. The voltage across the semiconductors can be halved and semiconductors with lower voltage ratings are employed. Thus, overall losses can be reduced along with cooling systems and passive components. Nevertheless, some challenges, such as more complex modulation, control and voltage balancing schemes should be properly addressed.

The switching cells of traditional bi-directional three-level converters, such as the Neutral Point Clamped (NPC) [12], [13] and the Flying Capacitor (FC) [14] are typically employed

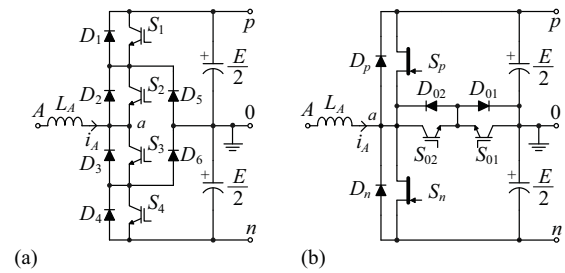


Fig. 1. Considered three-level regenerative rectifier topologies: (a) Neutral Point Clamped (NPC), and; (b) Modified Neutral Point Clamped (NPCm).

as three-level inverters. However, these topologies can be employed as rectifiers leading to the previously discussed advantages. These topologies are also commonly rated for very high power (hundreds of kW up to MW) and the use of such structures as bi-directional rectifiers in the lower kW range is not widespread. This work focuses on the computation of semiconductor current efforts and losses for two three-level regenerative rectifier topologies aiming at efficiency increase by the deployment of state-of-the-art power devices. The first topology is the conventional three-level NPC (cf. Fig. 1(a)). The second topology in this study is another type of three-level NPC where two switches are subject to the full dc-link voltage [14]–[16]. This topology is here named NPCm (cf. Fig. 1(b)).

The regenerative rectifier of interest is intended for 380 V/60 Hz input voltage aiming in a dc-link with a total voltage around 800 V. Furthermore, high switching frequency is required in order to reduce the volume and weight of passive components. Thus, the conventional NPC profits from the latest 600 V Si IGBT technology. However, the implementation of the NPCm requires two switches able to withstand the full dc voltage. In this regard there are no high performance and low switching losses IGBTs commercially available rated at 1200 V. On the other hand research efforts [17] aiming at high voltage turn-off devices based on SiC have already generated very fast semiconductors rated for 1200 V. Thus, the NPCm implemented in this work mixes 1200 V SiC

JFETs [18] and diodes with the same 600 V Si IGBT devices employed in the NPC. The objective of this work is, therefore, to compare the semiconductor current efforts and overall losses for both converter technologies while employing state-of-the-art semiconductors.

II. THREE-LEVEL REGENERATIVE RECTIFIER TOPOLOGIES

This section shows the operation principles of the considered multilevel PWM rectifier topologies. The considered topologies are shown in Fig. 1. It is seen that the circuit shown in Fig. 1(a) is a conventional Neutral Point Clamped converter (NPC) and the one depicted in Fig. 1(b) is a modified three-level converter structure, here named Modified Neutral Point Clamped Converter (NPCm). It is seen that both employ four turn-off devices, while the NPC (cf. Fig. 1(a)) requires six diodes, from which four are the anti-parallel IGBT diodes and two are the neutral point clamping diodes. The NPCm (cf. Fig. 1(b)) utilizes four diodes, from which two are anti-parallel IGBT diodes and two are implemented with discrete 1.2 kV rated SiC Schottky diodes. The main difference regarding semiconductor ratings is that semiconductors D_p , D_n , S_p and S_n are subject to the full dc-link voltage, while all other devices block half of it.

The employed power semiconductors are specified in Table I. "State-of-the-art" devices are chosen in order to compare both structures. The NPCm converter requires switches that block the full dc-link voltage connecting point a to, both, p and n terminals. Low switching losses conventional Si IGBTs and diodes are not commercially available at 1.2 kV ratings that are required for a 800 V dc-link. Thus, latest technology 1.2 kV normally-off SiC JFETs are considered for this structure. However, SiC devices still present higher costs than Si ones. Regarding 600 V-rated devices, latest generation Si IGBTs and Si Stealth diodes are able to achieve very low switching loss levels and are, therefore, employed where possible. For this reason 600 V Si IGBTs and Stealth diodes are employed in both converters at the component positions where the maximum theoretical requirement is limited to half of the dc-link voltage.

TABLE I
POWER SEMICONDUCTORS EMPLOYED IN THE CONSIDERED RECTIFIERS.

Component	NPC	NPCm	Features
IRF Si IGBT IRG4PC50W	S_1-S_4	S_{01}, S_{02}	$V_{CES} = 600$ V $V_{CE(on)} = 1.93$ V $I_C = 27$ A (@100°C)
SemiSouth SiC JFET Transistor SJEP120R063		S_n, S_p	$V_{DS} = 1200$ V $R_{DS(on)} = 63$ mΩ $I_D = 30$ A (@125°C) Normally-off
SemiSouth SiC Schottky SDP30S120		D_n, D_p	$V_{DC} = 1200$ V $V_F = 1.6$ V $I_D = 45.8$ A (@100°C)
Fairchild Si Stealth™ SDP30S120	$D_1 \dots D_6$	D_{01}, D_{02}	$V_{DS} = 600$ V $V_F = 2.1$ V $I_D = 30$ A (@25°C)

TABLE II
TURN-OFF SEMICONDUCTORS GATE SEQUENCE FOR POSITIVE MEAN
INPUT VOLTAGE VALUES.

Topology	Connected terminals			
	$a-p$	Delay	$n-a$	Delay
NPC	S_1, S_2	S_2	S_2, S_3	S_2
NPCm	S_p, S_{01}	S_{01}	S_{01}, S_{02}	S_{01}

Even though the requirements for the semiconductors and for the gate command signals are distinct in both converter structures, their external characteristics are similar. This means that the voltages and currents across all terminals (a , p , n and 0) are the same as long as both structures employ the same modulation strategy. Conventional Phase Opposition Disposition (POD) PWM modulation is employed in order to reduce input voltage (v_A) THD. The gate pulses sequence in order to generate similar positive mean voltage values is given in Table II for the two converters. The negative voltages are simply symmetrical to these. Delay interlock times are required for the proper operation of the circuits and are accordingly specified in Table II.

III. SEMICONDUCTOR CURRENT EFFORTS

Example waveforms are shown in Fig. 2(a) for the NPC and in Fig. 2(b) for the NPCm, both draining lagging input currents. The waveforms show the behavior of currents through the semiconductors with respect to arbitrary input phase voltage v_A and input current i_A . The operation of the rectifiers is defined in the following.

NPC: it is seen in Fig. 2(a) that the clamping diode D_6 switches during the complete positive half-cycle of the input current. The anti-parallel diodes of switches S_1 and S_2 conduct complementarily to D_6 while the input phase voltage is positive. After this instant, switches S_3 and S_4 start to operate and switch the current until the input current becomes negative.

NPCm: the current is switched between S_{02} and D_p while the input voltage and current are simultaneously positive. As the input voltage becomes negative the current is switched between S_{02} and S_n .

In order to achieve sinusoidal input currents, it is required that the rectifiers generate an according sinusoidal voltage based on the local average value of the switched voltage v_{A0} . Thus, the duty-cycle function $\delta_{S/D}$ for each switch is defined and the mean current value for a given device is

$$I_{S/D,avg} = \frac{1}{2\pi} \int_0^{2\pi} \delta_{S/D}(\omega t, M) \cdot i(\omega t, \phi) d\omega t \quad (1)$$

where, $i = \hat{I} \sin(\omega t + \phi)$, M is the modulation index and ϕ is the input current displacement angle. Respectively, the RMS current values are

$$I_{S/D,rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} \delta_{S/D}(\omega t, M) \cdot i(\omega t, \phi)^2 \cdot d\omega t}. \quad (2)$$

TABLE III
RMS AND AVERAGE CURRENT VALUES ACROSS EACH OF THE POWER SEMICONDUCTOR DEVICES.

	ϕ	NPC				NPCm			
		S_1, S_4	S_2, S_3	$D_1 \dots D_4$	D_5, D_6	S_p, S_n	S_{01}, S_{02}	D_p, D_n	D_{01}, D_{02}
Average current [A]	π	4.375	7.160	0.000	2.785	4.375	2.785	0.000	2.785
	$\pi/2$	1.393	5.767	1.393	4.375	1.393	4.375	1.393	4.375
	0	0.000	2.785	4.375	2.785	0.000	2.785	4.375	2.785
RMS current [A]	π	9.140	11.247	0.000	6.554	9.140	6.554	0.000	6.554
	$\pi/2$	4.570	10.277	4.570	9.205	4.570	9.205	4.570	9.205
	0	0.000	6.554	9.140	6.554	0.000	6.554	9.140	6.554

For the sake of brevity, only four duty-cycle functions are defined, two for the NPC rectifier,

$$\delta_{S_1}(\omega t, M) = \begin{cases} M \cdot \sin(\omega t) \rightarrow \forall(0 \leq \omega t < \pi) \\ 0 \rightarrow \forall(\pi \leq \omega t < 2\pi) \end{cases} \quad (3)$$

$$\delta_{S_3}(\omega t, M) = \begin{cases} 1 - \delta_{S_1}(\omega t, M) \rightarrow \forall(0 \leq \omega t < \pi) \\ 1 \rightarrow \forall(\pi \leq \omega t < 2\pi) \end{cases}, \quad (4)$$

and another two for the NPCm,

$$\delta_{S_p}(\omega t, M) = \begin{cases} M \cdot \sin(\omega t) \rightarrow \forall(0 \leq \omega t < \pi) \\ 0 \rightarrow \forall(\pi \leq \omega t < 2\pi) \end{cases} \quad (5)$$

$$\delta_{S_{02}}(\omega t, M) = \begin{cases} 1 - \delta_{S_p}(\omega t, M) \rightarrow \forall(0 \leq \omega t < \pi) \\ 1 \rightarrow \forall(\pi \leq \omega t < 2\pi) \end{cases}. \quad (6)$$

Fig. 3 shows the average and RMS current values for all switches in both circuit topologies with respect to the input current phase displacement angle. The current values are presented in per unit with a base current equal to the input current peak value. It is observed that the highest current values (RMS $\cong 1/2$ p.u. and AVG $\cong 0.32$ p.u.) occur in switches S_2 and S_3 in the NPC rectifier for current displacement angles higher than $2\pi/3$. All other power semiconductor devices present similar maximum current levels (RMS $\cong 0.4$ p.u. and AVG $\cong 0.2$ p.u.), although for different displacement angles. These angles are π rad for dc-link connected turn-off switches,

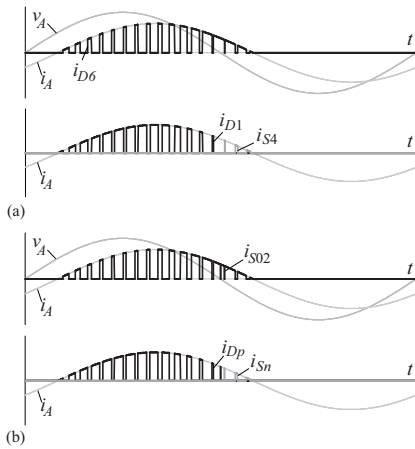


Fig. 2. Example theoretical waveforms considering i_A delayed from v_A for: (a) the NPC, and; (b) the NPCm.

$\pi/2$ rad for mid point connected ones and 0 rad for diodes connected in anti-parallel to the turn-off switches. The overall current distribution and, thus, conduction losses distribution is better in the NPCm converter.

The computed current efforts, according to Fig. 3, for all semiconductor devices are given in Table III for the case under analysis for three different input current displacement angles. Based on Table III, the computed current efforts allow that the NPCm converter can employ some of its devices with lower current ratings.

IV. SEMICONDUCTOR LOSSES

Linearized forward conducting voltage drop curves based on datasheet information for the considered semiconductors are depicted in Fig. 4 for different current levels. This figure shows that the 1.2 kV SiC JFETs present approximately twice the voltage drop of the 600 V Si IGBTs for higher current levels. However, the cost difference between the two components is high and there is a strong requirement to reduce the costs

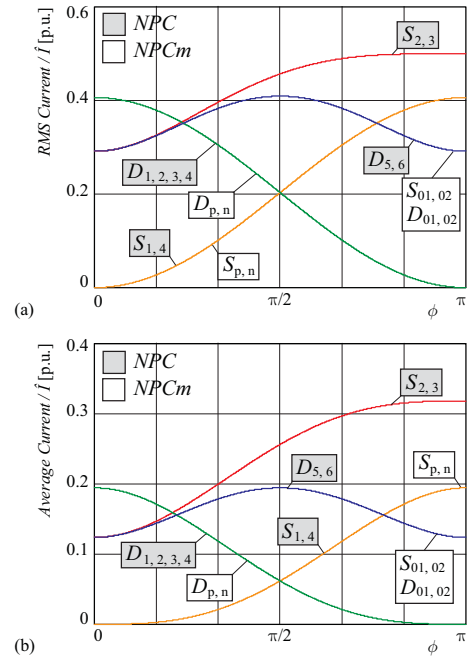


Fig. 3. Power semiconductor devices current (a) RMS, and; (b) average values for both topologies.

of SiC-based components. The 1.2 kV SiC Schottky diodes present the next higher voltage drop, followed by the IGBTs and the Stealth diodes, which are the slowest devices.

Switching energy curves are seen in Fig. 6. These curves show three portions of the switching energy per period, namely: switch turn-on e_{on} and turn-off e_{off} commutation processes as well as the energy associated to the reverse recovery e_{rr} (Stealth) or capacitive effects (SiC diodes) of the diode involved in the respective commutation. These measurements have been performed in an in-house made test fixture able to control temperature, voltage and current, while presenting

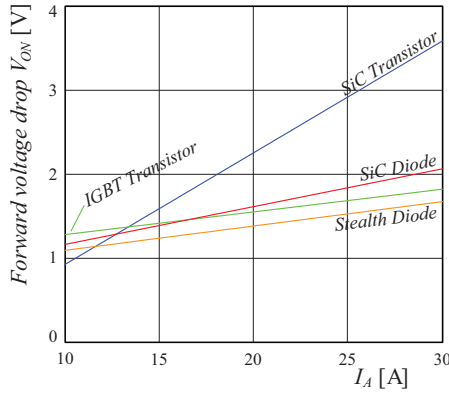


Fig. 4. Power semiconductor devices forward conducting voltage drop according to datasheet information. Test temperature: SiC—125°C; other—150°C.

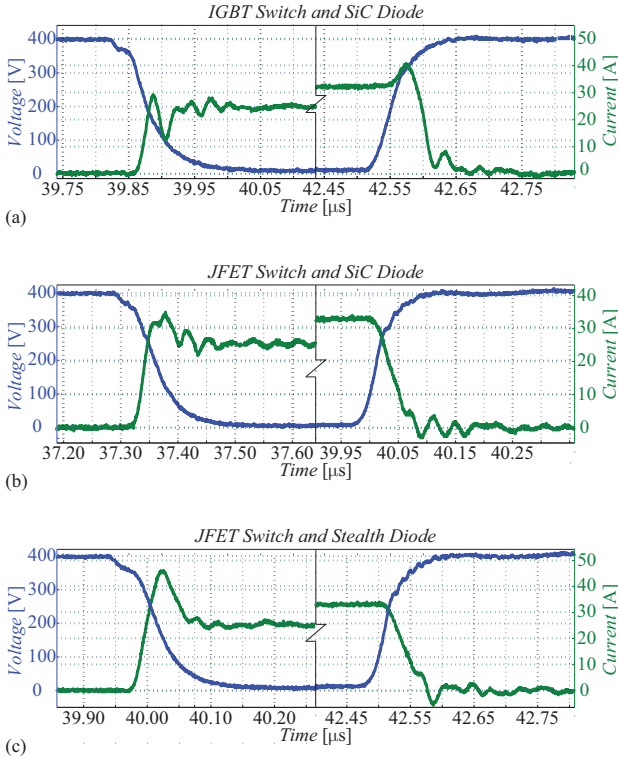


Fig. 5. Switching loss energy measurements for: (a) Si IGBT and SiC diode commutation; (b) SiC JFET and SiC diode commutation, and; (c) SiC JFET and Si Stealth diode commutation.

enough precision to characterize the switching voltages and currents. The switching loss measurements are required due to the difficulties in estimating stray inductances in the layout and, in special, due to the deployment of SiC JFET devices which are new devices and have not been completely modeled. Three example measurement results are shown in Fig. 5 for the three tested configurations regarding pairs of devices. The SiC JFET requires a custom gate driver circuit, which has been designed for low driver operation losses while preserving low switching on- and off-times.

Fig. 6(a) shows measurements and curve fittings for the switching energy losses regarding the commutations of an IGBT and a SiC diode. The curves for the commutations of a SiC JFET and a Stealth diode are given in Fig. 6(b), while Fig. 6(c) depicts the energy loss for the SiC JFET/SiC diode pair of semiconductors. The higher turn-off energy loss levels occur for the IGBT/SiC diode commutations. The highest turn-on losses occur for the SiC JFET/Stealth diode combination, while the highest e_{rr} is for the SiC JFET/SiC diode switchings.

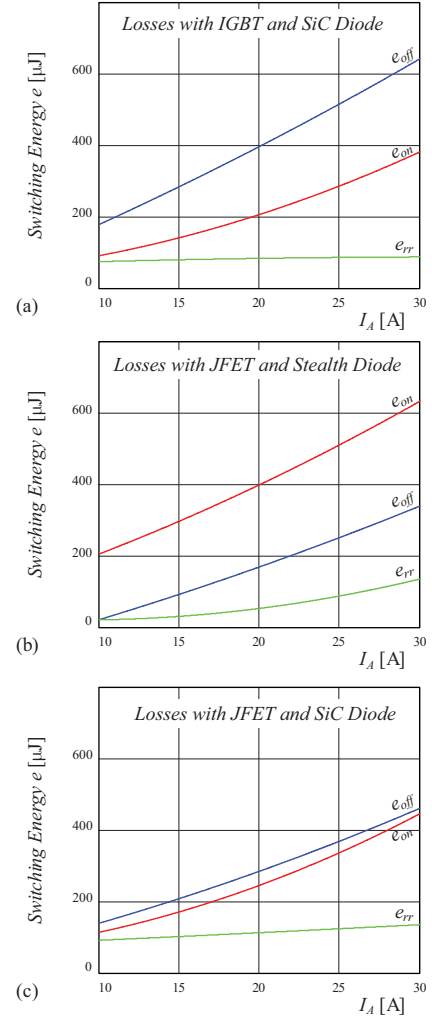


Fig. 6. Power semiconductor devices lost energy per switching cycle including turn-on, turn-off and reverse recovery processes. Test temperature: SiC—100°C; other—100°C.

TABLE IV
SEMICONDUCTOR RELATED LOSSES AND EFFICIENCY AT 3.5 kVA.

ϕ	Rectifier	P_{cond} [W]	P_{swit} [W]	P_{TOTAL} [W]	η [%]
0	NPC	38.74	21.30	60.05	98.313
	NPCm	28.74	20.29	49.03	98.619
$\pi/2$	NPC	40.23	31.11	71.33	98.003
	NPCm	34.57	18.75	53.33	98.499
π	NPC	41.72	40.91	82.62	97.694
	NPCm	36.64	17.21	53.85	98.485

Employing the characteristics given in Fig. 4, the conduction losses for each device is computed with

$$P_{S/D,con} = \frac{1}{2\pi} \int_0^{2\pi} ([i_{S/D}(\omega t, \phi) \cdot v_{S/D,on}(\omega t)] d\omega t, \quad (7)$$

where $v_{S/D,on}(\omega t) = k_{S/D,1} \cdot i_{S/D}(\omega t, \phi) + k_{S/D,0}$ is the forward voltage drop curve fitted polynomials based on datasheet information for different current values.

The switching energies given in Fig. 6 are obtained from switching loss measurements and are mathematically expressed as second order polynomials for the turn-on e_{on} , turn-off e_{off} and reverse recovery e_{rr}

$$e_{on}(\omega t, \phi) = k_{on,2}|i(\omega t, \phi)|^2 + k_{on,1}|i(\omega t, \phi)| + k_{on,0} \quad (8)$$

$$e_{off}(\omega t, \phi) = k_{off,2}|i(\omega t, \phi)|^2 + k_{off,1}|i(\omega t, \phi)| + k_{off,0} \quad (9)$$

$$e_{rr}(\omega t, \phi) = k_{rr,2}|i(\omega t, \phi)|^2 + k_{rr,1}|i(\omega t, \phi)| + k_{rr,0}. \quad (10)$$

The switching losses for a complete period are approximated with

$$P_{sw} = \frac{f_s}{2\pi} \int_0^{2\pi} [e_{on}(\omega t, \phi) + e_{off}(\omega t, \phi) + e_{rr}(\omega t, \phi)] d\omega t \quad (11)$$

Employing this methodology to the case under analysis leads to the losses values presented in Table IV, where the efficiency for different input current displacement angles is computed based only on the power semiconductor devices, i.e. all passive component losses are neglected. Efficiencies ranging from 98.485% for the NPCm, working as unity power factor regenerative operation (inverter), up to 98.619% also for the NPCm, though operating as unit power factor rectifier, are achievable. For all computed operating conditions the semiconductor losses are lower for the NPCm converter when compared to the NPC.

Fig. 7 shows the behavior of the total conduction losses for both converters as a function of the input current peak value and displacement angle. It is seen that the NPC presents increasing losses with increasing current and increasing displacement, where the higher losses occur for unity power factor regenerative operation. The conduction losses for the NPCm present higher variation regarding the input current angle, where the worst case is observed at π rad. As a general conclusion, the NPCm presents lower conduction losses throughout the entire operation range.

Total switching losses are depicted in Fig. 8 and show different tendencies when compared to the conduction losses. The NPC rectifier presents increasing switching losses with increasing input current displacement angle, whereas the opposite behavior is presented by the NPCm converter. Nevertheless, both converters present higher switching losses around 60 W at the extremes (0 rad / π rad) of the operation range.

Based on the aforementioned losses, the efficiency of the converters is calculated as given in Fig. 9. Once again, the converters behave differently. The NPC efficiency strongly drops when the converter operates at higher current levels and

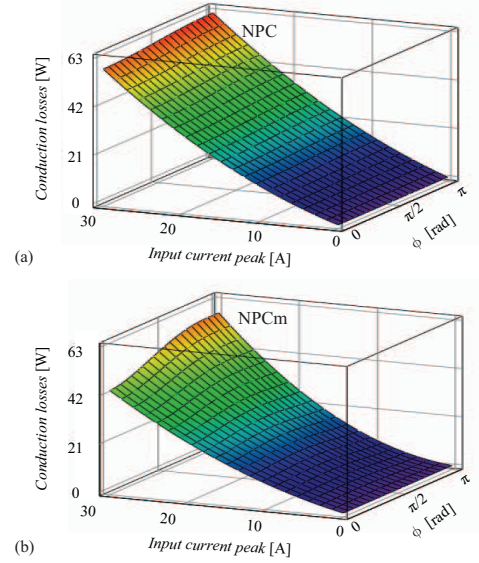


Fig. 7. Total conduction losses regarding power semiconductors: (a) NPC, and; (b) NPCm.

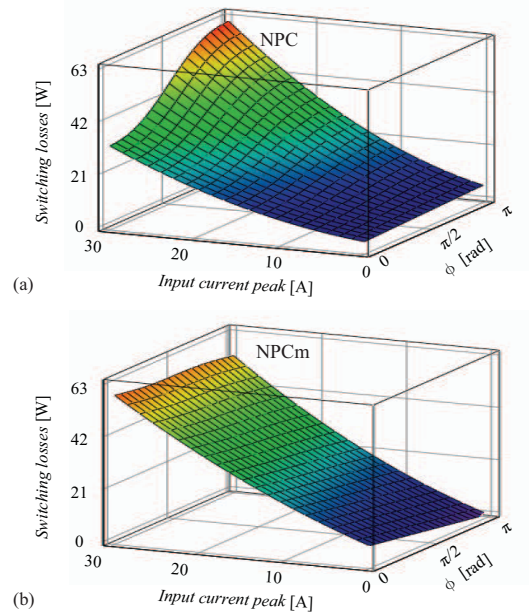


Fig. 8. Total switching losses regarding power semiconductors: (a) NPC, and; (b) NPCm.

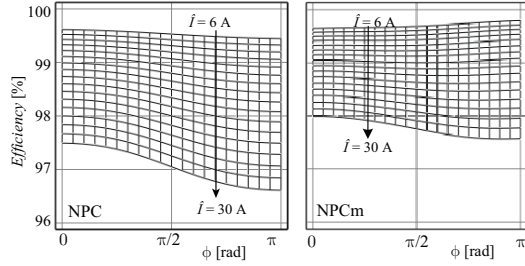


Fig. 9. Computed efficiency values regarding power semiconductors: (a) NPC, and; (b) NPCm.

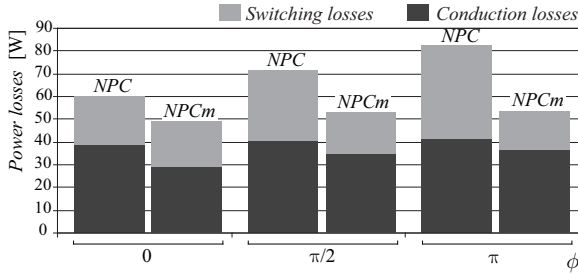


Fig. 10. Power semiconductor losses split into switching and conduction portions for, both, the NPC and the NPCm converters for three different current displacement angles. Operating conditions: $P_o = 3.5$ kVA; $\hat{I} = 22.5$ A; $M = 0.778$; $f_s = 40$ kHz.

achieves its maximum for unit power factor rectifier operation. The efficiency curves for the NPCm rectifier (cf. Fig. 9(b)) show that the higher efficiency points regarding input current angle depend on the involved current levels. For high currents, the efficiency is higher for unity power factor rectifier mode.

Fig. 10 shows the computed losses for three different input current displacement angles and rated output power. NPC losses are evenly distributed into switching and conduction losses. The switching losses are lower than the conduction losses in the NPCm converter, suggesting that the switching frequency could be increased in order to achieve the same efficiency levels as for the NPC converter. Conduction losses are lower for the NPCm converter and this fact is typically observed as long as semiconductors with balanced forward voltage drops are employed in both topologies.

V. CONCLUSIONS

Two candidate topologies for the implementation of a high performance 3.5 kW regenerative rectifier operating as ac electronic load have been compared with respect to achievable efficiency numbers. Both topologies present the same external characteristics, i.e., the same input and output current and voltage waveforms as long as equivalent modulation patterns are employed. Circuit operation has been reviewed and the current efforts (average and RMS values) across the power semiconductors has been presented for POD-PWM modulation. Different "state-of-the-art" power semiconductors have been chosen for the converters based on their specific needs. These semiconductors have been compared regarding current and voltage efforts as well as conduction and switching losses

behavior, which have been experimentally measured. Based on these, the losses for both converters have been computed and their efficiency presented for the complete operation range. Regarding semiconductor related losses, the chosen semiconductors allow for high efficiency levels at the specified switching frequency. As a main result, the NPCm topology employing the chosen semiconductors presents lower overall losses for the studied converter operation range. Conduction losses are lower for NPCm rectifier throughout the complete operating range.

REFERENCES

- [1] J. W. Kolar and H. Ertl, "Status of the techniques of three-phase rectifier systems with low effects on the mains," in *IEEE International Telecommunications Energy Conference*, 1999, p. 16 pp.
- [2] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality ac-dc converters," *IEEE Transactions on Industrial Electronics*, vol. 51, no. 3, pp. 641–660, 2004, 0278-0046.
- [3] G. Gong, M. L. Heldwein, U. Drofenik, J. Minibock, K. Mino, and J. W. Kolar, "Comparative evaluation of three-phase high-power-factor ac-dc converter concepts for application in future more electric aircraft," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 727–737, 2005, 0278-0046.
- [4] T. Nussbaumer and J. W. Kolar, "Comparison of 3-phase wide output voltage range pwm rectifiers," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 3422–3425, 2007.
- [5] Y. Zhao, Y. Li, and T. A. Lipo, "Force commutated three level boost type rectifier," in *IEEE Industry Applications Society Annual Meeting*, 1993, pp. 771–777 vol.2.
- [6] K. Oguchi and I. Maki, "A multilevel-voltage source rectifier with a three-phase diode bridge circuit as a main power circuit," *IEEE Transactions on Industry Applications*, vol. 30, no. 2, pp. 413–422, 1994, 0093-9994.
- [7] J. C. Salmon, "3-phase pwm boost rectifier circuit topologies using 2-level and 3-level asymmetrical half-bridges," in *Applied Power Electronics Conference and Exposition*, 1995, pp. 842–848 vol.2.
- [8] J. W. Kolar and F. C. Zach, "A novel three-phase utility interface minimizing line current harmonics of high-power telecommunications rectifier modules," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 4, pp. 456–467, 1997, 0278-0046.
- [9] B. R. Lin and T. C. Wei, "Unidirectional three-phase rectifier with high power factor," *IEE Proceedings - Electric Power Applications*, vol. 151, no. 2, pp. 215–222, 2004, 1350-2352.
- [10] B. R. Lin and T. Y. Yang, "Three-phase high power factor ac/dc converter," *IEE Proceedings - Electric Power Applications*, vol. 152, no. 3, pp. 485–493, 2005, 1350-2352.
- [11] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," *IEEE Transactions on Industry Applications*, vol. 41, no. 3, pp. 855–865, 2005, 0093-9994.
- [12] R. H. Baker, "Bridge converter circuit," Patent U.S. 4,270,163, 1981.
- [13] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped pwm inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, 1981, 0093-9994.
- [14] T. A. Meynard, H. Foch, F. Forest, C. Turpin, F. Richardeau, L. Delmas, G. Gateau, and E. Lefeuvre, "Multicell converters: derived topologies," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 978–987, 2002, 0278-0046.
- [15] P. M. Bhagwat and V. R. Stefanovic, "Generalized structure of a multilevel pwm inverter," *IEEE Transactions on Industry Applications*, vol. IA-19, no. 6, pp. 1057–1069, 1983, 0093-9994.
- [16] A. I. Alolah, L. N. Hulley, and W. Shepherd, "A three-phase neutral point clamped inverter for motor control," *IEEE Transactions on Power Electronics*, vol. 3, no. 4, pp. 399–405, 1988, 0885-8993.
- [17] S. Round, M. Heldwein, J. Kolar, I. Hofsjager, and P. Friedrichs, "A sic jfet driver for a 5 kw, 150 khz three-phase pwm converter," in *Industry Applications Conference*, vol. 1, 2005, pp. 410–416 Vol. 1.
- [18] SemiSouth, "Normally-off trench silicon carbide power jfet," 2009, available at <http://www.semisouth.com/>.