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A New Three-Level Quadratic (T-LQ) DC-DC Converter Suitable for Fuel Cell Applications

Yales Rômulo De Novaes*	Non-member
Ivo Barbi**	Non-member
Alfred Rufer*	Non-member

This paper presents a new non-insulated three-level DC-DC boost converter with quadratic static gain. The quadratic feature is interesting for applications where a wide voltage range is necessary. The voltage across the switches is smaller than the output voltage. Since it is a current-source converter, its application in fuel cell energy conversion systems seems interesting, but other applications where the involved voltages are higher is very possible. Theoretical analysis for CCM of operation and experimental results are presented. A comparison between the two cascaded boost converter, the single switch quadratic boost converter and the proposed converter is made regarding commutated power. By experimental results is shown that the efficiency of the proposed converter is higher than two cascaded boost converters, even with less installed semiconductor power.

Keywords: multilevel converter, quadratic converter, boost, fuel cells, renewable energy, transformerless, large voltage ratio, wide voltage range

1. Introduction

Fuel cell's steady-state and dynamic electrical characteristics are very peculiar when compared with other kind of power sources. When designing converters for fuel cells, it is necessary to consider the fuel cell innate characteristics instead of considering it only as an ideal DC voltage source. Also, the complete system must be taken into account when choosing static converters for fuel cell applications.

One of the fuel cells connatural characteristic is that it delivers energy at low voltages ($\approx 1.17\text{ V @ }80^\circ\text{C}$), depending on the application they are usually stacked to reach useful voltages. Nowadays, in applications where the power is situated between 1 kW and 10 kW the range of the fuel cell output voltage is between 24 V and 60 V. These values are low when compared with the necessary voltage at inverter's input, when this type of energy conversion is needed. This fact results in the necessity of another conversion stage between the fuel cell and the inverter, usually a step-up DC-DC converter. As a consequence the voltage gain of the DC-DC stage must be high enough to accommodate this difference. Then, cascaded converters or transformer isolation can be necessary, just to adapt the voltage difference.

Another important issue that must be taken into account when processing energy from fuel cells is its voltage

regulation. The converter that is directly connected to this kind of power source suffers from the highest voltage at no load and from the highest current at the maximum load but with lower voltage. This results in the overdimensioning of the converter. Likewise, if the converter connected to the fuel cell terminals is an isolated one, the design of the transformer will be affected and its VA ratings will be higher than the processed active power. Besides that, because the voltage is low the input current can be very high, even for low power (1 kW to 10 kW), making difficult to reach high efficiency in the first conversion stage.

On the other hand, the necessity of low power auxiliary power supplies well suited for high DC voltages ($> 800\text{ V}$) is clear in the implementation of high power converter for motor drives, power factor correction and multilevel converters among other applications. The possibility of connection of this ancillary power supplies directly at the high voltage DC links of the power converters makes easier the implementation. To contribute in the solution of this problem, Refs. (1) (2) proposed three-level forward and flyback topologies, in which the switches' voltages are equal to the input voltage divided by two. By using a similar technique to conceive the topologies, Ref. (3) proposed a family of three-level non-insulated basic converters.

Motivated by these facts and the mentioned contributions, this paper proposes three new step-up topologies, which are named Three-Level Quadratic (T-LQ) non-insulated DC-DC boost converters, being characterized by providing the variation of the output voltage with a quadratic gain. This means that comparing the classic boost converter with the proposed ones, the gain of the new converters can be the double. Another characteristic of the proposed converters is that the voltage across each active switch is lower than the output voltage. This occurs because this voltage is shared among the active

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* Laboratoire d'Electronique Industrielle (LEI) Ecole Polytechnique Fédérale de Lausanne (EPFL)

CH-1015, Lausanne, Switzerland, yales@ieee.org

** Power Electronics Institute (INEP), Federal University of Santa Catarina (UFSC)

P.O. Box 5119, 88040-970, Florianópolis, SC, Brazil

switches, as shall be shown later in the text. Defining the installed semiconductor power as being the sum of all switches commutated power, which utilizes the unit Volt-Ampere or in its short form VA, all topologies presented in this paper can be compared. Because semiconductor cost is usually related to its commutation capabilities, the utilized VA-ratings give an image of the converters cost. The installed semiconductor power can be related to the converter's power to give an idea of switches utilization. One of the new topologies which has the lowest VA-ratings is considered by the author as being suited for applications where low input voltage and high voltage ratio are required, like in fuel cell systems. Besides those characteristics, the presented topology is a current-sourced one, what enables the reduction of the input ripple current to very low values. This fact brings another advantage for application in fuel cell systems, where large ripple current may bring additional problems⁽⁴⁾⁽⁵⁾ or, at least, increase the electrode losses or material usage due to the high RMS current values⁽⁶⁾.

Inside this paper, a comparison regarding installed semiconductor power is made between the proposed topology, two cascaded boost converters and a single switch quadratic boost converter. The procedure to generate the new topology is shown. The static gain, topological states and main waveforms, are described theoretically for Continuous Conduction Mode (CCM) of operation of the lowest component count topology. To validate the theoretical analysis, prototypes of the new converter and the two boost cascaded converter were implemented considering the specifications of a fuel cell system. The efficiencies of both converters were compared and the experimental results are presented.

2. Application Overview and Candidate Topologies

The proposed converter topology was generated in the context of the application presented by Ref. (7), with the goal of improving the long-term UPS based on fuel cells. For the reader comfort, the UPS system is re-presented by Fig. 1, in which the DC-DC converter stage can be identified (multiple DC-DC converters).

A good topology to be adopted in the DC-DC conversion stage of this application could be the conventional boost converter. However, for high static gains, the converter losses becomes important, reducing its efficiency, even so if the ideal static gain can reach high values. This technological limitation can be seen by considering the component losses in the boost converter static gain equations. This is demonstrated from Eq. (1) to Eq. (7), where the last one is depicted in Fig. 2. This graphic shows the maximum gain as a function of parameterized resistances of a boost converter. Bigger the parameterized resistance, lower is the maximum gain. In those equations, variable R_L represents the AC resistance of the boost converter inductance, while variable R_S represents the active switch resistance, which clearly exist in case of MOSFET semiconductors. Variables q and p represent the same components but parameterized as a function of the effective load resistance R_o . Diode losses and output capacitor losses are not computed since this is just an example to show how the static gain is not infinite and is limited by losses.

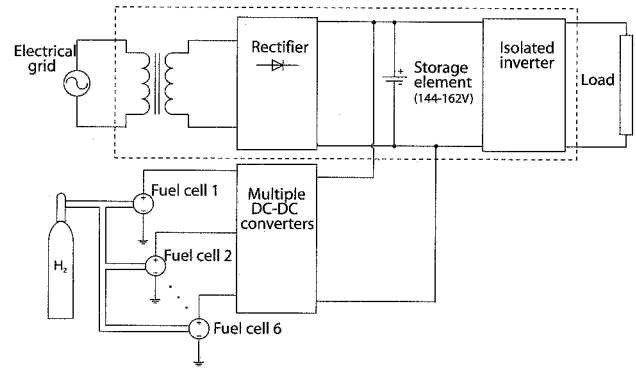


Fig. 1. Long-term uninterruptible power supply architecture

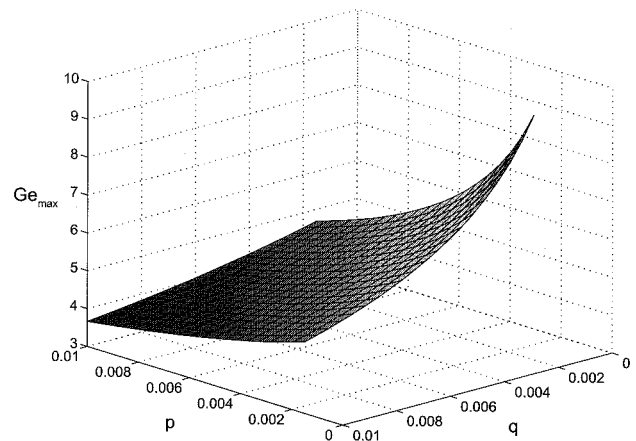


Fig. 2. Maximum boost converter static gain when considering component losses

$$Ge_{ideal}(D) = \frac{V_o}{V_i} = \frac{1}{1-D} \quad (1)$$

$$Ge = \frac{1}{1-D} \cdot \frac{1}{\left(\frac{R_L+R_S}{R_o}\right) \cdot \left(\frac{1}{1-D}\right)^2 - \frac{R_S}{R_o} \cdot \frac{1}{1-D} + 1} \quad (2)$$

$$q = \frac{R_L}{R_o} \quad (3)$$

$$p = \frac{R_S}{R_o} \quad (4)$$

$$Ge(D, p, q) = \frac{1}{1-D + p \cdot \left(\frac{D}{1-D}\right) + q \cdot \left(\frac{1}{1-D}\right)} \quad (5)$$

$$D_{Ge_{max}} = 1 - \sqrt{q+p} \quad (6)$$

$$Ge_{max} = \frac{\sqrt{q+p}}{2(p+q) - p\sqrt{q+p}} \quad (7)$$

Other solutions to accommodate this voltage difference could be the use of quadratic, cascaded or insulated converters. Since this application did not require insulation, a non-insulated topology can be adopted.

An architecture where two boost converters are cascaded is shown by Fig. 3(a). This solution fulfills the mentioned requirements. Another topology, with one less switch but with one more diode, Fig. 3(b) presents a single switch quadratic boost converter⁽⁸⁾⁽⁹⁾.

But which one of those solutions based on the boost converters has the lowest VA-ratings?

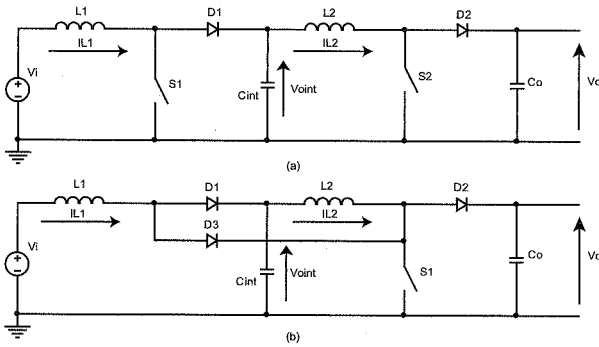


Fig. 3. (a) Two cascaded boost converters; (b) single switch quadratic boost converter

2.1 Commutated Power Analysis When comparing both solutions in terms of installed (commutated) semiconductor power, it is possible to conclude that the total commutated power in the single switch converter is higher than in the two cascaded converters. Since the cost of a semiconductor is also related to its capacity to commute a certain voltage and current, the total commutated power of a converter gives an image of the cost of this converter. In doing so, this figure of merit can be used for topologies comparison.

Defining the commutated power⁽¹⁰⁾ as presented by Eq. (8), it is possible to determine the total commutated power by using Eq. (9), where I_i and V_i are semiconductor's current and voltages. For the active switches, MOSFETs in this project, it is considered that the commutated power is the maximum voltage across the switch $V_{S_{irms}}$ times the RMS current $I_{S_{irms}}$, as shown by Eq. (10). While in case of diodes, it is considered that the commutated power is average current $I_{D_{iavg}}$ times maximum voltage $V_{D_{imax}}$, as presented by Eq. (11).

$$Sc_i = I_i \cdot V_i \quad (8)$$

$$Sc_{tot} = \sum_{i=1}^k V_i \cdot I_i \quad (9)$$

$$Sc_{S_i} = I_{S_{irms}} \cdot V_{S_{imax}} \quad (10)$$

$$Sc_{D_i} = I_{D_{iavg}} \cdot V_{D_{imax}} \quad (11)$$

Neglecting the inductor ripple current, since it should be low in fuel cell applications, it is possible to determine the semiconductors commutated power as presented from Eq. (12) to Eq. (16). Neglecting the efficiency, the total commutated power for the two cascaded converters (Fig. 3(a)) is presented by Eq. (17), parameterized as a function of the output power P_o . This parameterized commutated power represent exactly how many times the installed semiconductor VA-ratings (VA) is bigger then the rated power (W) of the converter.

$$\overline{Sc_{S_1}}(D) = \frac{Sc_{S_1}}{P_o} = \frac{\sqrt{D}}{(1-D) \cdot \eta_{tot}} \quad (12)$$

$$\eta_{tot} = \eta_1 \cdot \eta_2 \quad (13)$$

$$\overline{Sc_{S_2}}(D) = \frac{Sc_{S_2}}{P_o} = \frac{\sqrt{D}}{(1-D) \cdot \eta_2} \quad (14)$$

$$\overline{Sc_{D_1}}(D) = \frac{1}{\eta_2} \quad (15)$$

$$\overline{Sc_{D_2}}(D) = 1 \quad (16)$$

$$\overline{Sc_{tot}}(D) = \frac{2\sqrt{D}}{1-D} + 2 \quad (17)$$

Where D is the switch duty cycle and $\eta_{1,2,tot}$ are the efficiencies of the stage 1, 2 and total. The commutated power is described by Sc for the switches S_1 and S_2 and for diodes D_1 and D_2 . The total commutated power is identified by the subscript *tot* which is the sum of all semiconductor commutated powers. Over lined symbol means that the variable is parameterized as a function of P_o .

Following the same methodology for the single switch quadratic boost converter (Fig. 3(b)), the switch's commutated power and additional diode's commutated power are presented by Eq. (20) and Eq. (21), respectively. The total commutated power, neglecting the converter's efficiency, is presented by Eq. (22).

$$I_{S_{irms}} = (I_{L_{1avg}} + I_{L_{2avg}}) \cdot \sqrt{D} \quad (18)$$

$$V_{S_{imax}} = V_o \quad (19)$$

$$\overline{Sc_{S_1}}(D) = \frac{Sc_{S_1}}{P_o} = \frac{\sqrt{D}}{(1-D)^2} \left(\frac{\eta_2 + \eta_{tot}(1-D)}{\eta_{tot} \cdot \eta_2} \right) \quad (20)$$

$$\overline{Sc_{D_3}}(D) = \frac{D^2}{(1-D)^2 \cdot \eta_{tot}} \quad (21)$$

$$\overline{Sc_{btot}}(D) = 2 + \frac{D^2 + \sqrt{D}(2-D)}{(1-D)^2} \quad (22)$$

In Eq. (18), $I_{L_{1avg}}$ and $I_{L_{2avg}}$ are the inductors average currents. The power commutated by diode D_3 is described by Sc_{D_3} . The total commutated power for the topology presented in Fig. 3(b) is determined by $\overline{Sc_{btot}}$.

Considering that the duty cycle has the same value for all active switches, Eq. (17) and Eq. (22) can be rewritten as a function of the static gain, as presented by Eq. (25) and Eq. (26), respectively. These equations were obtained by substituting Eq. (24) into Eq. (17) and Eq. (22).

Just for comparison, the equations for the single stage converter (basic boost converter) are obtained from Eq. (12), Eq. (15) and Eq. (28), and the result is presented by Eq. (27) and Eq. (29).

$$Ge = \frac{1}{(1-D)^2} \quad (23)$$

$$D = 1 - \frac{1}{\sqrt{Ge}} \quad (24)$$

$$\overline{Sc_{tot}}(Ge) = 2\sqrt{Ge} - \sqrt{Ge} + 2 \quad (25)$$

$$\overline{Sc_{btot}}(Ge) = 2 + (1 - \sqrt{Ge})^2 + \sqrt{Ge(\sqrt{Ge} + Ge - 1)} - 1 \quad (26)$$

$$\overline{Sc_{tot}}(Ge) = \frac{\sqrt{D}}{(1-D)} + 1 \quad (27)$$

$$Ge = \frac{1}{1-D} \quad (28)$$

$$\overline{Sc_{tot}}(Ge) = 1 + \sqrt{Ge^2 - Ge} \quad (29)$$

In order to better visualize the results, the total commutated power as a function of static gain Ge of the single stage boost converter Eq. (29), cascaded boost converters Eq. (25) and the

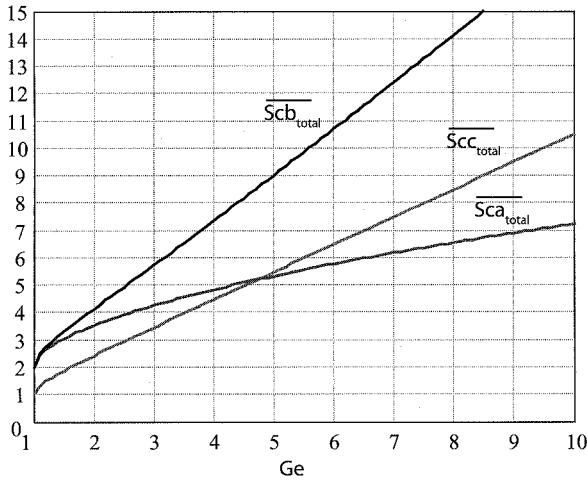


Fig. 4. Converters' total commutated power

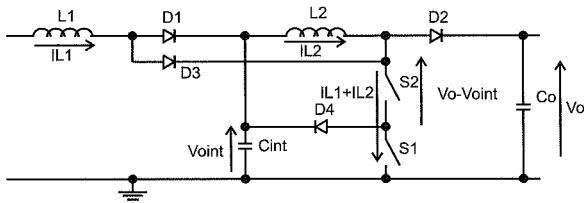


Fig. 5. Three-level quadratic boost converter, reducing the voltage across the switches - Top1A

single switch quadratic boost converter Eq. (26) are presented by Fig. 4. It is clear that the single switch quadratic converter has the highest commutated power. This can be explained by the following reasons. The voltage applied across diode D_3 is the voltage difference between the output voltage and the intermediary voltage and its current is high, because it is related to the input current. But the major problem is related to the active switch, which is submitted to the output voltage and input current I_{L1} added of current I_{L2} , making the relation between the total commutated power and the converter's output power higher. As expected, for the basic boost converter the commutated power becomes ideally higher than the two cascaded converters. This occurs for static gains higher than 4.72.

2.2 Converter Conception By substituting switch S_1 into Fig. 3(b) by two switches and adding a clamping diode D_4 , the converter presented by Fig. 5 (Top1A) can be drawn. The addition of another switch and a clamping diode follows the strategy presented in Ref. (3) to obtain three level topologies based on the basic converters (buck, boost and buck-boost). However those topologies do not present the quadratic characteristic. Now, the applied voltage across each switch is lower than the converter output voltage. But the commutated problem still remains because the input current (I_{L1} current) is being commutated by S_2 and S_1 . Also, there are too many diodes.

By changing the connection of diode D_3 to the connection point between S_1 and S_2 , the current that circulates in S_2 is reduced. This topology is presented in Fig. 6 (Top1B).

Now, for CCM in both inductors, two diodes can be removed from Fig. 6 resulting in the converter presented by Fig. 7 (Top1C). The commutated power of this converter

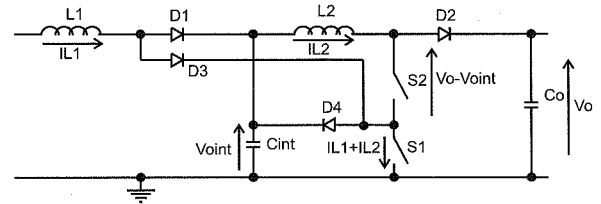


Fig. 6. Three-level quadratic boost converter, reducing the commutated power in S_2 - Top1B

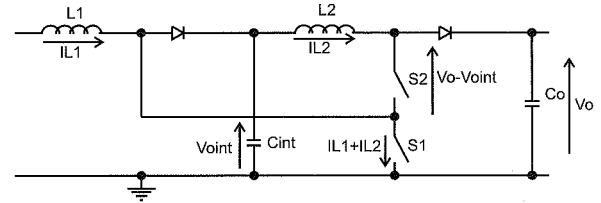


Fig. 7. Three-level quadratic boost converter, reducing the number of diodes - Top1C

is lower than the commutated power of the single switch quadratic converter, while keeping the quadratic characteristic. Also, the voltage across switch S_2 of Top1C is lower than the voltage across switch S_2 of the two cascaded boost converters (Fig. 3(a)). It means that in terms of voltage, the same switch capability can be used for S_1 and S_2 , depending on the required static gain. The drawback is that the current in switch S_1 of the proposed converter is higher than the current in switch S_1 of the two cascaded converters. But the total commutated power is the same, as presented by Eq. (33). The advantage of this converter is that two low voltage switches can be used, with low $R_{DS(on)}$ resistance in case of MOSFET's semiconductors. This converter can also be interesting for input voltages higher than the fuel cell's voltage range or even for use at higher output voltages with IGBTs.

$$\overline{Scd_{tot}}(D) = 2 + \frac{2 - D \cdot \lambda}{1 - D \cdot \lambda} \cdot \sqrt{D \cdot \lambda} + \frac{\lambda \cdot \sqrt{D^3}}{(1 - D)} \dots \dots (30)$$

$$\overline{Scd_{tot}}(D) = 2 + \frac{2 \sqrt{D}}{1 - D} \dots \dots \dots (31)$$

$$Ge \approx \frac{1}{(1 - D)^2} \text{ for } \lambda \rightarrow 1 \dots \dots \dots (32)$$

$$Scd_{tot}(Ge) = 2 \sqrt{Ge - \sqrt{Ge}} + 2 = \overline{Scd_{tot}} \dots \dots \dots (33)$$

3. Operation Principles

To explain the operation principles and analyze theoretically the proposed topology, the continuity of the current in both inductors must be taken into account.

In this paper only the CCM of operation in both inductors will be considered. Future publications shall deal in detail with different modes of operation.

A requirement for proper operation is that the conduction time of switch S_1 must be smaller than switch S_2 conduction time, then a special modulation strategy is necessary. In doing so, the voltage applied to the switch is lower than the output voltage, clamped by the intermediary voltage V_{oint} .

3.1 Topological States and Main Waveforms for CCM

The basic operation of this converter can be divided in four topological states, as depicted in Fig. 8. In the

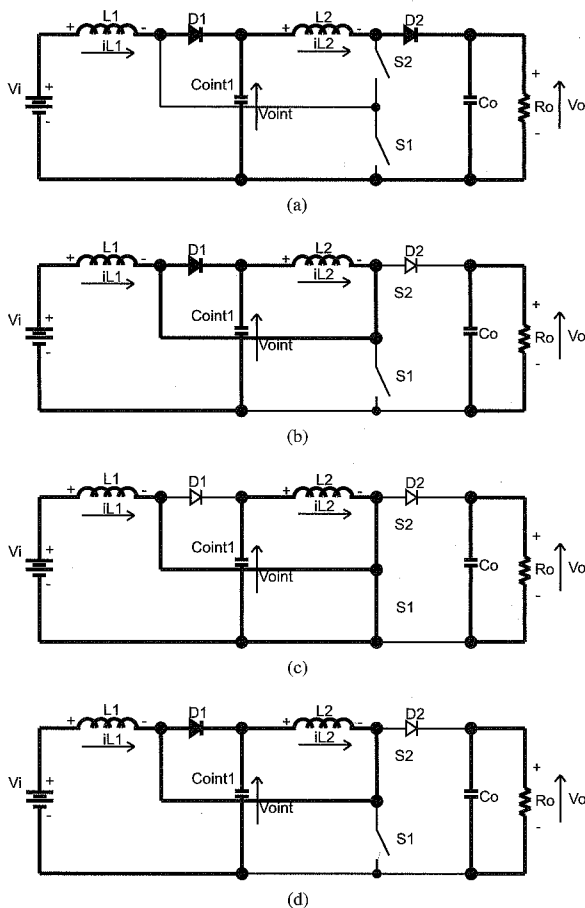


Fig. 8. Topological states of the proposed converter for CCM operation

first topological state, given by Fig. 8(a), both switches are blocked and the energy is being delivered from the power supply to the load. The second topological state is shown in Fig. 8(b). It starts when S_2 is turned on, freewheeling inductor's L_2 current. The voltage across S_1 is equal to V_{oint} . In the third topological state, S_1 is turned-on, starting the accumulation of energy in both inductors L_1 and L_2 . The last topological state starts when S_1 is blocked, one more time the freewheeling topological state takes place.

A vertically centralized modulation strategy can be used to drive the switches, resulting in two degrees of freedom when controlling the output voltage. It means that there are two duty cycles for control purposes. For easier understanding, Fig. 9 shows the main waveforms obtained through simulation for this mode of operation. In this figure the modulation scheme can be identified, including the switches' conduction times Δt_1 and Δt_3 . The voltages across the switches (V_{S1} and V_{S2}) are also shown. As expected they are a half of the output voltage if $V_{oint} \approx \frac{V_o}{2}$.

A non interesting topological state would occur if switch S_1 is turned-on before switch S_2 . The voltage applied across switch S_2 would be greater than $V_o - V_{oint}$ and this converter loses its main advantage. The same undesired situation would happen if switch S_2 is turned-off before S_1 . These two undesired situations result in the same topological state, as presented by Fig. 10.

3.2 Static Gain By inspection of Fig. 9, the static

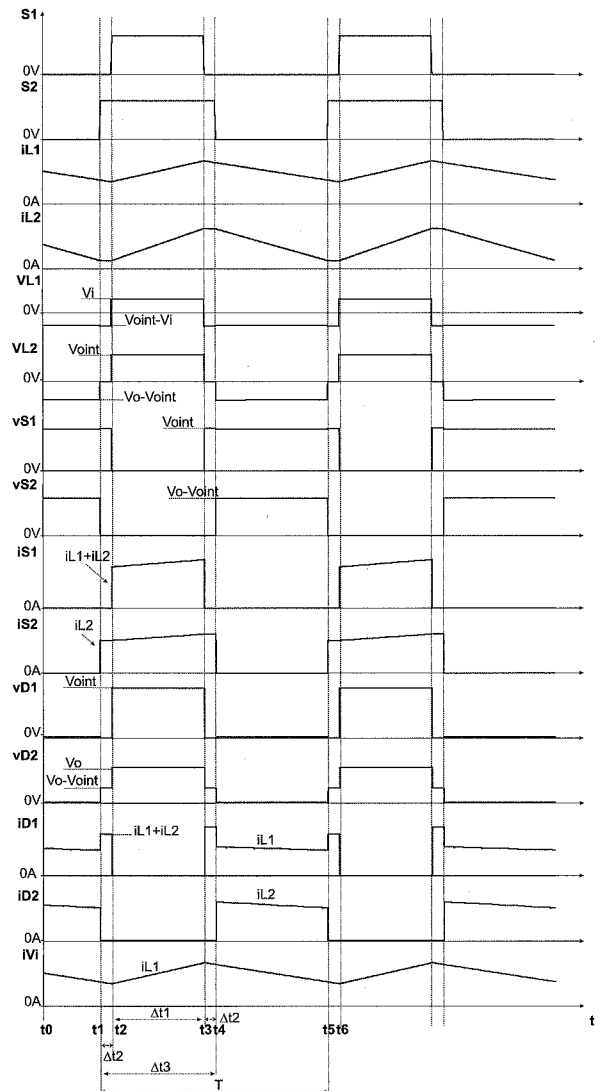


Fig. 9. Main waveforms for CCM operation in both inductors

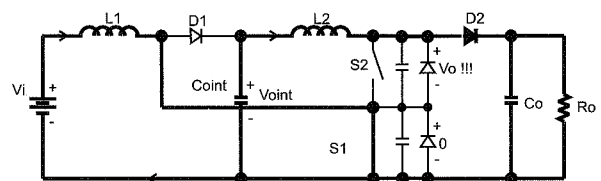


Fig. 10. Undesired topological state

gain of this converter can be obtained, which represents the output voltage variation as a function of the conduction time of each switch. The duty cycle D is defined as being switch S_2 conduction time Δt_3 divided by the switching period T as presented by Eq. (34). As stated before S_1 conduction time Δt_1 must be smaller than Δt_3 . To respect this restriction, a reduction factor λ is applied as shown by Eq. (35). This new variable must be higher than 0 and lower than 1.

$$D = \frac{\Delta t_3}{T} \quad (34)$$

$$\Delta t_1 = \Delta t_3 \cdot \lambda \quad (35)$$

To obtain the static gain, each step-up stage can be analyzed separately, as follows. In steady state the average

voltage across L_1 is equal to zero. Then Eq. (36) can be written, where V_{oint} is the intermediary DC link voltage and V_i is the input voltage. The static gain between the intermediary DC link and the input voltage is determined by Eq. (38). The same procedure is taken to obtain the static gain for the second step-up voltage stage. Considering steady state operation, the average voltage across L_2 is equal to zero as presented by Eq. (39). The partial static gain is given by Eq. (41), where V_o is the output voltage.

By multiplying Eq. (38) by Eq. (41) the total static gain can be obtained as shown by Eq. (42). By applying the limit function in Eq. (42) with $\lambda \rightarrow 1$, Eq. (36) is obtained demonstrating the quadratic characteristic and justifying the designation of "quadratic converter".

$$V_i \Delta_{t_3} \lambda = (V_{oint} - V_i) \cdot (T - \Delta_{t_3} + \Delta_{t_3} - \Delta_{t_1}) \dots (36)$$

$$V_i(D \cdot \lambda) = (V_{oint} - V_i)(1 - D \cdot \lambda) \dots (37)$$

$$\frac{V_{oint}}{V_i} = \frac{1}{1 - D \cdot \lambda} \dots (38)$$

$$V_{oint} \Delta_{t_1} = (V_o - V_{oint}) \cdot (T - \Delta_{t_3}) \dots (39)$$

$$V_{oint} \cdot D \cdot \lambda = (V_o - V_{oint}) \cdot (1 - D) \dots (40)$$

$$\frac{V_o}{V_{oint}} = \frac{D(\lambda - 1) + 1}{1 - D} \dots (41)$$

$$Getot_{ccm} = \frac{V_{oint}}{V_i} \cdot \frac{V_o}{V_{oint}} = \frac{D(\lambda - 1) + 1}{(D \cdot \lambda - 1)(D - 1)} \dots (42)$$

$$\lim_{\lambda \rightarrow 1} (Getot_{ccm}) = \frac{1}{(1 - D)^2} \dots (43)$$

It is interesting to notice in Eq. (38) and Eq. (41) that the static gains $\frac{V_{oint}}{V_i}$ and $\frac{V_o}{V_{oint}}$ are dependent of the conduction time of both switches differently of what happens when using cascaded boost converters. In other words, the output voltage is not only affected by the intermediary voltage and switch S_2 duty cycle but also by switch S_1 conduction time. The influence of S_1 in the output voltage can be clearly visualized in the third topological state of Fig. 8.

The total static gain as a function of the duty cycle with λ as a parameter is presented by Fig. 11. The same static gain is being presented by Fig. 12, but as a function of λ and with D as parameter. From both figures one can see that for a large static gain variation, acceptable values of λ and D can be used.

The choice of D and λ can be based in different criteria according with designer intentions. If the idea is to keep switches' voltages evenly shared, i.e. with the same magnitude, then the relation between the output voltage and the intermediary voltage that is given in Eq. (44) must be respected. By substituting Eq. (44) into Eq. (41), duty cycle D can be recalculated as a function of λ , yielding Eq. (45). Since λ can only physically vary from nearly 0 to nearly 1, duty cycle D , resulting from Eq. (45), can vary from 1 to 0.5 only. So, for the maximum value of λ , which is 1, the duty cycle D would be 0.5. Substituting these values into the total static gain equation Eq. (42), the maximum gain that still provides an evenly shared switches' voltages is equal to 4, as shown by Eq. (46). The minimum gain while having an equal voltage across the switches occurs for $\lambda \approx 0.001$ and $D \approx 0.990$; for this case the static gain is equal to 2.

$$\frac{V_o}{V_{oint}} = 2 \dots (44)$$

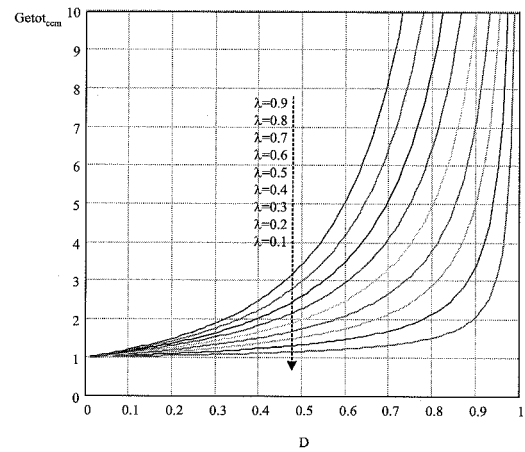


Fig. 11. CCM static gain as a function of D with λ as parameter

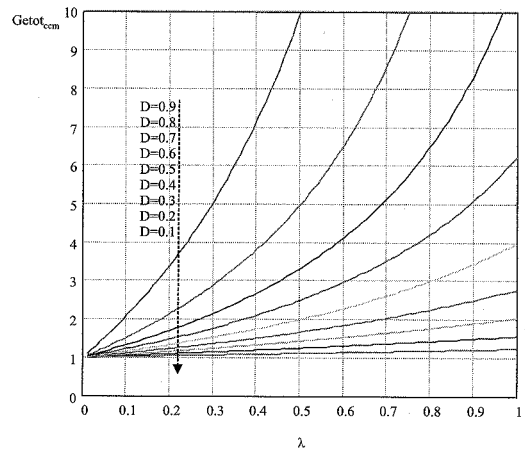


Fig. 12. CCM static gain as a function of λ with D as parameter

$$D(\lambda) = \frac{1}{1 + \lambda} \dots (45)$$

$$Ge_{max}(D = 0.5, \lambda = 1) = 4 \dots (46)$$

But, the static gain of this converter can ideally be higher than 4 or lower than 2, in these cases, the voltages across the switches will not be evenly shared anymore. That should not be considered as a drawback, because the current of S_1 is higher than the current in S_2 , so it could be interesting to have a situation where the voltage across S_2 is higher than the voltage across S_1 , keeping the same commutated power at both switches. Another possibility to wisely chose the values for D and λ would be by minimizing the converter losses, or at least switches losses.

Yet another possibility, would be to minimize the voltage difference among switches ($V_{S2} - V_{S1}$). This could be easily reached by maximizing λ since the voltage difference decreases with a higher λ (Eg. $\lambda = 0.990$) and then calculating D for a given static gain.

A numerical example is given here, where the voltage difference across the active switches is minimized when a static gain equal to 8 is required. Considering an input voltage equal to 25 V and an output voltage equal to 200 V, λ could be kept constant and equal to 0.990, while D would be automatically controlled to regulate the output voltage. This

procedure would give a $D = 0.65$ and an ideal static gain equal to 7.962. The intermediary gains are not individually higher than 4, which seems feasible from the technological point of view. Yet the voltage difference across the switches is the smallest possible value for the specifications given above.

In other words, the choice of λ and D should be made according with the converter specifications and the application requirements, probably targeting at the highest efficiency possible. This topic is not deeply discussed here because it is not within the main goal of the paper.

4. Simulation Results

In order to validate the commutated power equations and the operation principles of the proposed converter, the TL-Q converter, the single switch boost converter and the two cascaded converters were simulated to investigate their devices stress. The presented values were obtained by simulating all converters with an input voltage of 24 V, output voltage equal to 96 V and output power equal to 500 W. The intermediary voltage was equal to 48 V. Inductances L_1 and L_2 equal to $120\mu\text{H}$ and $250\mu\text{H}$ respectively. A summary of these results is presented in Table 1, where Top1C is the new converter, Top2 is the two-cascaded boost converter and Top3 is the single switch quadratic boost converter. One can

Table 1. Converters' simulation results. Top1C: proposed converter; Top2: two cascaded boost converters; Top3: single switch quadratic boost converter

Stresses	Topologies		
	Top1C	Top2	Top3
$IS1_{avg}$	15.18 A	10.267 A	15.28 A
$IS2_{avg}$	5 A	5 A	-
$IS1_{rms}$	21.3 A	14.4 A	21.37 A
$IS2_{rms}$	7.02 A	7.03 A	-
$VS1$	48.8 V	48.8 V	96.62 V
$VS2$	48.8 V	97.8 V	96.62 V
$ID1_{avg}$	9.8 A	9.8 A	9.8 A
$ID2_{avg}$	4.82 A	4.82 A	4.82 A
$ID3_{avg}$	-	-	10.257 A
$VD1$	48 V	48 V	48 V
$VD2$	96 V	96 V	96 V
$VD3$	-	-	48 V
SC_{tot}/Po	4.63	4.63	6.98

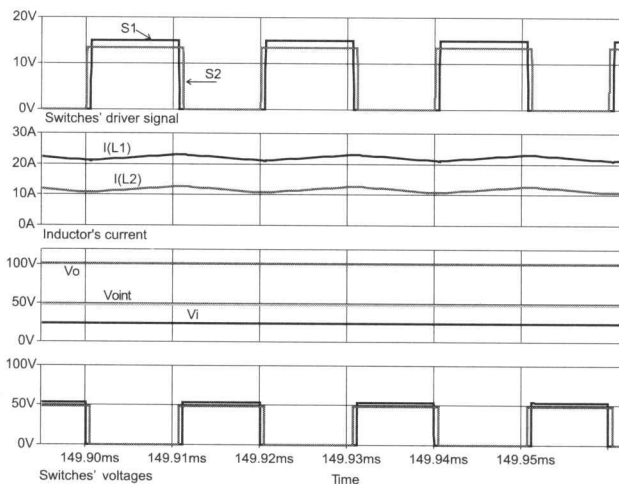


Fig. 13. TL-Q Simulation results operating in CCM

see that the relation between the output power and the commutated power is worst for the single switch quadratic boost converter. Comparing the obtained results for both, Top1C and Top2 topologies, the current stress of switch S_1 is higher in Top1C converter. However, the blocking voltage of switch S_2 is lower in the new converter. Due to these facts, the total commutated power is the same for both converters.

In Fig. 13 the TL-Q (Top1C) converter waveforms obtained by simulation are shown. The output power is 500 W, the input voltage is 25 V, the intermediary voltage was set to 50 V and the output voltage is 100 V. Switching frequencies of both modulators are equal to 50 kHz. The chosen duty cycle was 0.55 and parameter λ was set to 0.9.

It is important to mention that the voltages across the switches are perfectly clamped when considering this ideal circuit, so the concept of being a three-level converter is validated.

5. Experimental Results

The proposed converter has been implemented to validate its principle of operation for 25 V input voltage and 100 V output voltage. The maximum output power is 450 W and the chosen switching frequency is 50 kHz. The value of λ is constant and near 0.9. A picture of the prototype is shown by Fig. 14. The following semiconductors were installed: IRFB4710 from the industry International Rectifier, MUR1520 and MUR820 both from the industry ON Semiconductor.

In Fig. 15 are presented the input current and the input voltage. Since the converter is operating in CCM, the ripple current is very small, what is interesting for fuel cell applications. If less ripple is required by the application, the input inductance could be increased, a capacitor could be added to the input (operating as a filter by considering the fuel cell impedance) or interleaved converters could be used. The output voltage and output current are being presented by Fig. 16. Note that the output voltage is around 100 V.

The switches' voltages are being presented by Fig. 17. In this figure one can see that none of the switches are being submitted to the highest converter voltage, which is 100 V. During the turn off commutation, an overvoltage occurs, which is justified by the utilization of a non appropriate layout design for this converter. After the turn-off transient it is

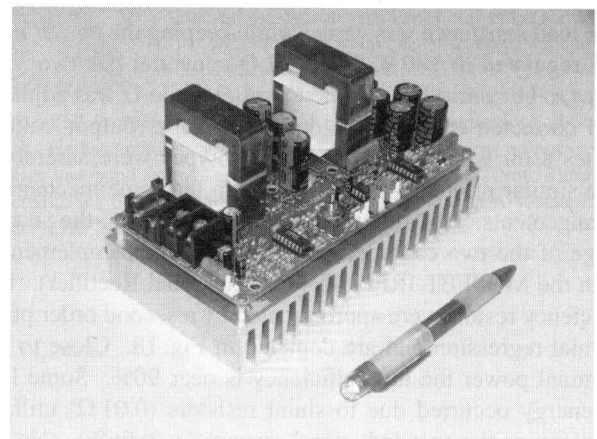


Fig. 14. Picture of the prototype

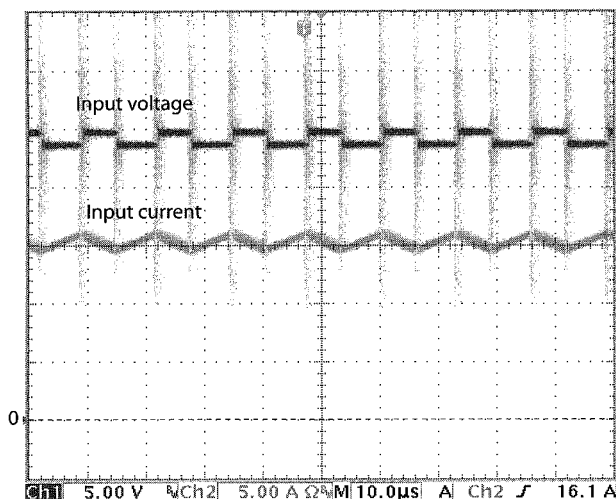


Fig. 15. Converter's input voltage (5 V/div) and current (5 A/div)

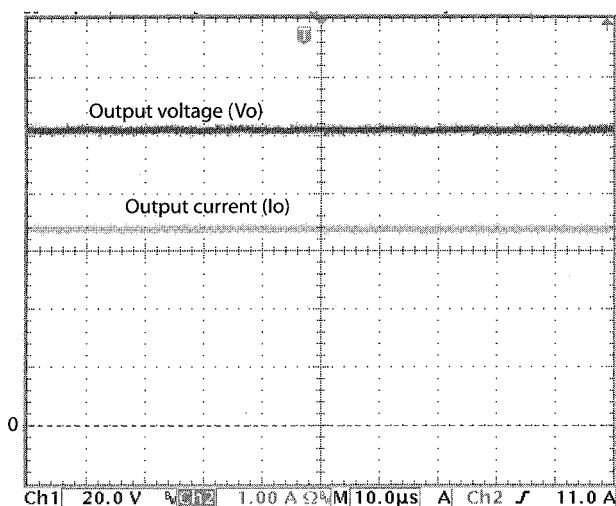


Fig. 16. Converter's output voltage (20 V/div) and current (1 A/div)

possible to see that the switch's voltages are clamped, validating the proposal of this work. Any kind of auxiliary snubber circuit was used to help the commutations.

5.1 Efficiency The efficiency of the T-LQ converter and the efficiency of two cascaded converters were obtained by supplying both converters with a fixed voltage, set to 25 V. The load resistance was varied while keeping the output voltage regulated to 100 V. Since T-LQ converter has two variables to be controlled, λ was set to 0.9 while D was adjusted and corrected to reach the desired voltage (output voltage varies a bit with power). Both prototypes were assembled in a similar printed circuit board, with the same mechanical arrangements. But, due to voltage requirements, the second stage of the two cascaded converter has been implemented with the MOSFET IRFP260N (International Rectifier). The efficiency results were approximated by a second order polynomial regression and are depicted in Fig. 18. Close to the nominal power the total efficiency is near 90%. Some loss of energy occurred due to shunt resistors (0.01Ω) utilized to measure the two inductors' current ($\approx 0.96\%$). No efforts were done to improve the efficiency by using snubber or

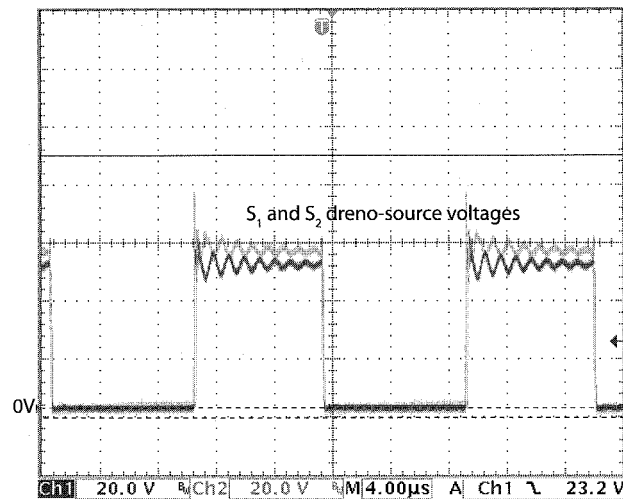


Fig. 17. S_1 and S_2 voltages, switching at 50 kHz and 485 W

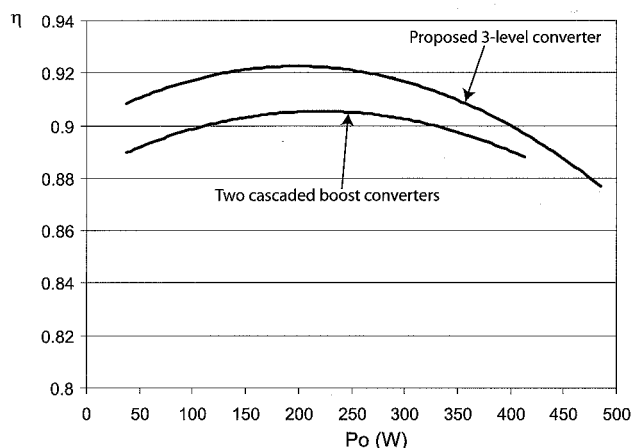


Fig. 18. Converter's efficiency comparison

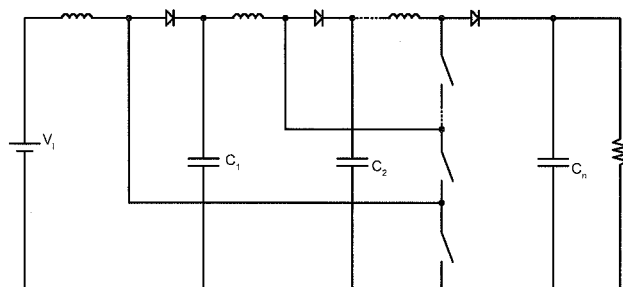


Fig. 19. Multilevel topology

commutation techniques, since the applied voltage is not so high. The efficiency of this converter, when compared with the two boost cascaded converters, is lightly higher. These results were obtained by using the same printed circuit board and the same components, except switch for S_2 . Also, the installed semiconductor power of the two cascaded boost converter was 1000 VA, while the installed semiconductor power of the proposed converter was 750 VA. I.e., for the same installed semiconductor power, the efficiency of the proposed converter could be even higher.

5.2 Multilevel Converters Other number of levels and higher values of output voltage can be obtained with the multilevel circuit presented in Fig. 19. The voltage across the

active switches are determined by the difference between the capacitors' voltages.

The duty cycle of the upper switch must have the highest value, while the duty cycle of the lowest switch has the smallest value. Since the total efficiency of these converters seems to be affected by the cascaded connection, a great number of levels may become unattractive. Of course this depends on the application and electrical specifications.

6. Conclusion

The integration of two boost cascaded converters is presented in this paper originating three new quadratic three-level converters. The main advantage of the proposed topology, when compared with the single switch quadratic boost converter, is that the total installed semiconductor power is lower. When comparing the presented topology with two cascaded boost converters, the voltage across the switch S_2 is lower in the proposed converter, while the current in switch S_1 is higher, keeping the same semiconductor installed power.

The presented converter can be interesting for applications where a high voltage ratio is necessary, what can be the case of fuel cell applications, but only when transformer isolation is not required. This converter can be also interesting for higher power and higher output voltages. A generalization to obtain multilevel converters based on the same commutation cell was also presented. Future works shall deal with the buck and buck-boost converters based on the same commutation cell, discontinuous conduction mode of operation, modeling issues and inductors coupling.

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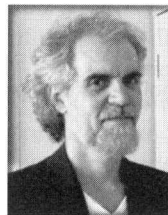
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Yales Rômulo De Novaes (Non-member) was born in Indaial, Santa Catarina, Brazil, in 1974. In 1999 he received the bachelor degree in electrical engineering from Regional University of Blumenau, Santa Catarina, Brazil. The M.Eng. and Dr. degrees were obtained from Power Electronics Institute (INEP) of the Federal University of Santa Catarina (UFSC) in 2000 and 2006, respectively. During 2001, he worked as a development engineer in the same institute. In 2006 he joined the Industrial Electronics Laboratory, EPFL as scientific collaborator. Dr. De Novaes is member of the Brazilian power electronics society (SOBRAEP) and IEEE PELS.



Ivo Barbi (Non-member) was born in Gaspar, Santa Catarina, Brazil, in 1949. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1973 and 1976, respectively, and the Dr.Eng. degree from the Institut National Polytechnique de Toulouse, France, in 1979. He founded the Brazilian Power Electronics Society, the Power Electronics Institute of the Federal University of Santa Catarina, and created the Brazilian Power Electronics Society. Currently, he is a Professor with the Power Electronics Institute, Federal University of Santa Catarina. Dr. Barbi has been an Associate Editor in the Power Converters Area of the IEEE Transactions on Industrial Electronics since 1992.



Alfred Rufer (Non-member) was born in Diessbach, Switzerland, in 1951. He received the M.S. degree from the Swiss Federal Institute of Technology Lausanne (EPFL), Lausanne, Switzerland, in 1976. In 1978, he joined ABB, Turgi, Switzerland, where he was involved in the fields of power electronics and control, such as high-power variable-frequency converters for drives. In 1985, he was a Group Leader involved with power-electronic development in ABB. In 1993, he became an Assistant Professor at EPFL. Since 1996, he has been a full Professor and Head of the Industrial Electronics Laboratory, EPFL. He has authored or co-authored several publications on power electronics and applications, and he holds several patents. Prof. Rufer was elected to the IEEE Fellow grade in 2006 and became an Associate Editor of the IEEE Transactions on Power Electronics in 2007.

