

Modeling and Digital Control of a Single-Stage Step-Up/Down Isolated PFC Rectifier

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Abstract—This paper presents the dynamic modeling and digital control of a single-stage isolated current rectifier with power factor correction based on the integration of full-bridge and flyback converters. This converter is designed to operate with adjustable output voltage so that it can operate in two distinct operation modes, depending on the input and output voltages. Therefore, small-signal state-space average models are obtained for the converter operating in step-down and step-up operation modes, and analysis and design of the digital control system are included for different operating points. Experimental results based on a 3-kW prototype are presented to validate the proposed control system under distinct conditions.

Index Terms—Digital control, isolated rectifier, power factor correction (PFC).

I. INTRODUCTION

ISOLATED power factor corrected ac–dc converters have been widely used in active front-end converters [1]. These converters are designed to guarantee galvanic isolation and regulated output voltage as well as to draw input current with sinusoidal waveform in compliance to international standards [2]. Two-stage converters have been normally used in these applications, where a pre-regulator converter with power factor correction (PFC) is cascaded to a dc–dc isolated converter [3]–[9]. These PFC circuits offer excellent performance in terms of input power factor, holdup time capability, and efficiency, but their power density are normally reduced.

Cost-effective high-density solutions for isolated ac–dc PFC are the single-stage isolated converters (SSIC). SSICs normally present fewer components than two-stage converters but their analysis and design are usually more complex [10]–[27]. Several SSICs have been proposed in the literature, including small power converters operating mainly in discontinuous conduction mode (DCM) [10]–[20] and higher power converters in continuous conduction mode (CCM) [21]–[27]. Among SSICs operating in CCM, the full-bridge-flyback (FBF) isolated current rectifier presents some features that make it attractive for many

applications, such as constant switching frequency, step-down and step-up operation, high-power-level capability, and the absence of an auxiliary pre-loading circuit to control the inrush current [27].

From the control point of view, cascaded control structures have been used to control PFC SSICs [23], [28]. Many design techniques for this control scheme have been developed. However, as in nonisolated converters, the main difficulties to design these control loops are the availability of proper dynamic models and the operation in distinct points [16], [29], [30].

On the other hand, digital control techniques have been widely used in SSICs when the converter has complex modulation strategies. For this FBF isolated current rectifier, the digital implementation is particularly attractive because this converter is designed to operate with adjustable output voltage. As a result, a single microcontroller can be used for reference generation, control, and modulation.

Due to these facts, this paper proposes a digital control system for an ac–dc PFC circuit based on the isolated integrated FBF topology [27], which can operate in a wide output voltage range and in two distinct operation modes. Small-signal state-space average models for step-up and step-down modes are presented so that it is possible to design and to analyze the digital control system in different operating points. Experimental results for a 3-kW converter are included to validate the proposed control technique in both operation modes.

This paper is organized as follows. Section II shows the system description, including the converter features and control loop structure. Section III presents the small-signal state-space averaged models from duty ratio to input current of the converter in both operating modes, while Section IV shows the input-current-to-output-voltage small-signal model. Section V describes the control design methodology and analysis of the closed-loop system. Finally, Section VI presents some experimental results to validate the proposed control scheme.

II. SYSTEM DESCRIPTION

Here, we show the main features, modulation strategy, and control structure of the FBF isolated current rectifier.

A. Circuit Operation

Fig. 1 shows a simplified diagram of the closed-loop isolated rectifier. The converter is composed of an input full-bridge diode rectifier (D_1 , D_2 , D_3 and D_4), a flyback coupled inductor (L_c), four switches (S_1 , S_2 , S_3 , and S_4), a full-bridge transformer (T_1), two flyback diodes (D_5 and D_6), an output full-bridge rectifier (D_7 , D_8 , D_9 , and D_{10}), and an output filter capacitor (C_o). A unitary turns ratio is assumed for the transformer T_1 and for the coupled inductor L_c .

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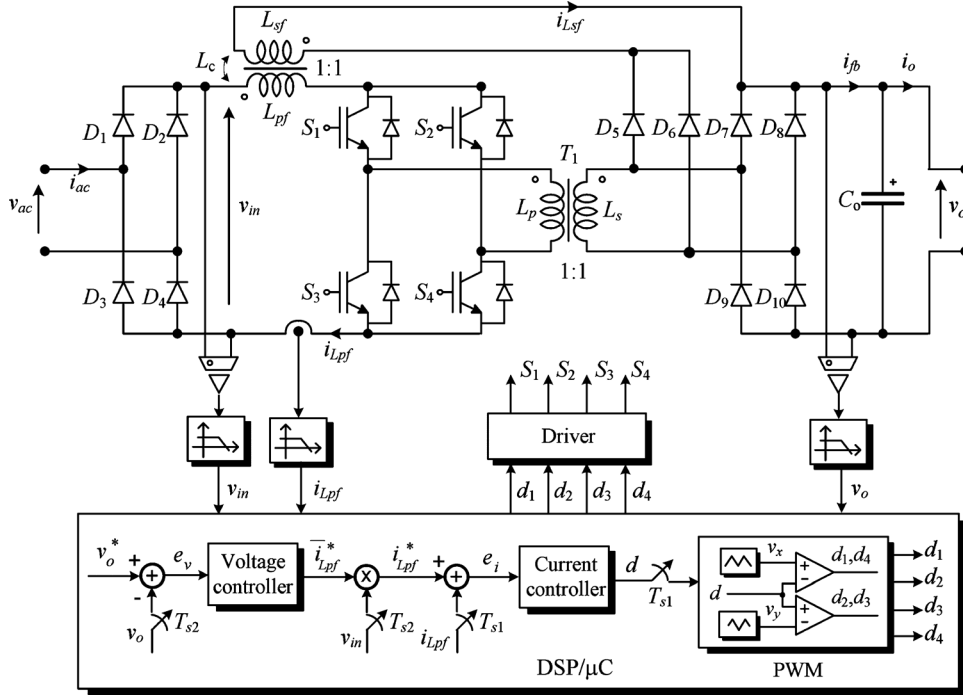


Fig. 1. Simplified diagram of the SSIC including digital control.

This converter is designed to operate in CCM. It is worth mentioning that the definition of the conduction mode is related to the magnetizing current i_{Lc} , equal to $i_{Lpf} + i_{Lsf}$, as shown in Fig. 2, where i_{Lpf} and i_{Lsf} are the primary and secondary currents of the coupled inductor L_c . For this conduction mode, there are two different operation modes depending on the input and output voltage levels. The converter operates in step-up mode when the rectified input voltage (v_{in}) is less than the output voltage referred to the primary side of the transformer (v_o'). On the other hand, the converter operates in step-down mode when the input voltage is higher than v_o' . Assuming unitary turns ratios ($N = 1$) for T_1 and L_c , the transition between the operation modes occurs when the duty ratio is 0.5 [27].

Pulsewidth modulation (PWM) strategy can be applied to this converter. Two comparators and two triangular waveforms with a 180° phase shift between them are used, as presented in Fig. 1. The command signals of S_1 and S_4 are obtained from the comparison of the input d with one triangular waveform (v_x), while the command signals of S_2 and S_3 are obtained from the comparison of d with the other one (v_y). The resulting pulse-width modulation patterns for step-up and step-down operating modes are shown in Fig. 2.

FBF isolated current rectifier can be analyzed as a dc-dc converter assuming that switching frequency is much higher than the input voltage frequency. From these considerations, the input-to-output voltage conversion ratio can be derived for step-up and step-down operation modes, respectively, as follows:

$$M_{up} = \frac{V_o}{V_{in}} = \frac{D}{1-D} \quad (1)$$

$$M_{down} = \frac{V_o}{V_{in}} = 2D \quad (2)$$

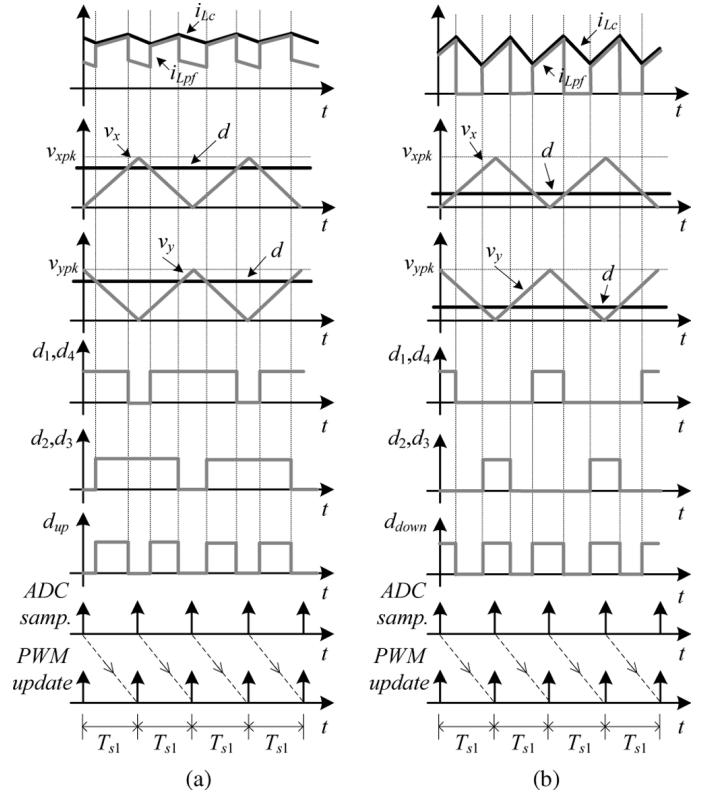


Fig. 2. PWM pattern. (a) Step-up mode. (b) Step-down mode.

where V_o is the output voltage, V_{in} is the input voltage, and $D = d/v_{xpk} = d/v_{ypk}$ is the duty ratio.

From (1) and (2), one can observe the same input-to-output voltage conversion ratio when $D = 0.5$. Consequently, this con-

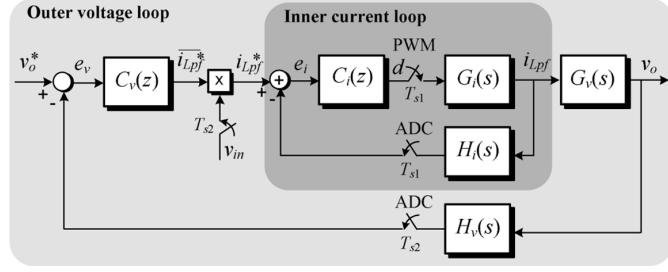


Fig. 3. Digital control structure.

verter presents a smooth transition between step-up and step-down operating modes.

B. Control Structure

Fig. 1 presents the digital control structure considered in this investigation. This control technique uses two cascaded control loops, as detailed in Fig. 3: an inner current loop, which is used to track the input current reference, and an outer voltage loop to guarantee a regulated output voltage.

Section III will show that the duty ratio to input current model of this converter depends on the operation point as well as on the converter operation modes (step-up or step-down). Moreover, when V_o is smaller than the peak value of the input voltage, this converter cyclically commutates between these operation modes. Many approaches have been used to solve this problem, such as gain scheduling control and switching control. In this paper, since there is a smooth transition between the operation modes, a single linear current controller is used for both modes.

For proper operation of both control loops, it is presumed the dynamic decoupling (time-scale separation) between the current and voltage dynamics [31], [32]. In PFC converters, most designs guarantee timescale separation using a small input inductance L_c and a large output capacitor C_o . In this case, the input current has a dynamic behavior that is much faster than the output voltage.

The digital control system samples the input current i_{Lpf} and updates the control action d twice in each PWM period, as shown in Fig. 2. As can be seen, it uses one sampling period to calculate the control action, which is updated at the next sampling instant. On the other hand, the output voltage v_o and the input voltage v_{in} are sampled and updated once in ten switching periods. As shown in Fig. 1, the sampled signals are filtered before the analog-to-digital conversion, and dynamics of these filters are considered in the control system design.

III. DUTY RATIO TO INPUT CURRENT MODEL

Here, we present a linear-time invariant (LTI) small-signal duty ratio to input current model of the FBF isolated current rectifier, which is necessary to design the inner current loop. The following hypotheses are assumed.

- 1) $v_{in}(t)$ is an ideal sinusoidal voltage source with constant magnitude during each switching period T_s .
- 2) $v_o(t)$ is constant, i.e., $v_o(t) = V_o$.
- 3) $i_{Lsf}^*(t) = \alpha v_{in}(t)$, where α is constant during each half low-frequency fundamental period.
- 4) Unitary turns ratios ($N = 1$) for T_1 and L_c .
- 5) Converter operates in CCM in relation to the magnetizing current $i_{Lc}(t)$.

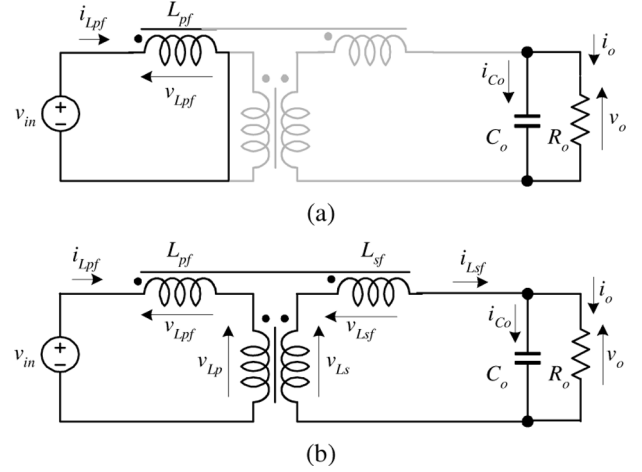


Fig. 4. Equivalent representation of the converter operating in step-up mode. (a) Operation stage 1. (b) Operation stage 2.

- 6) High-frequency harmonics generated by switching are neglected.
- 7) All components are lossless.

The modeling technique is based on the piecewise-linear state-space representation for each operation stage and on state-space averaged model of the converter around a quiescent operating point [33].

A. Step-Up Mode

Fig. 4 shows equivalent circuits for the four operation stages of the FBF isolated current rectifier operating in step-up mode [27]. Fig. 4(a) shows the equivalent circuit when all switches are simultaneously on, while Fig. 4(b) presents the equivalent circuit when S_1 and S_4 or S_2 and S_3 are off. Consequently, one can obtain an equivalent command signal d_{up} for this mode, shown in Fig. 2(a), whose duty ratio is

$$D_{up} = 2D - 1. \quad (3)$$

The state-space averaging method requires a common set of state variables for all equivalent circuits. Both equivalent circuits have two independent states if T_1 is assumed as an ideal transformer. To derive the state-space averaged model of the FBF current rectifier operating in CCM, the magnetizing current of the coupled inductor $i_{Lc}(t)$ has been considered as state variable, since the input current $i_{Lpf}(t)$ cannot be directly used due to its discontinuous characteristic. Moreover, the output voltage $v_o(t)$ is the other state variable. As a result, the state variables, input and output are defined, respectively, as follows:

$$\mathbf{x}(t) = [i_{Lc}(t) \quad v_o(t)]^T \quad (4)$$

$$u(t) = [v_{in}(t)] \quad (5)$$

$$y(t) = [i_{Lc}(t)] \quad (6)$$

where the magnetizing current is given by

$$i_{Lc}(t) = i_{Lpf}(t) + i_{Lsf}(t). \quad (7)$$

The linear state-space models are given by

$$\begin{cases} \mathbf{K} \frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_i \mathbf{x}(t) + \mathbf{B}_i u(t) \\ y(t) = \mathbf{C}_i \mathbf{x}(t) + \mathbf{E}_i u(t) \end{cases}, \quad i = 1, 2 \quad (8)$$

where i represent the operation stage and

$$\mathbf{K} = \begin{bmatrix} L_c & 0 \\ 0 & C_o \end{bmatrix}. \quad (9)$$

The state equation matrices for the operation stage 1 are

$$\begin{aligned} \mathbf{A}_1 &= \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{R_o} \end{bmatrix} \\ \mathbf{B}_1 &= \begin{bmatrix} 1 \\ 0 \end{bmatrix} \\ \mathbf{C}_1 &= [1 \quad 0] \\ \mathbf{E}_1 &= [0]. \end{aligned} \quad (10)$$

On the other hand, for the operation stage 2, the state equation matrices are given by (see Appendix I)

$$\begin{aligned} \mathbf{A}_2 &= \begin{bmatrix} 0 & \frac{-1}{2} \\ \frac{1}{2} & \frac{-1}{R_o} \end{bmatrix} \\ \mathbf{B}_2 &= \begin{bmatrix} \frac{1}{2} \\ 0 \end{bmatrix} \\ \mathbf{C}_2 &= [1 \quad 0] \\ \mathbf{E}_2 &= [0]. \end{aligned} \quad (11)$$

The linearized ac averaged model of the converter around a quiescent operating point is obtained from [33]

$$\begin{cases} \mathbf{K} \frac{d\hat{\mathbf{x}}(t)}{dt} = \mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\hat{u}(t) + \mathbf{B}'\hat{d} \\ y(t) = \mathbf{C}\hat{\mathbf{x}}(t) \end{cases} \quad (12)$$

where

$$\mathbf{A} = (2D - 1)\mathbf{A}_1 + (2 - 2D)\mathbf{A}_2 \quad (13)$$

$$\mathbf{B} = (2D - 1)\mathbf{B}_1 + (2 - 2D)\mathbf{B}_2 \quad (14)$$

$$\mathbf{C} = (2D - 1)\mathbf{C}_1 + (2 - 2D)\mathbf{C}_2 \quad (15)$$

$$\mathbf{B}' = 2(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + 2(\mathbf{B}_1 - \mathbf{B}_2)U \quad (16)$$

$$\mathbf{X} = -\mathbf{A}^{-1}\mathbf{B}U. \quad (17)$$

This model is valid for small ac variations around an equilibrium point, where the steady-state values for D , U , Y , and $\mathbf{X}$ are known. So, the transfer function from control to coupled inductor current can be obtained from

$$Y(s) = [\mathbf{C}(s\mathbf{I} - \mathbf{K}^{-1}\mathbf{A})^{-1}\mathbf{K}^{-1}\mathbf{B}']U(s). \quad (18)$$

This transfer function can be rewritten as

$$\hat{G}_{Lcd}(s) = \frac{\hat{i}_{Lc}(s)}{\hat{d}(s)} = k_u \frac{b_{u1}s + b_{u0}}{a_{u2}s^2 + a_{u1}s + a_{u0}} \quad (19)$$

where

$$\begin{aligned} k_u &= \frac{V_{in}}{R_o(1-D)^2} & a_{u2} &= L_c R_o C_o \\ a_{u1} &= L_c & a_{u0} &= R_o(1-D)^2 \\ b_{u1} &= C_o R_o^2(1-D) & b_{u0} &= R_o(1-D^2). \end{aligned} \quad (20)$$

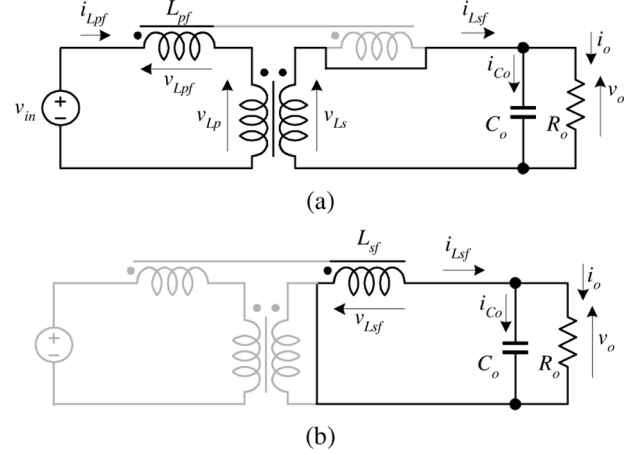


Fig. 5. Equivalent model of the converter operating in step-down mode. (a) Operation stage 1. (b) Operation stage 2.

On the other hand, from Fig. 2(a), one can observe that the relation between the averaged input current $i_{Lpf}(t)$ and averaged magnetizing current $i_{Lc}(t)$ is given by

$$\langle i_{Lpf}(t) \rangle = [2d(t) - 1] \langle i_{Lc}(t) \rangle + [2 - 2d(t)] \frac{\langle i_{Lc}(t) \rangle}{2}. \quad (21)$$

Applying small perturbations in (21) and neglecting the dc and second-order nonlinear terms, one can obtain the following linearized equation:

$$\hat{i}_{Lpf}(s) = D\hat{G}_{Lcd}(s)\hat{d}(s) + I_{Lc}(D)\hat{d}(s) \quad (22)$$

where (see Appendix II)

$$I_{Lc}(D) = \frac{2V_o^3}{R_o V_{in}^2 \text{pk}} \frac{1-D}{D^2}. \quad (23)$$

Substituting (19) and (23) into (22) yields

$$G_i(s) = \frac{\hat{i}_{Lpf}(s)}{\hat{d}(s)} = \frac{c_{u2}s^2 + c_{u1}s + c_{u0}}{a_{u2}s^2 + a_{u1}s + a_{u0}} \quad (24)$$

where

$$\begin{aligned} c_{u2} &= a_{u2}I_{Lc}(D) \\ c_{u1} &= Dk_u b_{u1} + a_{u1}I_{Lc}(D) \\ c_{u0} &= Dk_u b_{u0} + a_{u0}I_{Lc}(D). \end{aligned} \quad (25)$$

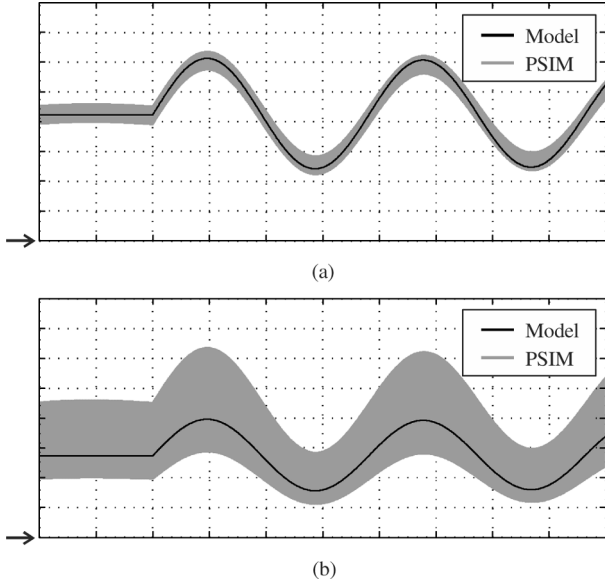
B. Step-Down Mode

Fig. 5 presents the equivalent circuits for the four operation stages of the FBF isolated current rectifier operating in step-down mode. Fig. 5(a) shows the equivalent circuit when S_1 and S_4 , or S_2 and S_3 are on, while Fig. 5(b) presents the equivalent circuit when all switches are simultaneously off. From the equivalent circuit representation, an equivalent command signal d_{down} is derived, shown in Fig. 2(b), whose duty ratio is given by

$$D_{\text{down}} = 2D. \quad (26)$$

TABLE I
CONVERTER PARAMETERS

$P_o = 3 \text{ kW}$	Nominal output power
$V_o = 400 \text{ V}$	Nominal output voltage
$V_{rms} = 220 \text{ V}$	Nominal rms input voltage
$f_i = 60 \text{ Hz}$	Input frequency
$f_s = 100 \text{ kHz}$	Switching frequency
$R_o = 53.3 \text{ } \Omega$	Nominal load resistance
$C_o = 2900 \text{ } \mu\text{F}$	Output converter capacitance
$L_{pf} = L_{sf} = L_c = 100 \text{ } \mu\text{H}$	Input converter inductance

Fig. 6. Comparison between small-signal averaged model of the FBF current rectifier in step-up mode and PSIM simulation (5 A/div, 2.5 ms/div). (a) Magnetizing current i_{Lc} . (b) Input current i_{Lpf} .

The state-space averaged model of the converter in step-down mode is also derived from the magnetizing current of the coupled inductor $i_{Lc}(t)$. As a result, the state, input and output variables are given by (4)–(6). The matrices equations for both operation stages are given by

$$\mathbf{A}_1 = \begin{bmatrix} 0 & -1 \\ 1 & \frac{-1}{R_o} \end{bmatrix} \quad \mathbf{B}_1 = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \quad \mathbf{C}_1 = \begin{bmatrix} 1 & 0 \end{bmatrix} \quad \mathbf{E}_1 = [0] \quad (27)$$

$$\mathbf{A}_2 = \begin{bmatrix} 0 & -1 \\ 1 & \frac{-1}{R_o} \end{bmatrix} \quad \mathbf{B}_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad \mathbf{C}_2 = \begin{bmatrix} 1 & 0 \end{bmatrix} \quad \mathbf{E}_2 = [0] \quad (28)$$

and $\mathbf{K}$ is given by (9).

The linearized ac averaged model of the converter around a quiescent operating point is also described by (12), where

$$\mathbf{A} = 2D \mathbf{A}_1 + (1 - 2D) \mathbf{A}_2 \quad (29)$$

$$\mathbf{B} = 2D \mathbf{B}_1 + (1 - 2D) \mathbf{B}_2 \quad (30)$$

$$\mathbf{C} = 2D \mathbf{C}_1 + (1 - 2D) \mathbf{C}_2 \quad (31)$$

and $\mathbf{B}'$ and $\mathbf{X}$ are given by (16) and (17), respectively.

Using (12), (16)–(18), and (29)–(31), the resulting transfer function from duty ratio to magnetizing current can be obtained:

$$\hat{G}_{Lcd}(s) = \frac{\hat{i}_{Lc}(s)}{\hat{d}(s)} = k_d \cdot \frac{b_{d1}s + b_{d0}}{a_{d2}s^2 + a_{d1}s + a_{d0}} \quad (32)$$

where

$$\begin{aligned} k_d &= \frac{V_o}{(L_c D)} & a_{d2} &= R_o C_o \\ a_{d1} &= 1 & a_{d0} &= \frac{R_o}{L_c} \\ b_{d1} &= R_o C_o & b_{d0} &= 1. \end{aligned} \quad (33)$$

Moreover, the relation between the averaged input current $i_{Lpf}(t)$ and the averaged magnetizing current $i_{Lc}(t)$ is given by

$$\langle i_{Lpf}(t) \rangle = 2 \langle d(t) \rangle \langle i_{Lc}(t) \rangle. \quad (34)$$

Applying small perturbations in (34) and neglecting the dc and second-order nonlinear terms [33], one can obtain the following linearized equation:

$$\hat{i}_{Lpf}(s) = 2D \hat{G}_{Lcd}(s) \hat{d}(s) + 2I_{Lc}(D) \hat{d}(s) \quad (35)$$

where, from a similar analysis presented in Appendix II for the boost mode, one can verify that

$$I_{Lc}(D) = \frac{V_o^3}{2R_o D^2 V_{in\text{ pk}}^2}. \quad (36)$$

Substituting (36) and (32) into (35) results in

$$G_i(s) = \frac{\hat{i}_{Lpf}(s)}{\hat{d}(s)} = \frac{c_{d2}s^2 + c_{d1}s + c_{d0}}{a_{d2}s^2 + a_{d1}s + a_{d0}} \quad (37)$$

where

$$\begin{aligned} c_{d2} &= 2I_{Lc}(D) a_{d2} \\ c_{d1} &= 2D k_d b_{d1} + 2a_{d1} I_{Lc}(D) \\ c_{d0} &= 2D k_d b_{d0} + 2a_{d0} I_{Lc}(D). \end{aligned} \quad (38)$$

C. Model Validation

Simulation results are presented to validate the models derived previously. The obtained models were compared with PSIM simulations of the FBF current rectifier using the parameters shown in Table I. For both operating modes the converter was simulated with a dc input voltage source (dc–dc mode) until the steady-state condition was reached, when d was slightly perturbed around the quiescent operating point. As a response to this small-signal disturbance around the quiescent operating point, the current waveforms vary according the converter dynamics.

Simulation for step-up mode had been carried out for $V_{in} = U = 220 \text{ V}$, $V_o = 400 \text{ V}$, $R_o = 53.3 \text{ } \Omega$, $D = 0.645$, and $\Delta D = 0.001$. Fig. 6 shows the comparison between the simulation results and averaged waveforms obtained from analytical models. On the other hand, Fig. 7 presents a comparison for this converter in step-down mode, where $V_{in} = U = 300 \text{ V}$, $V_o = 200 \text{ V}$, $R_o = 20 \text{ } \Omega$, $D = 0.33$, and $\Delta D = 0.001$. As

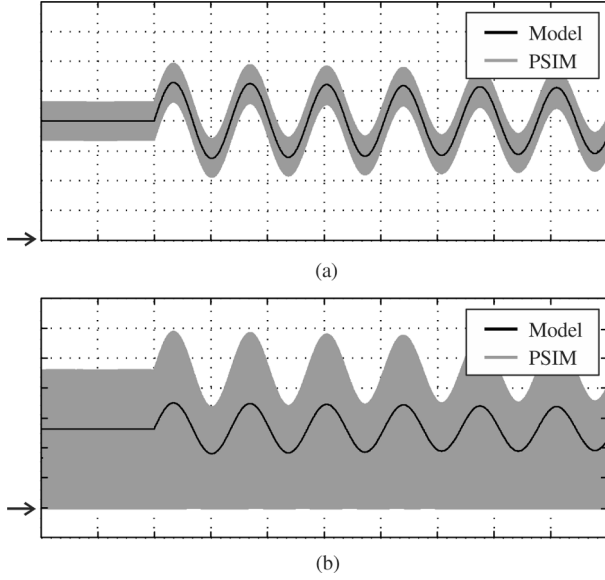


Fig. 7. Comparison between small-signal averaged model of the FCB current rectifier in step-down mode and PSIM simulation (2.5 A/div, 2.5 ms/div). (a) Magnetizing current i_{Lc} . (b) Input current i_{Lpf} .

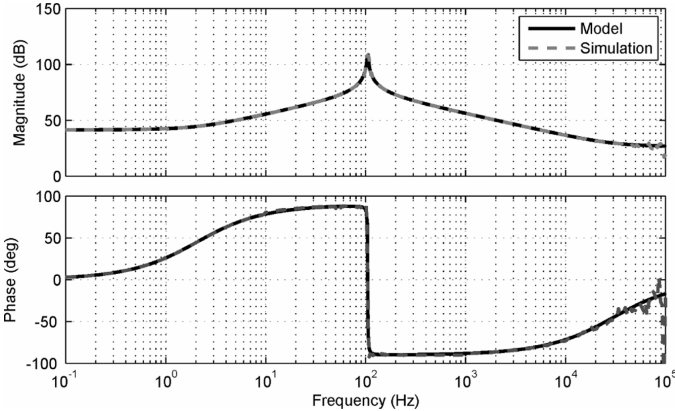


Fig. 8. Step-up mode: frequency response of the duty ratio to input current transfer function (24) and frequency response obtained from ac sweep simulation in PSIM.

can be seen in these results, the duty ratio perturbation results in highly oscillatory current waveforms around the respective dc operating points, due to the low damping factor of the converter in both operation modes. In both cases, the current waveforms obtained from models are equal to the average values of the simulated current waveforms. Therefore, the obtained ac models describe suitably the dynamic behavior of the converter around a quiescent operating point.

In addition, Figs. 8 and 9 compare the frequency responses obtained from the duty ratio to input current transfer functions and the frequency responses obtained from ac sweep simulations in PSIM, for step-up and step-down modes, respectively. One can observe that these models strongly agree with the simulation results, mainly in the low-frequency range (dc up to approximately $f_s/5$ [34]), where the switching effects can be neglected.

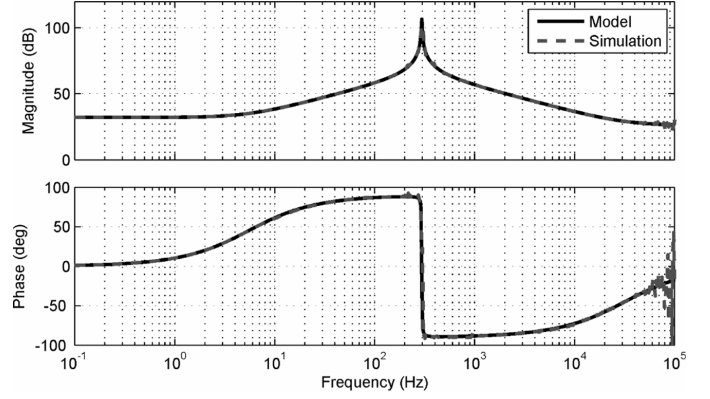


Fig. 9. Step-down mode: frequency response of the duty ratio to input current transfer function (37) and frequency response obtained from ac sweep simulation in PSIM.

IV. INPUT-CURRENT-TO-OUTPUT-VOLTAGE MODEL

Here, we present the input-current-to-output-voltage averaged model of the converter shown in Fig. 1, where the objective is to derive the transfer function from the averaged value of the rectified input current to output voltage, so that it is possible to design the outer voltage loop.

First, one can obtain the transfer function from the full-bridge converter current i_{fb} to the output voltage v_o as

$$\frac{v_o(s)}{i_{fb}(s)} = \frac{\frac{1}{C_o}}{s + \frac{1}{R_o C_o}}. \quad (39)$$

As the relation between the currents i_{fb} and the i_{Lpf} is nonlinear, one can obtain it from input-output energy balance

$$\int_0^{T_1} p_o(t) dt = \int_0^{T_1} p_{in}(t) dt. \quad (40)$$

Assuming unitary power factor and that the capacitor C_o is large enough to produce an output voltage with small ripple, one can rewrite (40) as

$$I_o V_o = I_{ac} V_{ac} \quad (41)$$

where I_{ac} and V_{ac} are the rms values of the input current and input voltage, respectively, and I_o and V_o are the dc values of the output current and output voltage, respectively.

In addition, the relation between the rms value of the input current and the average current in the inductor L_{pf} is

$$\overline{I_{Lpf}} = \frac{1}{\pi} \int_0^\pi \sqrt{2} I_{ac} \sin(\omega t) d\omega t = \frac{2\sqrt{2} I_{ac}}{\pi} \quad (42)$$

and, considering that $I_o = \overline{I_{fb}}$ and $m_a = \sqrt{2} V_{ac}/V_o$, the following relation can be obtained:

$$\overline{I_{fb}} = \frac{\pi m_a \overline{I_{Lpf}}}{4}. \quad (43)$$

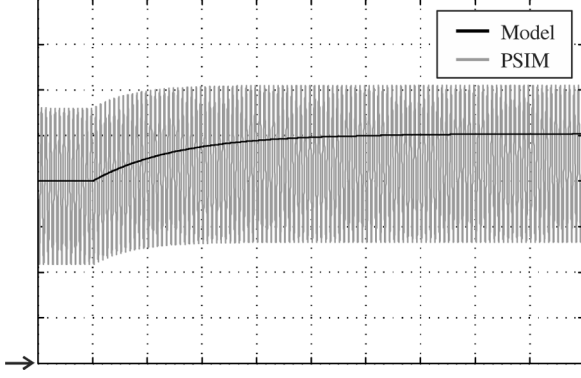


Fig. 10. Comparison between input current to output voltage averaged model of the FBF current rectifier and PSIM simulation (100 V/div, 100 ms/div).

Consequently, a low-frequency model around a quiescent operating point is derived replacing (43) in (39) as follows:

$$G_v(s) = \frac{\bar{v}_o(s)}{\bar{i}_{Lpf}(s)} = \frac{\pi m_a}{4} \frac{R_o}{R_o C_o s + 1}. \quad (44)$$

To validate the derived model, the converter had been simulated with parameters shown in Table I, using a sinusoidal input voltage source and an inner current control loop to track the reference current. Due to the pulsating instantaneous input power, the output voltage has an average value and an ac component at twice of the power supply frequency, which is not modeled in the derived low-frequency model. One can observe from Fig. 10 that the output of the averaged model adequately follows the average output voltage value of the simulated converter for small amplitude disturbances.

V. CONTROL DESIGN

This section presents a digital control design for the converter parameters given in Table I. In this design example, this converter is used in the input stage of a double-conversion UPS, whose dc bus voltage is always higher than the input voltage. As a result, the converter only operates in step-up mode.

The digital control system has been implemented in the DSP TMS320F2812. Therefore, the design methodology of the current and voltage controllers considers the main features of this DSP [35]. The crossover frequency of the current loop gain f_c was chosen as 5 kHz to achieve a good dynamic performance and the crossover frequency of the voltage loop gain was chosen as 12 Hz to synthesize low-THD input currents. Consequently, the input current has a dynamic behavior much faster than the output voltage and the control loops are dynamically decoupled [32].

A. Current Loop

A block diagram of the digital system used to control the input current is presented in Fig. 11(a), where $C_i(z)$ is a digital proportional-integral (PI) controller with a low-pass filter.

Since the input current waveform has a discontinuous characteristic, a first-order low-pass filter was included in the feedback path to obtain the average value of the current i_{Lpf} , so that

$$H_i(s) = h_i H_{lpf}(s) = h_i \frac{1}{s + 1} \frac{1}{\frac{R_{lp} C_{lp}}{1}} \quad (45)$$

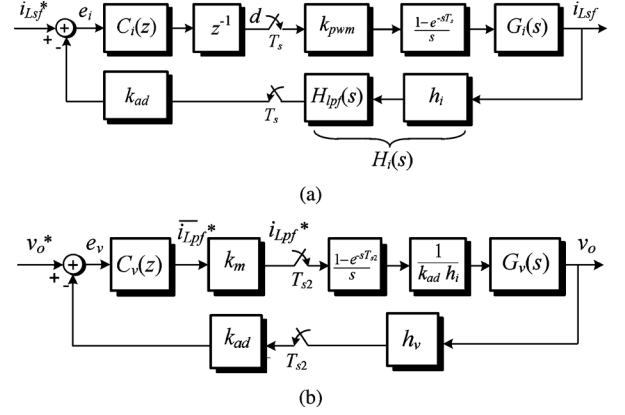


Fig. 11. Detailed digital control structure. (a) Current loop. (b) Voltage loop.

TABLE II
CONTROLLER SYSTEM PARAMETERS

$f_{s1} = 200 \text{ kHz}$	Sampling frequency - current loop
$f_{s2} = 10 \text{ kHz}$	Sampling frequency - voltage loop
$R_{lp} = 1 \text{ k}\Omega$	Resistance of low-pass filter
$C_{lp} = 10 \text{ nF}$	Capacitance of low-pass filter
$h_i = 0.1$	Current sensor gain
$h_{vo} = 0.005$	Output voltage sensor gain
$h_{vin} = 0.0042$	Input voltage sensor gain
$k_{ad} = 2^{12/3}$	A/D converter gain
$k_{pwm} = 1/750$	PWM gain

where h_i is the current sensor gain. The parameters of this filter are shown in Table II.

Assuming that the sampling frequency is much higher than the loop frequency bandwidth ($f_c < 0.1 f_{s1}$), the frequency response of centered pulse-width modulator (PWM) can be approximated by a zero-order hold (ZOH) [37]. Therefore, the discrete-time transfer function of $G_i H_i(s)$ is given by

$$G_i H_i(Z) \left\{ \left(\frac{1 - e^{-sT_s}}{s} \right) G_i(s) H_i(s) \right\}. \quad (46)$$

Moreover, the unit delay to update the control action can be included to design the inner current loop, so that

$$G_i H'_i(z) = z^{-1} G_i H_i(z). \quad (47)$$

The design of the digital PI controller was based on the frequency response method using the w-plane methodology [36]. Consequently, it is necessary to obtain the loop transfer function $T_i(w)$ in the w-domain. For the system shown in Fig. 11(a), this transfer function is given by

$$T_i(w) = k_{pwm} k_{ad} C_i(w) G_i H'_i(w) \quad (48)$$

where k_{pwm} is the PWM gain and k_{ad} is the ADC gain.

From (20) and (23)–(25), one can verify that the duty ratio to input current transfer function $G_i(s)$ depends on the duty ratio. Therefore, the transfer function $G_i H_i(w)$ also depends on the operating point. This is particularly important for PFC converters, because the input voltage is variable. Fig. 12 shows the

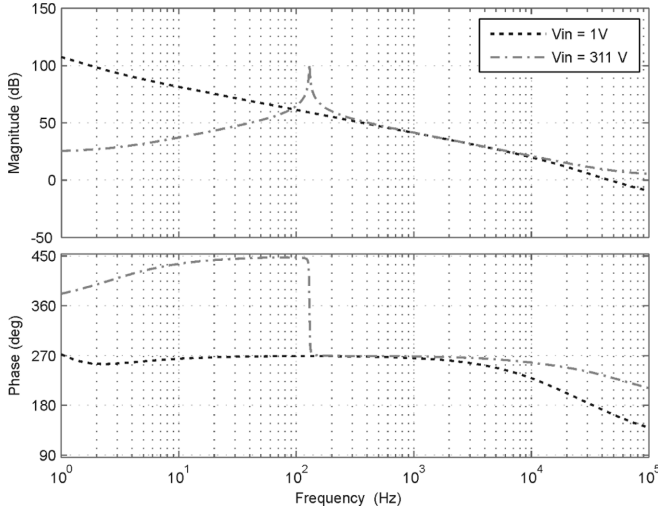


Fig. 12. Frequency response of $G_i H_i(w)$ for distinct operating voltages.

frequency response of $G_i H_i(w)$ for two distinct input voltage levels: $V_{in} = 1$ V and $V_{in} = 311$ V (peak value). One can observe that this transfer function presents larger phase-shift and smaller magnitude at high frequencies when $V_{in} = 1$ V. Consequently, the current compensator was designed for this operating point ($V_{in} = 1$ V) to ensure minimum values of phase margin and crossover frequency at all operating points.

It is worth mentioning that most converters are stable when is ensured the closed-loop stability based in small-signal models at all operating points. This analysis is presented in Section VI.

The specifications imposed to the digital control system are a minimum phase margin equal to 45° and a minimum crossover frequency equal to 5 kHz. As a result, the transfer function of the current controller is

$$C_i(w) = 14200 \frac{w + 3142}{w(w + 314200)}. \quad (49)$$

The discrete-time current controller is derived from w-plane to z-plane transform [36] as

$$C_i(z) = \frac{0.02z^2 + 0.0003124z - 0.01973}{z^2 - 1.12z + 0.1201}. \quad (50)$$

Fig. 13 presents the frequency response of the loop transfer function $T_i(w)$ with the compensator shown in (49), presenting a gain crossover frequency equal to 5 kHz and a phase margin around 48° .

B. Voltage Loop

A block diagram of the digital control system used to regulate the output voltage is shown in Fig. 11(b), where $C_v(z)$ is a digital PI controller. This low-bandwidth voltage loop regulates the dc output voltage under input voltage and load disturbances, similarly to a conventional boost PFC converter without an input voltage feedforward action.

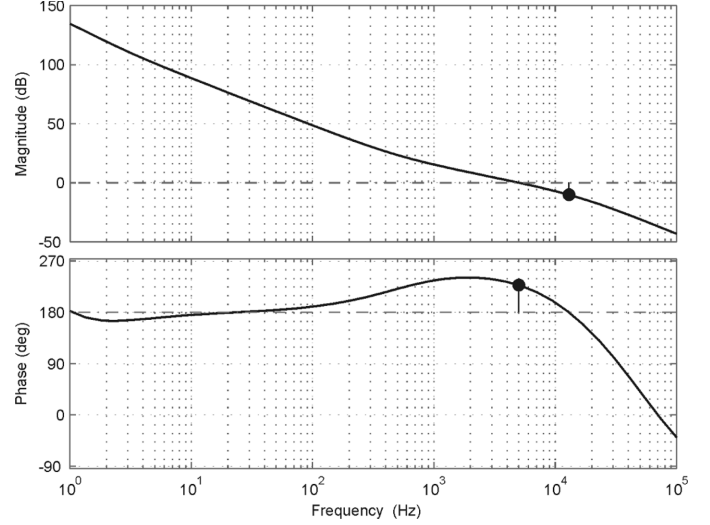


Fig. 13. Compensated current loop frequency response.

It is assumed that the input current is constant over a switching period to derive the discrete-time transfer function of $G_v(s)$, then

$$G_v(z) = Z \left\{ \left(\frac{1 - e^{-sT_s}}{s} \right) G_v(s) \right\}. \quad (51)$$

For the system presented in Fig. 11(b), the w-domain loop transfer function $T_v(w)$, utilized to design the voltage controller, is given by

$$T_v(w) = k_m k_{ad} h_v \frac{1}{k_{ad} h_i} C_v(w) G_v(w) \quad (52)$$

where h_v is the voltage sensor gain, $1/(k_{ad} h_i)$ is the low-frequency gain of the current loop, and k_m is the equivalent multiplier gain, given by

$$k_m = h_{vin} k_{ad} \overline{V_{in}} \quad (53)$$

where $\overline{V_{in}} = 2V_{in \max}/\pi$.

The specifications imposed to the outer voltage loop are a phase margin around 60° and a crossover frequency around 12 Hz. As a result, the transfer function of the PI voltage controller is

$$C_v(w) = 0.53 \frac{w + 50.27}{w}. \quad (54)$$

Then, the discrete-time voltage controller can be computed by using the w-plane to z-plane transform as

$$C_v(z) = \frac{0.005313z - 0.005287}{z - 1}. \quad (55)$$

As can be observed from Fig. 14, the resulting phase margin of $T_v(w)$ is around 60° and the crossover frequency is 12 Hz.

VI. STABILITY ANALYSIS

The stability analysis of the inner current loop, whose design is presented in Section V, is not straightforward due to the nonlinear behavior of the FBF isolated current rectifier. The models

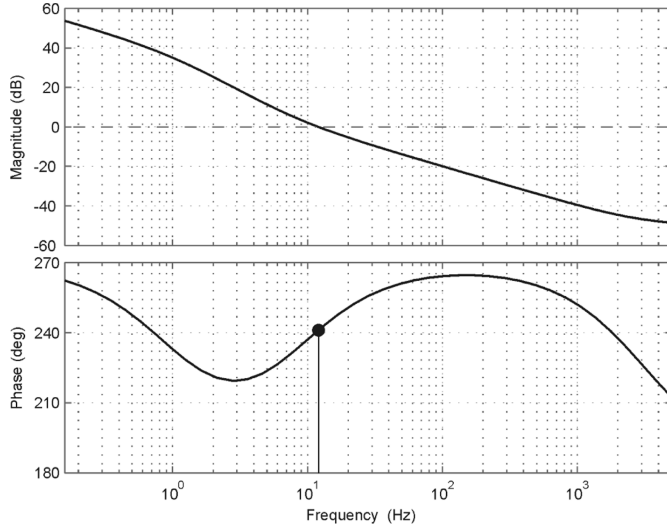
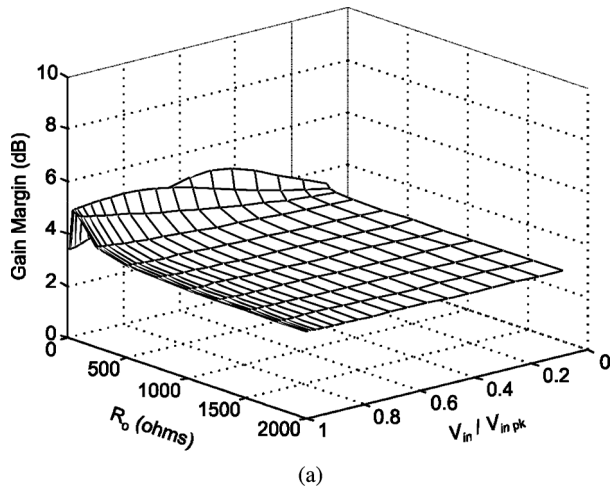
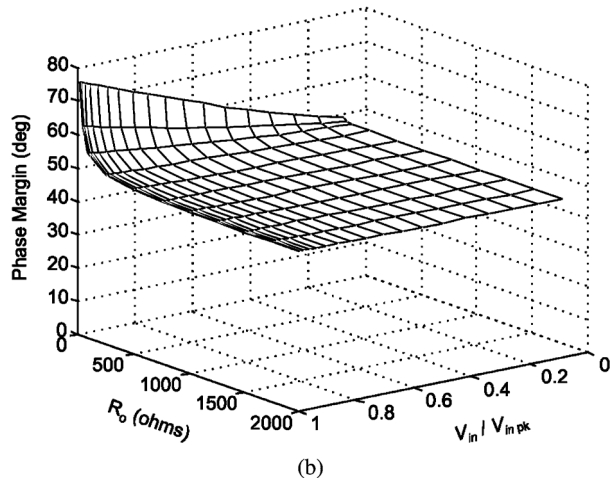


Fig. 14. Compensated voltage loop frequency response.



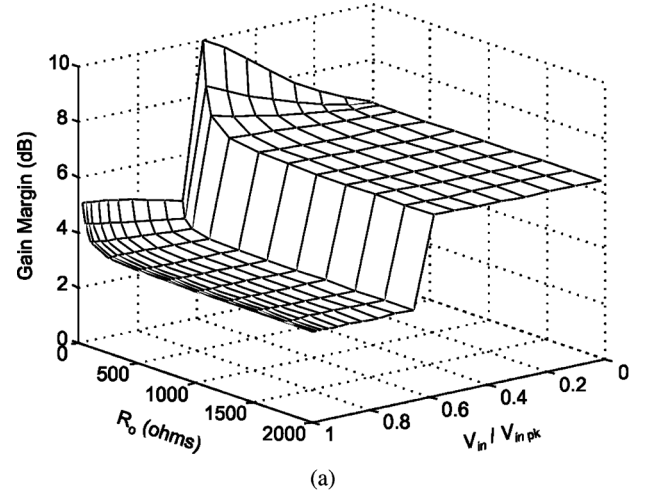
(a)



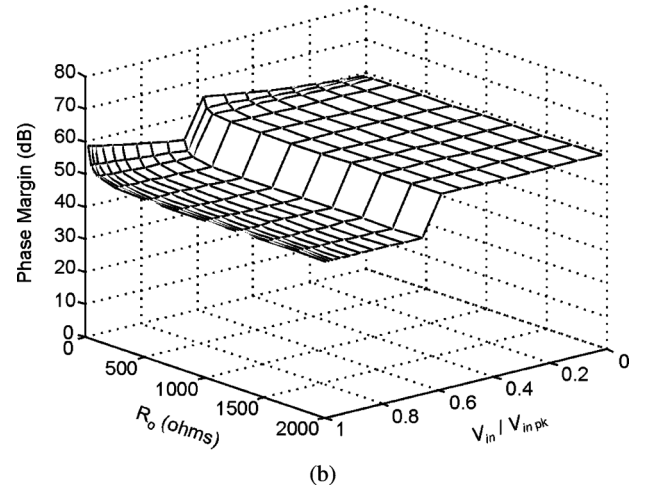
(b)

Fig. 15. Stability analysis of the inner current loop in step-up mode ($V_o = 400$ V) varying V_{in} and R_o . (a) Gain margin. (b) Phase margin.

derived in Section III were derived assuming the dc-dc operation for a single operation point. However, the operation point is continuously changing due to ac-dc operation and converter can operate in two distinct modes.



(a)



(b)

Fig. 16. Stability analysis of current loop in mixed step-up and step-down modes ($V_o = 200$ V) varying V_{in} and R_o . (a) Gain margin. (b) Phase margin.

On the other hand, the proposed control approach uses a single linear current controller for both operation modes. Therefore, the stability is analyzed considering the impact of parametrical variations in the closed-loop system. Figs. 15 and 16 show gain margin (GM) and phase margin (PM) of the inner current loop for two operation points (distinct output voltages) in step-up mode and mixed step-up and step-down modes, respectively. These curves were plotted for the full range of instantaneous values of the input voltage V_{in} and load (R_o).

Fig. 15 shows that GM and PM have small changes in their values when the converter operates only in step-up mode. On the other hand, one can observe in Fig. 16 an abrupt change in these curves when the converter operates in mixed modes. This sudden change is related to the transition between step-up and step-down modes, which have differences in their dynamic models. However, due to smooth gain transition between modes, there is no oscillation after these mode transitions.

In addition, Fig. 17 presents the minimum values of GM and PM for different values of V_o , considering all values of V_{in} and R_o analyzed in Figs. 15 and 16. The minimum value for GM is 2 dB and for PM is 30°. One can conclude that although this control loop had been designed for operation only in step-up mode, with $V_o = 400$ V, it remains stable in all operation points, including the operation in step-down mode.

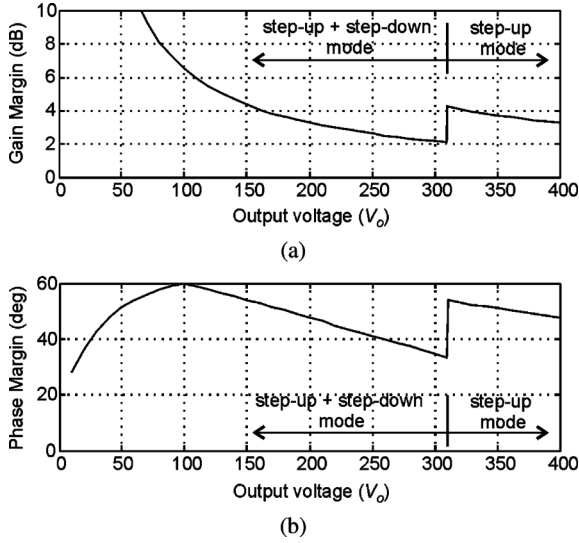


Fig. 17. Minimum stability margins varying V_{in} , R_o and V_o . (a) Gain margin. (b) Phase margin.

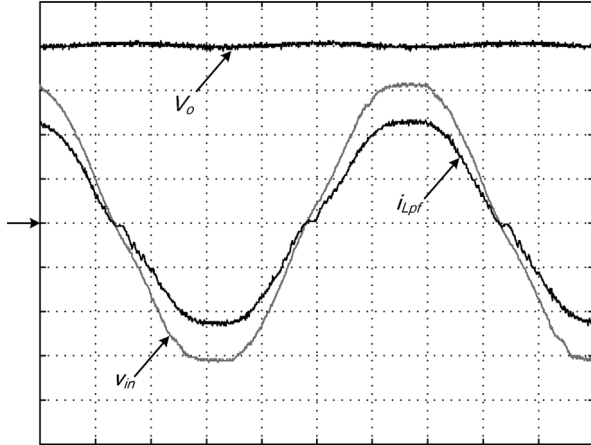


Fig. 18. Experimental results in step-up mode: input current, input and output voltage waveforms (100 V/div, 10 A/div, 2.4 ms/div).

VII. EXPERIMENTAL RESULTS

A prototype of the closed-loop converter shown in Fig. 1 was built in our laboratory to verify the performance of the digital control system under distinct practical conditions. The digital controllers were implemented on DSP TMS320F2812 from Texas Instruments. The main parameters of the prototype and control system are presented in Tables I and II, respectively.

Fig. 18 shows the input current and input and output voltage waveforms with nominal resistive load and nominal input and output (400 V) voltages. At this operating point, the converter operates only in step-up mode, the total harmonic distortion (THD) of the input current waveform is 5.6% and the input power factor is 0.99. Moreover, Fig. 19 presents the input current and the output voltage waveforms during a sudden load change from half-load to nominal load.

On the other hand, to evaluate the performance of the closed-loop system in step-down mode, Fig. 20 presents the input current, the input and output voltages with a resistive load equal to 20 Ω , nominal input voltage and output voltage equal to 200 V. At this operating point, the converter operated in a mixed

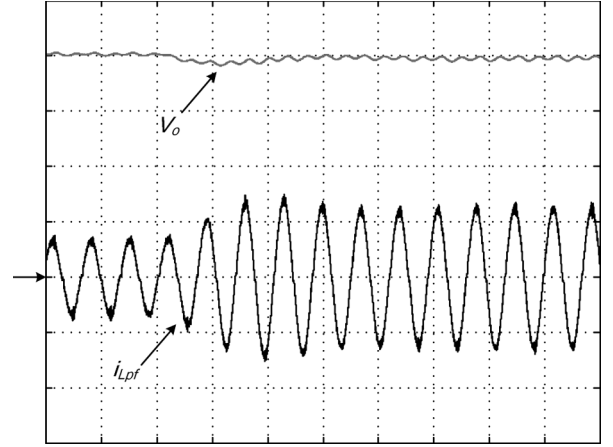


Fig. 19. Experimental results in step-up mode: input current and output voltage waveforms during a sudden load change (50%–100%) (100 V/div, 20 A/div, 24 ms/div).

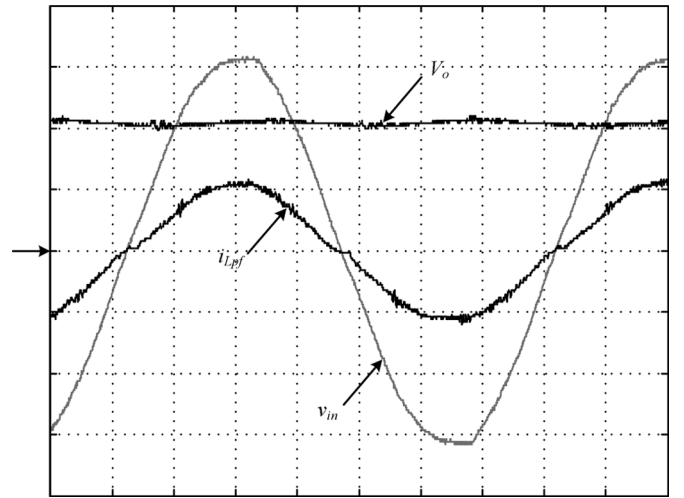


Fig. 20. Experimental results in mixed step-up and step-down modes: input current, input and output voltage waveforms (100 V/div, 10 A/div, 2.4 ms/div).

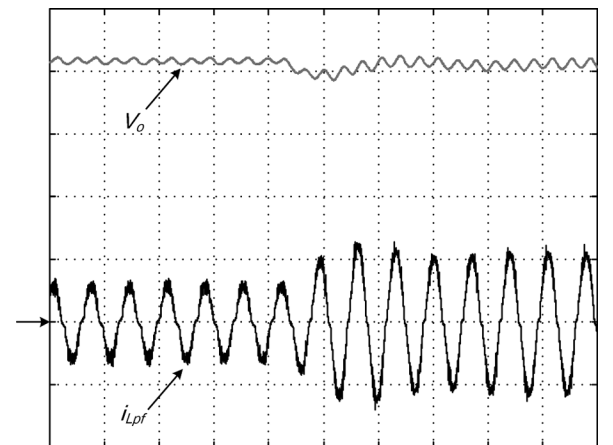


Fig. 21. Experimental results mixed step-up and step-down modes: input current and output voltage waveforms during a sudden load change (50%–100%) (50 V/div, 10 A/div, 24 ms/div).

step-up and step-down modes. Even using the same digital control system, which was designed to operate in step-up mode,

the input current waveform has low THD (6.3%) and high input power factor (0.99). Finally, Fig. 21 shows the dynamic performance of the closed-loop converter operating in mixed step-up and step-down modes during a sudden load change from half-load to nominal load.

VIII. CONCLUSION

This paper presented a detailed modeling of an FBF isolated rectifier, using the state-space averaging method. Distinct duty ratio-to-input current models were obtained for each operation mode, which present distinct dynamic behavior. It was verified that by designing the current control loop from the model achieved in the step-up mode, the controller performs well even in step-down mode. The input current-to-output voltage model was also obtained and it is the same for both operation modes.

Digital controllers were designed from frequency response methods. Experimental results show that the closed-loop system has a good steady-state and transient performances, even with sudden load changes.

APPENDIX I

The model of the circuit shown in Fig. 4(b) is given by

$$\begin{cases} -v_{in}(t) + v_{Lpf}(t) + v_{Lp}(t) = 0 \\ -v_{Ls}(t) + v_{Lsf}(t) + v_o(t) = 0 \end{cases} \quad (56)$$

The circuit description of the magnetic coupled inductor is given as follows:

$$\begin{cases} v_{Lpf}(t) = (r_L + \rho L_{pf}) i_{Lpf}(t) + \rho L_c i_{Lsf}(t) \\ v_{Lsf}(t) = \rho L_c i_{Lpf}(t) + (r_L + \rho L_{sf}) i_{Lsf}(t) \end{cases} \quad (57)$$

where ρ is the derivate operator (d/dt) and L_c is the mutual inductance. Assuming the unitary primary/secondary winding ratio and unitary coupling coefficient, we obtain

$$L_c = L_{pf} = L_{sf}. \quad (58)$$

Moreover, assuming an unitary primary/secondary turn ratio in the transformer T_1 , we obtain

$$v_{Lp}(t) = v_{Ls}(t). \quad (59)$$

Applying (57)–(59) to (56) derives the state-space model given in (11).

APPENDIX II

Assuming the sinusoidal input current and the unitary power factor operation, we obtain from the energy balance analysis that

$$i_{in}(\omega t) = \frac{2V_o^2}{R_o V_{in\ pk}} |\sin(\omega t)|. \quad (60)$$

Rewriting (1) assuming that the input voltage is given by $v_{in}(\omega t) = V_{in\ pk} |\sin(\omega t)|$, we have

$$|\sin(\omega t)| = \frac{V_o}{V_{in\ pk}} \frac{1 - d(\omega t)}{d(\omega t)}. \quad (61)$$

Substituting (61) into (60) and given that

$$i_{Lc}(\omega t) = \frac{i_{in}(\omega t)}{d(\omega t)} \quad (62)$$

results in (23).

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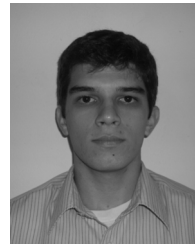
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