

# A Small Signal Model for Controlling the DC Bus Voltage of a Series Active Power Filter

Guilherme da Silva Fischer, Alisson Mengatto and Marcello Mezaroba

Santa Catarina State University - UDESC

Electric Power Processing Group - nPEE

89.219-710, Joinville - SC, Brazil

guilherme.silva.fischer@gmail.com, alisson\_mengatto@hotmail.com, marcello.mezaroba@udesc.br

**Abstract**—This paper presents the modeling and DC-bus voltage control strategy for a voltage controlled series active power filter (APF) 3-phase 4-wire voltage source converter (VSC) that uses feedback from the load-side bus. The VSC is connected through a coupling transformer and has no auxiliary converter for controlling the DC-bus voltage. The simplified control strategy and required small signal models for controller design are presented and validated by simulating a 45 kVA load supplied by distorted and unbalanced voltages.

## I. INTRODUCTION

The continuous increase of non-linear loads connected to the power grid encourages the developments of power quality correction techniques. The harmonic currents of non-linear loads cause voltage drops on the source impedance that distort the voltage waveform applied to the load. The series active power filter (APF) [1] ensures that the Load-bus voltage is sinusoidal and with low distortion even when supplying non-linear loads or when the grid voltage is distorted, by injecting harmonic voltage components with opposite phase in series with the supply voltage. Furthermore, the series APF is a voltage controlled converter that utilizes a coupling transformer connected in series between the Load-bus and the PCC-bus to compensate distorted or unbalanced voltages. Fig. 1 illustrates the conventional structure of a three-phase series APF.

The distribution of electric power in 3-phase low voltage power systems is usually implemented using 4-wire connections. Typical loads connected to three-phase four-wire power system are adjustable speed drives, electric furnaces, lighting ballasts, office equipment and other power electronics related facilities. These loads may be either single-phase or three-phase and have non-linear input current with high harmonic content, which causes voltage distortion. Assuming an imbalance in load or source voltage, three degrees of freedom are necessary to compensate the phase voltages independently.

The three degrees of freedom requirement can be accomplished on a typical three leg VSC by splitting the DC-bus capacitor and connecting the central point to the neutral. This configuration presents challenges in the converter control when the DC-bus voltage is not supplied through an independent dc power source, i.e., the series APF is controlled as to supply the losses in the pulse width modulated (PWM) converter directly

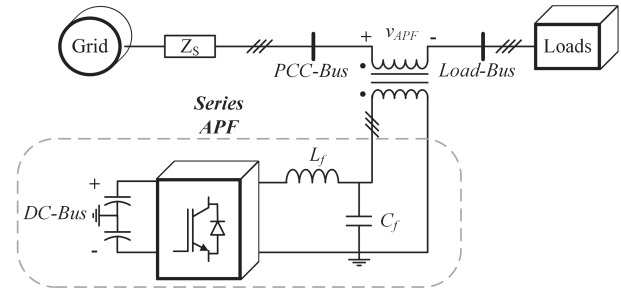


Fig. 1. Series APF structure.

from the ac source. Few papers present this approach in the literature for 3-phase 4-wire series APF, where solutions are proposed for single phase converters [2], 3-wired converters [3] or using three single-phase full-bridge converters each coupled through a single phase transformer [4].

The conventional control strategy to compensate the Load-bus voltage distortion is to extract its fundamental and harmonic components to generate counter harmonics as references for the series APF output voltage, resulting in a pure sinusoidal voltage at the Load-bus [2], [5], [6]. High-order filters are necessary to separate the fundamental voltage online, which increases computational efforts and complexity, and the digital implementation adds an extra time delay which will deteriorate the compensation performance [7]. In transformerless applications [5] the performance of the series APF when controlling the converter output voltage is higher because there is no leakage or magnetizing inductance, or winding resistance, but in systems where coupling transformers are used there is no guarantee that output voltage of the converter will be correctly reflected to the secondary side of transformer, with the exact transformation ratio required, especially at the higher order harmonics, leading to over or under compensation of the voltage harmonics.

Schemes to control the DC-bus voltage using the load itself in applications with rectifiers [8] or using a separate low power diode bridge rectifier that needs only to process active power for converter losses [9] are found in the literature, however, added costs and voltage level control restrictions (e.g. necessity to choose appropriate turns ratio of the coupling transformer) are a drawback of this solutions. Several different

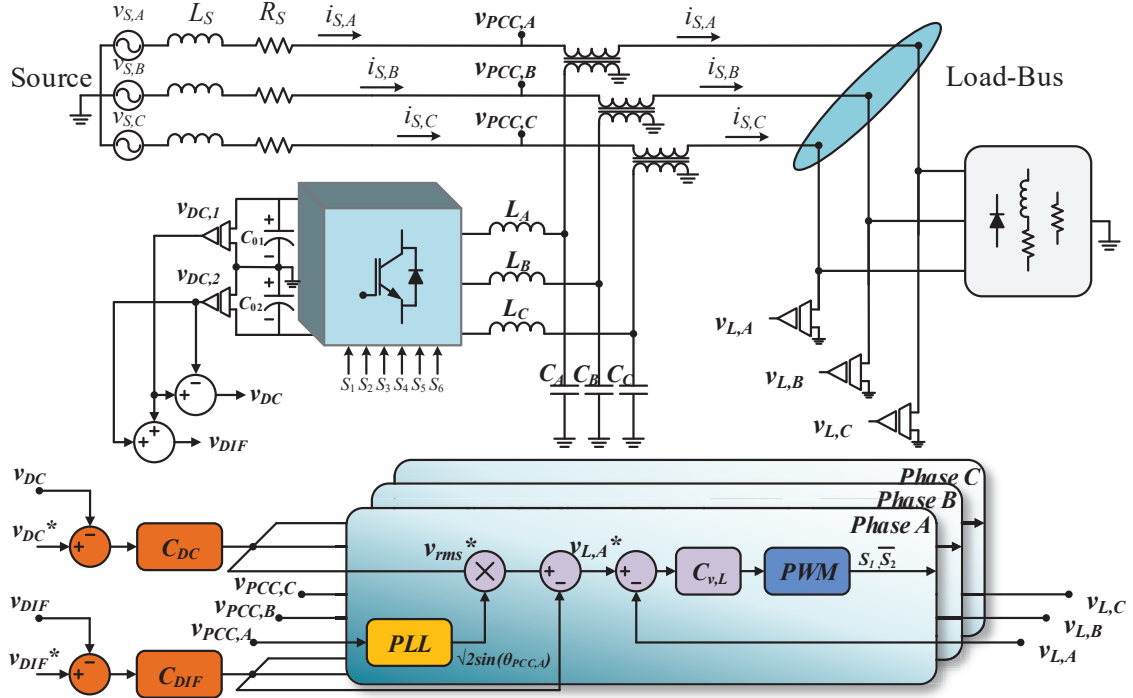


Fig. 2. General diagram of the series APF.

DC-bus voltage control schemes exist in power conditioners. In universal power quality conditioners (UPQC) [10] [11] the DC-bus voltage is controlled by the shunt APF. Using the "pq" theory [12], a directly absorbed real power control can be applied [4] utilizing no other power electronics equipment or dc sources.

In [2] the control strategy for the DC-bus voltage using a series APF is established as a voltage drop in the fundamental frequency in phase with the source voltage, and its model was proposed by average instantaneous values at the switching frequency. Another possibility is to create a voltage drop synchronized with the load current in the fundamental frequency so that the series APF is seen as a resistor in series with the load. It is also possible to control the DC-bus voltage while injecting reactive power at the fundamental frequency, regulating the load voltage within limits that are imposed by the load power factor, similarly to dynamic voltage restorers (DVRs) [13]. The solution in [2] is also used in this paper for its simplicity, but a different model is proposed since the feedback voltage is located at the load side, and the effect of the load current is considered in the model.

This paper is focused on the modeling and control strategy for the DC-bus voltage of a series APF that uses voltage feedback directly from the terminal load. The equivalent models are presented and validated by simulation. The simulated system is based on a commonly found situation of unbalanced and distorted supply voltages in a 45 kVA system. The proposed control strategy is capable of providing balanced sinusoidal voltages with low harmonic distortion to the loads when linear and non-linear loads are connected.

## II. CONTROL STRATEGY

The power circuit of the proposed series APF is made up of a four-wire three-phase converter and its output filter. Three single-phase transformers are used to connect the series APF between the utility grid and the terminal load as shown in Fig. 2. The control structure has one internal loop per phase for controlling the load voltage independently, and two external loops for DC-bus voltage control and assurance of balanced voltages in the capacitors. A block diagram representation including the linear models is shown in Fig. 3.

In the proposed control scheme, the power calculation and harmonic extraction are not needed since the harmonics, voltage unbalances and other disturbances are compensated by the load voltage controller, which has a reference that is purely sinusoidal.

The load voltage reference,  $v_L^*$ , is a result of the DC-bus voltage control loop and the phase locked loop (PLL). The PLL used was the same as in [14] and has a robust response in the presence of harmonic and noise.  $C_{DC}$  and  $C_{DIF}$  are the DC-bus controllers for the total and differential DC-bus voltages, respectively. The  $C_{DIF}$  loop will not be described in details in this paper since the DC-bus voltage modeling and control are the focus. Controller  $C_{DC}$  tracks the DC-bus voltage reference  $v_{DC}^*$ , by setting the rms amplitude reference of the Load-Bus voltage,  $v_{rms}^*$ , as reducing the load voltage increases the voltage drop (and absorbed power) in the series APF. The desired load voltage amplitude is multiplied by a sine wave in phase with the PCC-bus voltage, which is synchronized by independent PLLs for each phase.

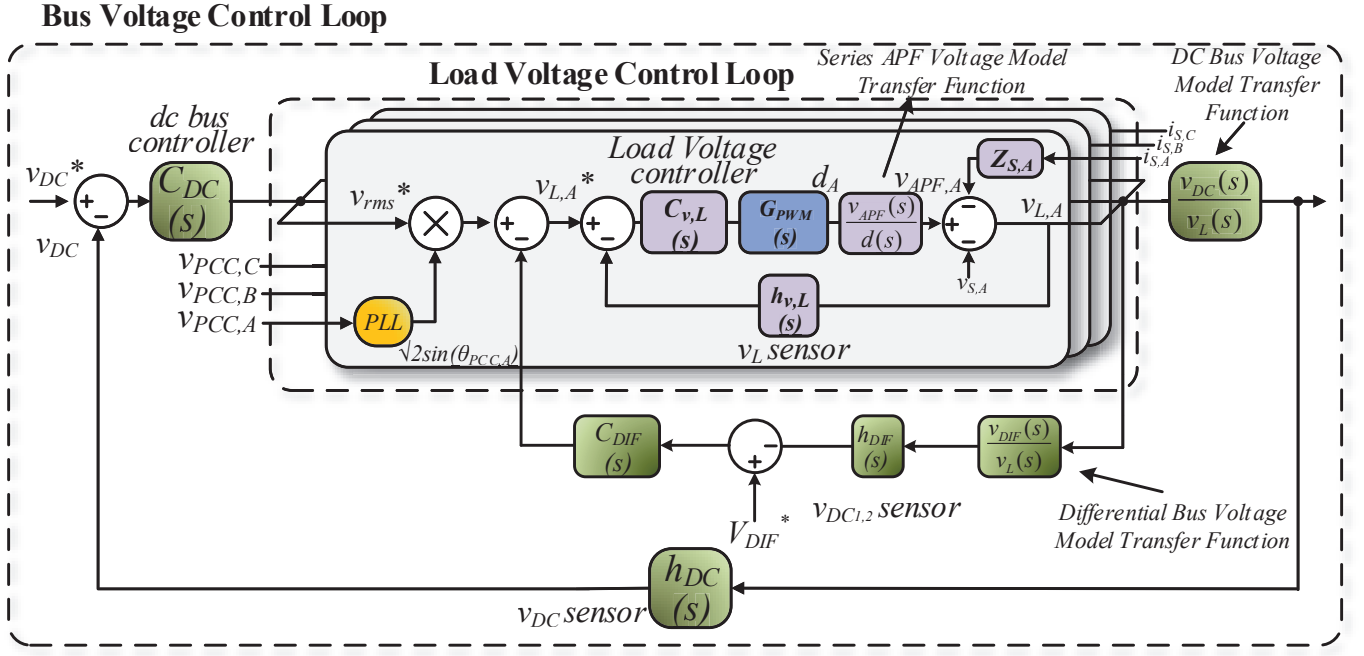


Fig. 3. Block diagram of the series APF control strategy including the representation of linear models.

Each Load-bus voltage loop must synthesize the output converter voltages  $v_{APF,A}$ ,  $v_{APF,B}$ ,  $v_{APF,C}$  to provide sinusoidal and balanced three phase voltages for the load. Therefore, the Load-bus voltage controllers  $C_{v,L}$  determine the converter duty cycle based on the Load-bus voltage feedback, without measuring the PCC-bus voltage to extract the harmonic components. In this technique, harmonic components present in the source voltage and harmonic components created by the voltage drop in the source impedance are seen as disturbances in the system output, as seen in Fig 3. In order to compensate the high order voltage harmonic components which are considered disturbances, the dynamic response of the Load-bus voltage controllers should be fast. This requirement is met designing high bandwidth controllers, which results in a voltage with low harmonic content provided to the load.

The model for controlling the Load-bus voltage in each phase as a function of the duty cycle signal was deduced in [15], but a shunt APF was used to control the DC-bus voltage. Therefore the main contribution of this work is the modeling of the DC-bus voltage in the series APF as a function of the Load-bus voltage amplitude, allowing a control strategy for the series APF that does not require any auxiliary converter for DC-bus voltage control while using a simpler strategy for compensating the PCC-bus harmonics.

A low bandwidth external loop is used for the DC-bus voltage control so that the sine reference is not distorted by high-frequency oscillations, and its output is the rms voltage reference for the three load-bus voltage controllers. The differential controller has even lower bandwidth and subtracts a dc component at the reference for the three phase voltages, achieving voltage balance in the DC-bus capacitors.

A proportional-integral controller is used in for  $C_{DIF}$ .

### III. MODEL FOR DC-BUS CONTROLLER DESIGN

A small signal model is necessary for designing the controller for the proposed DC-bus voltage control strategy. As presented in the introduction, [2] uses a voltage drop at the fundamental line frequency in the series APF for absorbing active power, and models the DC-bus voltage dynamics as a function of this voltage drop, but at the switching frequency. Since the model was developed at the switching frequency, low-frequency effects such as the source voltage and the load current are not present in their model. These effects are considered in the model presented in this paper and are not negligible. Furthermore, in this work the proposed control strategy uses feedback from the Load-bus for compensating the distorted voltage, therefore the voltage drop in the series APF can not be directly controlled as in [2]. This difference also requires a different model for designing the DC-bus voltage controller.

The DC-bus voltage controller has low bandwidth (significantly lower than grid frequency) and the active power transfer in the system occurs at the fundamental frequency, therefore the modeling process can start by considering that the power flow can be calculated through phasor analysis at the fundamental line frequency.

From the equivalent circuit in Fig. 4 the active power flow into the series APF,  $p_{APF}$ , is given by (1), and the voltage drop in the series APF is given by (2) as the difference between the PCC-bus voltage and the Load-bus voltage.

$$p_{APF} = \text{Re}(\overline{i_s^*} \overline{v_{APF}}) \quad (1)$$

$$\overline{v_{APF}} = \overline{v_{PCC}} - \overline{v_L} \quad (2)$$

The PCC-bus voltage can be found from the source voltage and the voltage drop at the source impedance  $\overline{Z_S} = R_S + jX_S$  (3).

$$\overline{v_{PCC}} = \overline{v_S} - \overline{Z_S} \overline{i_S} \quad (3)$$

Since the APF is series connected, load current and source current are the same and given by (4).  $\overline{Z_L} = R_L + jX_L$  is the equivalent load impedance.

$$\overline{i_S} = \overline{i_L} = \frac{\overline{v_L}}{\overline{Z_L}} \quad (4)$$

Equations (1), (2), (3), and (4) can be combined into (5) and (6).

$$\overline{v_{PCC}} = \overline{v_S} - \frac{\overline{Z_S}}{\overline{Z_L}} \overline{v_L} \quad (5)$$

$$p_{APF} = \text{Re} \left( \frac{\overline{v_L}^*}{\overline{Z_L}^*} \left( \overline{v_S} - \frac{\overline{Z_S}}{\overline{Z_L}} \overline{v_L} - \overline{v_L} \right) \right) \quad (6)$$

To progress from 6 the real part must be taken, but the phase angle of both  $\overline{v_L}$  and  $\overline{v_S}$  are not yet known. To continue first  $\overline{v_{PCC}}$  is set as the phase reference, such that  $\angle \overline{v_{PCC}} = 0$  deg and thus  $\overline{v_{PCC}} = v_{PCC}$  (i.e., there is only a real component). The chosen control strategy creates a voltage drop in the series APF in phase with the PCC-bus voltage, such that  $\angle \overline{v_{PCC}} = \angle \overline{v_L} = 0$  deg, and again  $\overline{v_L} = v_L$ .

Since  $\overline{v_{PCC}}$  has only a real part, its imaginary part in (5) is 0, which gives (7).

$$\text{Im}(v_{PCC}) = \text{Im} \left( \overline{v_S} - \frac{\overline{Z_S}}{\overline{Z_L}} v_L \right) = 0 \quad (7)$$

The source voltage is separated into its real and imaginary parts in (8).

$$\overline{v_S} = a_S + jb_S \quad (8)$$

Equations (7) and (8) can be combined and manipulated into (9), where  $Z_L = |\overline{Z_L}|$ .

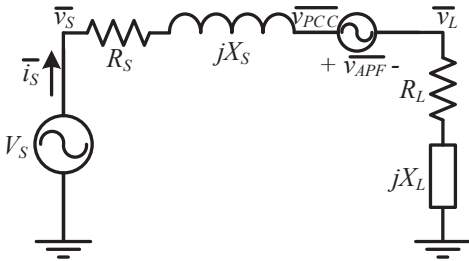


Fig. 4. The equivalent circuit at the fundamental line frequency of the system. The load reactive component  $X_L$  can be either inductive or capacitive.

$$b_S = \frac{R_L X_S - R_S X_L}{Z_L^2} v_L \quad (9)$$

The amplitude of the voltage source is constant and a system parameter, and related to its real and imaginary parts by (10). Combining (9) and (10) yields (11).

$$V_S^2 = a_S^2 + b_S^2 \quad (10)$$

$$a_S = \sqrt{V_S^2 - \left( \frac{R_L X_S - R_S X_L}{Z_L^2} v_L \right)^2} \quad (11)$$

Equations (11), (9), and (6) are combined into (12), which is a non-linear equation that relates the load voltage amplitude with the active power absorbed by one phase of the series APF.

$$p_{APF} = \frac{v_L}{Z_L^2} \left[ \sqrt{V_S^2 - \left( \frac{R_L X_S - R_S X_L}{Z_L^2} v_L \right)^2} R_L - v_L \left( \frac{R_L X_S - R_S X_L}{Z_L^2} X_L + R_S + R_L \right) \right] \quad (12)$$

To linearize (12) a first order Taylor Series approximation is used. The constant term  $P_{APF}$  is shown in (13), and the first order, small signal term  $\hat{p}_{APF}$  in (14).

$$P_{APF} = \frac{V_L}{Z_L^2} \left[ V_L \left( \sqrt{V_S^2 - \left( \frac{R_L X_S - R_S X_L}{Z_L^2} V_L \right)^2} R_L - \left( \frac{R_L X_S - R_S X_L}{Z_L^2} X_L + R_S + R_L \right) V_L \right) \right] \quad (13)$$

$$\hat{p}_{APF} = \frac{1}{Z_L^2} \left[ \frac{R_L \left( V_S^2 - 2 \left( \frac{R_L X_S - R_S X_L}{Z_L^2} V_L \right)^2 \right)}{\sqrt{V_S^2 - \left( \frac{R_L X_S - R_S X_L}{Z_L^2} V_L \right)^2}} - 2 \left( \frac{R_L X_S - R_S X_L}{Z_L^2} X_L + R_S + R_L \right) V_L \right] \hat{v}_L \quad (14)$$

The active power absorbed by each phase of the series APF flows into the DC-bus capacitor, which results in (15), where  $C_O$  is the equivalent DC-bus capacitor (i.e. series equivalent of the split capacitors). Linearization is now done by substituting  $v_{DC} = V_{DC} + \hat{v}_{DC}$  and  $p_{APF} = P_{APF} + \hat{p}_{APF}$  (the DC operating point and a small signal disturbance), yielding (16).

$$\frac{1}{2} C_O \frac{d(v_{DC}^2)}{dt} = 3 p_{APF} \quad (15)$$

$$\frac{1}{2} C_O \frac{d(V_{DC}^2 + 2V_{DC} \hat{v}_{DC} + \hat{v}_{DC}^2)}{dt} = 3 P_{APF} + 3 \hat{p}_{APF} \quad (16)$$

Removing the dc terms and terms with order higher than one, and applying the Laplace transform to (16) yields (17).

$$sC_O V_{DC} \hat{v}_{DC}(s) = 3 \hat{p}_{APF}(s) \quad (17)$$

The Laplace transform is also applied to (14), which is combined with (17) and manipulated into the small signal model (18).

$$\frac{\hat{v}_{DC}(s)}{\hat{v}_L(s)} = \left[ \frac{R_L \left( V_S^2 - 2 \left( \frac{R_L X_S - R_S X_L}{Z_L^2} V_L \right)^2 \right)}{\sqrt{V_S^2 - \left( \frac{R_L X_S - R_S X_L}{Z_L^2} V_L \right)^2}} - 2 \left( \frac{R_L X_L - R_S X_L}{Z_L^2} X_L + R_S + R_L \right) V_L \right] \frac{3}{sC_O V_{DC} Z_L^2} \quad (18)$$

The operating point of the Load-bus voltage in (18) is calculated by considering that the APF is lossless, in (19).

$$V_L = V_S \left| \frac{\overline{Z_L}}{\overline{Z_L} + \overline{Z_S}} \right| \quad (19)$$

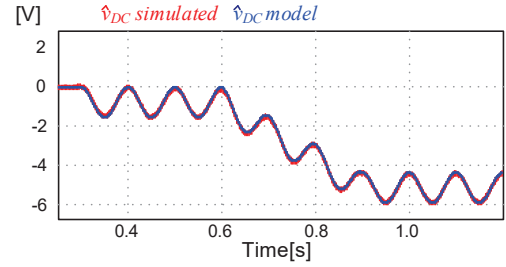
A simpler model can be found if the load impedance is much larger than the source impedance, that is  $R_L \gg R_S$ ,  $X_L \gg X_S$ ,  $Z_L \gg Z_S$ , and is shown in (20). This equation allows for a couple interesting observations of this control strategy. The first one is that the model gain is proportional to the load displacement power factor ( $R_L/Z_L$ ), and is zero if the load is purely reactive. This means that highly reactive loads will result in a higher voltage drop in the series APF, decreasing the load voltage. The second one is that the gain is also proportional to the load current amplitude (approximated as  $V_S/Z_L$ ), this does not pose a problem as a lower load current also results in lower power loss in the series APF, partially compensating this lower gain.

$$\frac{\hat{v}_{DC}(s)}{\hat{v}_L(s)} = -\frac{3R_L V_S}{sC_O V_{DC} Z_L^2} \quad (20)$$

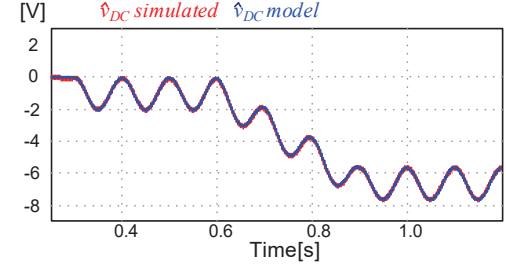
The model was validated by simulating a series APF setting  $v_{rms}^*$  for nominal operation, and applying disturbances into both the model and the simulated APF, and comparing their dynamics, as illustrated by Fig. 5a and Fig. 5b, for different load conditions. The results show that the model closely follows the dynamics of the simulated system, and therefore can be safely used for designing the DC-bus voltage controller.

#### IV. SERIES APF SIMULATION

The proposed control strategy is simulated considering a mix of linear and non-linear loads. The total load power of 45 kVA is shared between three phase resistive loads, inductive-resistive loads, capacitive filter rectifiers and thyristor controlled rectifiers. The simulation parameters are shown in Table I. To provide a real case scenario, the voltage source was distorted by including 5% of third and 3% of fifth harmonics. This voltage distortion is additional to the distortion caused by the non-linear loads in the PCC-bus voltage. The phase voltages are unbalanced with fundamental amplitudes of 127 Vrms, 120 Vrms, and 134 Vrms in each



(a) Case I:  $\overline{Z_L} = (4.57 + j5)\Omega$ .



(b) Case II:  $\overline{Z_L} = 4.57\Omega$ .

Fig. 5. DC-bus voltage dynamics of the simulated series APF and small signal model for a disturbance of 1V, 10Hz@0.3s, a 0.3V@0.6s step and, a -0.3V@0.9s step.  $\overline{Z_S} = (0.019 + j0.058)\Omega$ ,  $V_S = 127\text{Vrms}$ ,  $V_{DC} = 520\text{V}$ .

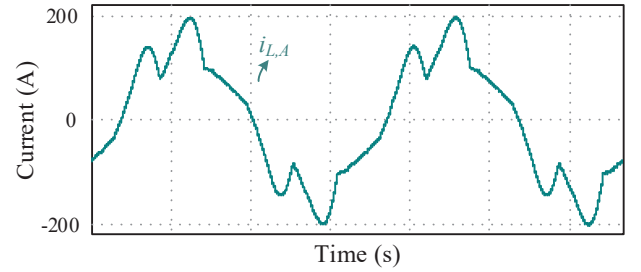


Fig. 6. Total load current at phase A ( $i_{L,A}$ ) considered in the simulation (5ms/div).

phase. The source current for phase A of the simulated system is shown in Fig. 6 and has a  $\text{THD}_i$  of 23.0%.

Waveforms of the source voltage  $v_S$ , the PCC-bus voltage  $v_{PCC}$ , and the Load-bus voltage  $v_L$  already compensated by the series APF control system are shown in Fig. 7. The load-bus voltage is balanced, as the same amplitude reference is used for all three phases. A voltage total harmonic distortion ( $\text{THD}_v$ ) of approximately 3.5% was achieved, within recommend values by standard IEEE 519 [16]. Simulation measurements of  $\text{THD}_v$  and Load-bus rms voltages with and without the series APF are shown in Table II.

After the system start-up the DC-bus voltage controller was able to track the reference without steady state error in approximately 0.4 s as shown in Fig. 8. The DC-bus capacitor initial condition represents a typical pre-charge system.

In order to validate the dynamics of the DC-bus controller, a voltage source step was applied to the system. Starting from a nominal condition of balanced source voltages with 127 Vrms per phase, a positive step of 10 Vrms is applied to the source voltage, followed by a negative step of 10 Vrms 0.6 s latter.

TABLE I  
SIMULATION PARAMETERS

| Symbol             | Quantity                        | Value         | Symbol      | Quantity                                      | Value                   |
|--------------------|---------------------------------|---------------|-------------|-----------------------------------------------|-------------------------|
| $S_L$              | Three-Phase Load Apparent Power | 45 kVA        | $\bar{Z}_S$ | Source Impedance                              | $0.019 + j0.058 \Omega$ |
| $V_{L,nom}$        | Load-bus Nominal Voltage        | 127 Vrms      | $\bar{Z}_L$ | Equivalent Load Impedance                     | $0.842 + j0.546 \Omega$ |
| $V_{DC}$           | Total DC-Bus Voltage            | 520 V         | $S_R$       | Resistive Load Power                          | 20% $S_L$               |
| $\omega$           | Angular Frequency               | $2\pi 60$ rad | $S_{RL}$    | Resistive-inductive Load Power                | 30% $S_L$               |
| $L_A, L_B, L_C$    | ac Side Inductors               | 150 $\mu H$   | $S_{CFR}$   | 3 $\phi$ Capacitive Filter Rectifier Power    | 30% $S_L$               |
| $C_A, C_B, C_C$    | ac Side Capacitors              | 75 $\mu F$    | $S_{THY}$   | 3 $\phi$ Thyristor Controlled Rectifier Power | 20% $S_L$               |
| $C_{O,1}, C_{O,2}$ | DC-bus Capacitors               | 5.6 mH        | $f_s$       | Switching Frequency                           | 15 kHz                  |

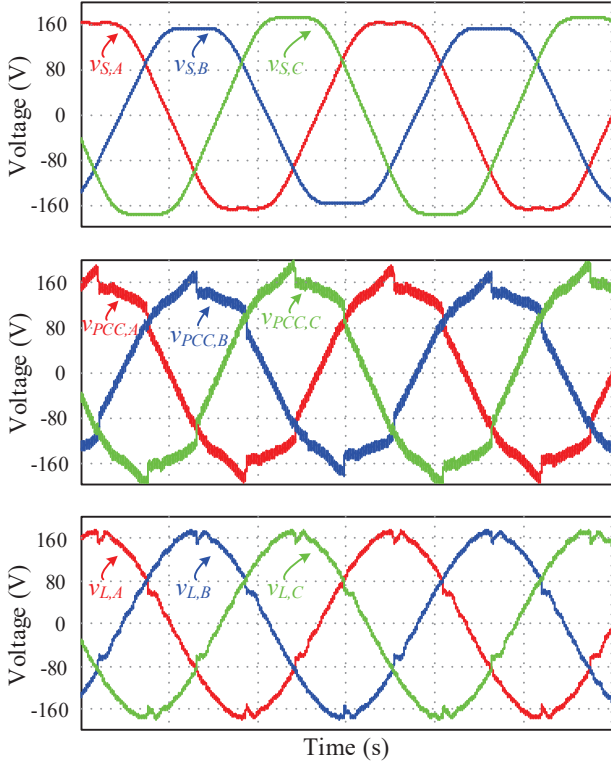


Fig. 7. Waveforms of the source voltage  $v_S$ , the PCC-bus voltage  $v_{PCC}$  and the Load-bus voltage  $v_L$ , for phases A, B, and C (5ms/div).

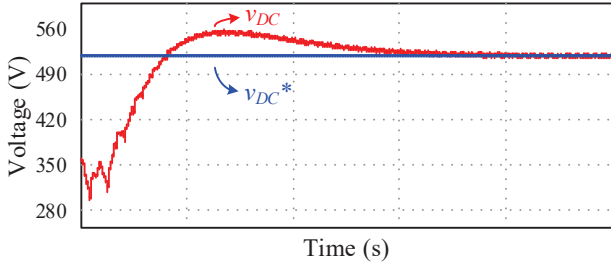


Fig. 8. DC-bus voltage reference  $v_{DC}^*$  and simulated DC-bus voltage at system start-up (100ms/div).

Waveforms of the DC-bus voltage  $v_{DC}$ , the PCC-bus voltage  $v_{PCC}$ , the Load-bus voltage  $v_L$ , the voltage drop in the series APF  $v_{APF}$ , and the DC-bus voltage controller output  $v_{rms}^*$

are shown in Fig. 9. When the positive voltage source step occurs the PCC-bus voltage also increases, nevertheless the DC-bus voltage controller output (which is the Load-bus rms amplitude reference) does not change immediately, increasing the voltage drop and power absorbed by the series APF. This increase in absorbed power leads to an increase in the DC-bus voltage. The DC-bus controller then reacts by increasing the Load-bus voltage amplitude reference, which reduces the voltage drop in the series APF back to the level required for compensating its power loss.

At the start of the negative source voltage step the Load-bus voltage reference is higher than the new PCC-bus voltage, this leads to a phase inversion of the voltage drop in the series APF (i.e., the series APF delivers active power to the load for a short time) and a drop in the DC-bus voltage. The DC-bus controller output then reduces the Load-bus voltage amplitude reference, increasing the voltage drop in the series APF back to the level required for compensating its power loss.

## V. CONCLUSION

This paper presented a DC-bus voltage control strategy for a three-phase four-wire series APF connected to the load through a coupling transformer without using an auxiliary dc source. A model relating the DC-bus voltage of the series APF and the voltage at the load was proposed and validated through simulation and demonstrated to be suitable for controlling the DC-bus voltage and balancing the phases voltages, when considering that the Load-bus voltage harmonics were already compensated by a cascaded high-bandwidth controller.

Different from other works, the DC-bus voltage small signal model was deduced considering the fundamental frequency dynamics of the load. This is advantageous because it shows that there is a relationship between the model gain and the load current and power factor, and that different load conditions should be analyzed when designing the control system. Furthermore, the load voltage was directly measured for feedback instead of the output voltage of the series APF, this allows for a simpler control strategy with high rejection of distortions at the load side, even when using a coupling transformer.

## ACKNOWLEDGMENT

The authors would like to thank UDESC, FAPESC, CAPES, and FITEJ for the financial support of this work.

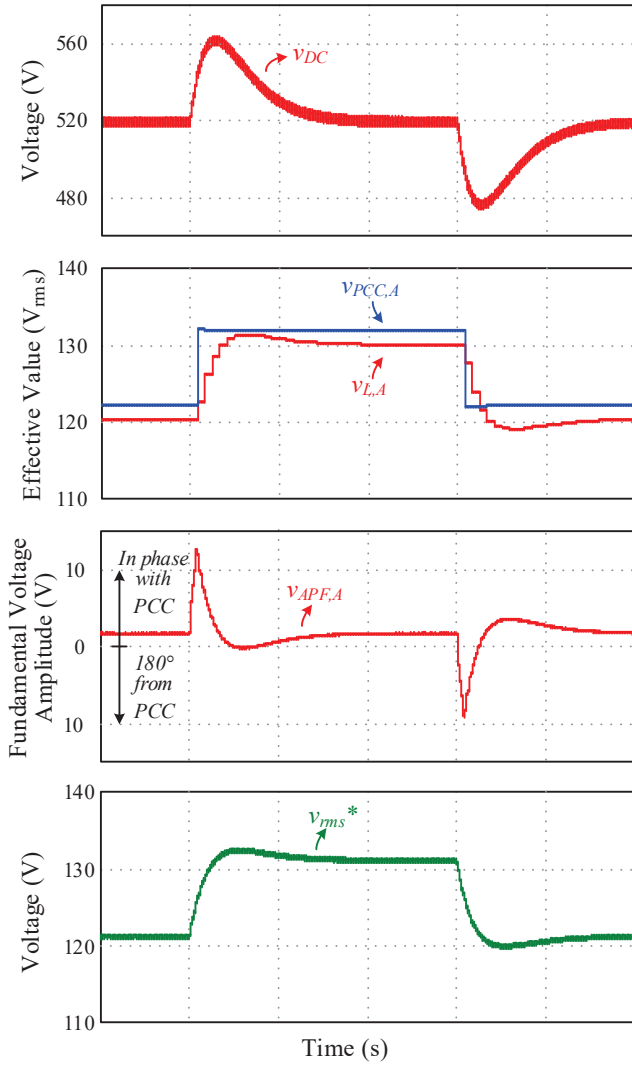


Fig. 9. Simulated waveforms of the DC-bus voltage  $v_{DC}$ , the PCC-bus voltage  $v_{PCC}$ , the Load-bus voltage  $v_L$ , the voltage drop in the series APF  $v_{APF}$  and the DC-bus voltage controller output  $v_{rms}^*$  for a positive step of 10 Vrms followed by a negative step of 10 Vrms in the source voltage amplitude (200ms/div).

TABLE II

THD AND RMS VALUES OF THREE-PHASE LOAD VOLTAGES WITH AND WITHOUT COMPENSATION.

| Variable         | Without Series APF | With Series APF |
|------------------|--------------------|-----------------|
| THD $_{v,A}$ (%) | 7.60               | 3.54            |
| THD $_{v,B}$ (%) | 7.09               | 3.48            |
| THD $_{v,C}$ (%) | 5.18               | 3.50            |
| $v_{L,A}$ (Vrms) | 121.48             | 120.38          |
| $v_{L,B}$ (Vrms) | 115.19             | 120.59          |
| $v_{L,C}$ (Vrms) | 129.19             | 120.34          |

## REFERENCES

- [1] P. Fang Zheng, "Application issues of active power filters," *IEEE Industry Applications Magazine*, vol. 4, no. 5, pp. 21–30, 1998.
- [2] E. R. Ribeiro and I. Barbi, "Harmonic voltage reduction using a series active filter under different load conditions," *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1394–1402, 2006.
- [3] C. B. Jacobina, A. C. Oliveira, R. R. Matias, and A. P. D. Queiroz, "Three-phase series active power filter without dc voltage source," in *2008 IEEE Power Electronics Specialists Conference*, June 2008, pp. 880–884.
- [4] M. Aredes and E. H. Watanabe, "New control algorithms for series and shunt three-phase four-wire active power filters," *IEEE Transactions on Power Delivery*, vol. 10, no. 3, pp. 1649–1656, Jul 1995.
- [5] J. G. Pinto, H. Carneiro, B. Exposto, C. Couto, and J. L. Afonso, "Transformerless series active power filter to compensate voltage disturbances," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, Aug 2011, pp. 1–6.
- [6] G. Carlos and C. Jacobina, "Series compensator based on cascaded transformers coupled with three-phase bridge converters," *IEEE Transactions on Industry Applications*, vol. PP, no. 99, pp. 1–1, 2016.
- [7] Y. Chang, L. Jinjun, W. Xiaoyu, and W. Zhaoan, "A novel control of series active power filter without harmonics detection," in *2007 IEEE Power Electronics Specialists Conference*, Conference Proceedings, pp. 1112–1115.
- [8] S. Srianthumrong, H. Fujita, and H. Akagi, "Stability analysis of a series active filter integrated with a double-series diode rectifier," *IEEE Transactions on Power Electronics*, vol. 17, no. 1, pp. 117–124, Jan 2002.
- [9] J. Turunen, M. Salo, and H. Tuusa, "The influence of the dc-link voltage control on the current harmonic filtering of the series hybrid active power filters," in *31st Annual Conference of IEEE Industrial Electronics Society, 2005. IECON 2005.*, Nov 2005, pp. 6 pp.–.
- [10] R. J. M. d. Santos, J. C. d. Cunha, and M. Mezaroba, "A simplified control technique for a dual unified power quality conditioner," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 11, pp. 5851–5860, 2014.
- [11] V. Khadkikar, "Enhancing electric power quality using upqc: A comprehensive overview," *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2284–2297, 2012.
- [12] H. Akagi, E. H. Watanabe, and M. Aredes, *Instantaneous power theory and applications to power conditioning*. John Wiley & Sons, 2007, vol. 31.
- [13] A. M. Rauf and V. Khadkikar, "An enhanced voltage sag compensation scheme for dynamic voltage restorer," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 2683–2692, 2015.
- [14] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and J. Cabaleiro, "Robust phase locked loops optimized for dsp implementation in power quality applications," in *2008 34th Annual Conference of IEEE Industrial Electronics*, Nov 2008, pp. 3052–3057.
- [15] J. Dias, M. Mezaroba, C. Rech, L. Michels, and T. D. Busarello, "Controle digital simplificado para um compensador unificado de qualidade de energia," in *XVIII Congresso Brasileiro de Automtica*, Conference Proceedings, pp. 2549–2556.
- [16] "IEEE recommended practice and requirements for harmonic control in electric power systems," *IEEE Std 519-2014 (Revision of IEEE Std 519-1992)*, pp. 1–29, 2014.